ZC702 Evaluation Board for the Zynq-7000 XC7Z020 All Programmable SoC

User Guide

UG850 (v1.2) April 4, 2013

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Revision History

The following table shows the revision history for this document.

Date	Version	Revision
05/24/2012	1.0	Initial Xilinx release.
10/08/2012	1.1	The board photo in Figure 1-2 was updated. Table 1-2, Switch SW16 Configuration Option Settings was added. The part number in Quad-SPI Flash Memory, page 19 changed to N25Q128A13ESF40F. In Table 1-6, the J35 shunt controls OTG and Device mode. The frequency jitter in System Clock, page 28 changed from 20 ppm to 50 ppm. The action description under Program_B Pushbutton, page 49 changed. The 34 differential user-defined signals are defined as 34 LA pairs, LA00–LA33, in LPC Connectors J3 and J4, page 51. In the same section, 34 differential user-defined pairs changed to 68 single-ended or 34 differential user-defined signals. Appendix F, Regulatory and Compliance Information now includes a link to the Declaration of Conformity and markings for waste electrical and electronic equipment (WEEE), restriction of hazardous substances (RoHS), and CE compliance.

Date	Version	Revision
04/04/2013	1.2	Chapter 1, ZC702 Evaluation Board Features: Marvell 88E1111 was changed to Marvell 88E1116R throughout the document. The bullet just before Block Diagram, page 9 changed from PL JTAG header to PS JTAG header. In Table 1-1, page 11, callout 3, P*C28F00AG18FE StrataFlash memory* changed to 128 Mb, N25Q128A11ESF40G. In callout 9, Marvell M88E1116R-BAB1C000 changed to 88E1116RA0-NNC1C000. Callout 30 for J59 and 31 for J60 were added. The Zynq-7000 XC7Z020 AP SoC, page 12 description for callout 1 changed. Callout 29 added a link to Table 1-2. Table 1-2 was removed because it is a duplicate of Table 1-10. Above Table 1-2, page 15, "configuration option" was changed to "*JTAG* configuration option." In Table 1-2, the *PLL Used mode* row was removed and the default setting changed. Section Encryption Key Backup Circuit, page 15 was added. In I/O Voltage Rails, page 16, "There are four I/O banks available on the XC7Z020 AP SoC" was changed to "There are four *PL* I/O banks available on the XC7Z020 AP SoC." A note about DDR3 memory was added after Table 1-4, page 17. In Quad-SPI Flash Memory, page 19 and Figure 1-6, *N25Q128A13ESF40F* (Micron/Numonyx) changed to N25Q128A11ESF40G. In Quad-SPI Flash Memory, page 19, "The configuration section of UG585..." was changed to add "The configuration *and QSPI* section of UG585..." JTAG information in Figure 1-10 and Table 1-10 was updated. In Figure 1-10 pin numbers 5 and 6 are swapped and in U76, IN2 and IN1 switched places. In Table 1-10, *SW10* became SW10[1:2] in the table column heading and the default setting was added. In Processing System Clock Source, page 29, frequency jitter changed from 20 ppm to 50 ppm. In I2C Bus, page 36, NXP semiconductor changed to TI. Figure 1-15 is updated. R249 was added to Figure 1-17. In Table 1-22, reference designator DS12 changed to DS14. U3 level shifter was changed to TXS0104E in Figure 1-19 and Table 1-21. The User I/O, page 42 section was updated. Figure 1-21 added two LEDs. Table 1-23 added Net Name PS_LED1 and PS_MIO8_LED0 and removed pin info. Section User PS Switches, page 46 was added. The Figure 1-26 title changed. A paragraph about design criteria was added to Power Management, page 55. A paragraph about the TI Fusion Digital Power graphical user interface precedes Table 1-30. Voltages were added to the description of U19 in Table 1-30. The TI link on page 58 was updated. Appendix A, Default Switch and Jumper Settings: In Table A-1, SW16 position 4 changed from right to left. Appendix C, Master UCF Listing: A reminder was added to use the latest UCF listing. Minor changes were made to the list, and power and ground pin constraints were removed. Appendix D, Board Specifications: This appendix was added to the book. Appendix F, Regulatory and Compliance Information: A link to the ZC702 board master answer record was added.

Table of Contents

ZC702 Evaluation Board Features

Overview

The ZC702 evaluation board for the XC7Z020 All Programmable SoC (AP SoC) provides a hardware environment for developing and evaluating designs targeting the Zynq™-7000 XC7Z020-1CLG484C AP SoC. The ZC702 board provides features common to many embedded processing systems, including DDR3 component memory, a tri-mode Ethernet PHY, general purpose I/O, and two UART interfaces. Other features can be supported using VITA-57 FPGA mezzanine cards (FMC) attached to either of two low pin count (LPC) FMC connectors.

ZC702 Board Features

The ZC702 board features are listed in here. Detailed information for each feature is provided in Feature Descriptions starting on page 12.

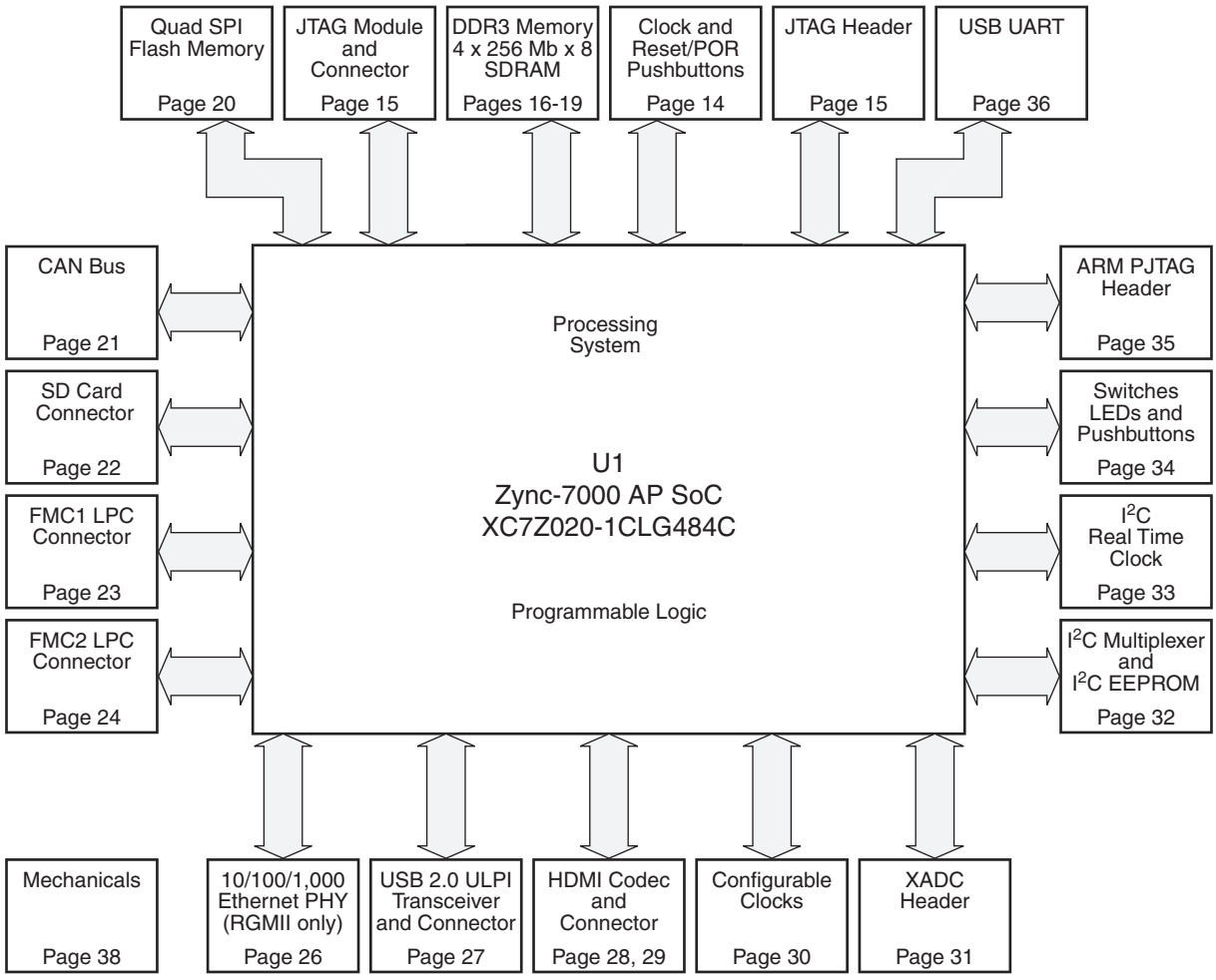
- Zynq-7000 XC7Z020-1CLG484C AP SoC
- 1 GB DDR3 component memory (four 256 Mb x 8 devices)
- 128 Mb Quad SPI flash memory
- USB 2.0 ULPI (UTMI+ low pin interface) transceiver
- Secure Digital (SD) connector
- USB JTAG interface via Digilent module
- Clock sources:
  - Fixed 200 MHz LVDS oscillator (differential)
  - I^2C programmable LVDS oscillator (differential)
  - Fixed 33.33 MHz LVCMOS oscillator (single-ended)
- Ethernet PHY RGMII interface with RJ-45 connector
- USB-to-UART bridge
- HDMI codec
- I^2C bus

- I^2C bus multiplexed to:
  - Si570 user clock
  - ADV7511 HDMI codec
  - M24C08 EEPROM (1 kB)
  - 1-To-16 TCA6416APWR port expander
  - RTC-8564JE real time clock
  - FMC1 LPC connector
  - FMC2 LPC connector
  - PMBUS data/clock
- Status LEDs:
  - Ethernet status
  - Power good
  - FPGA INIT
  - FPGA DONE
- User I/O:
  - Two programmable logic (PL) user pushbuttons
  - PL user DIP switch (2-pole)
  - Eight PL user LEDs
  - Two processing system (PS) pushbuttons shared with PS 2-pole DIP switch
  - Two PS user LEDs
  - Dual row Pmod GPIO header
  - Single row Pmod GPIO header
- AP SoC PS Reset Pushbuttons:
  - SRST_B PS reset button
  - POR_B PS reset button
- Two VITA 57.1 FMC LPC connectors
- Power on/off slide switch
- Power management with PMBus voltage and current monitoring via TI power controllers
- Dual 12-bit 1 MSPS XADC analog-to-digital front end
- Configuration options:

- Quad SPI flash memory
- USB JTAG configuration port (Digilent module)
- Platform cable header JTAG configuration port
- 20-pin PL PJTAG header
- 20-pin PS JTAG header

Block Diagram

The ZC702 board block diagram is shown in Figure 1-1.



Note: Page numbers reference the page number of schematic 0381449.

Figure 1-1: **ZC702 Board Block Diagram**

Board Layout

Figure 1-2 shows the ZC702 board. Each numbered feature that is referenced in Figure 1-2 is described in Table 1-1 with a link to detailed information provided under Feature Descriptions starting on page 12.

CAUTION! *The ZC702 board can be damaged by electrostatic discharge (ESD). Follow ESD prevention measures when handling the board.*

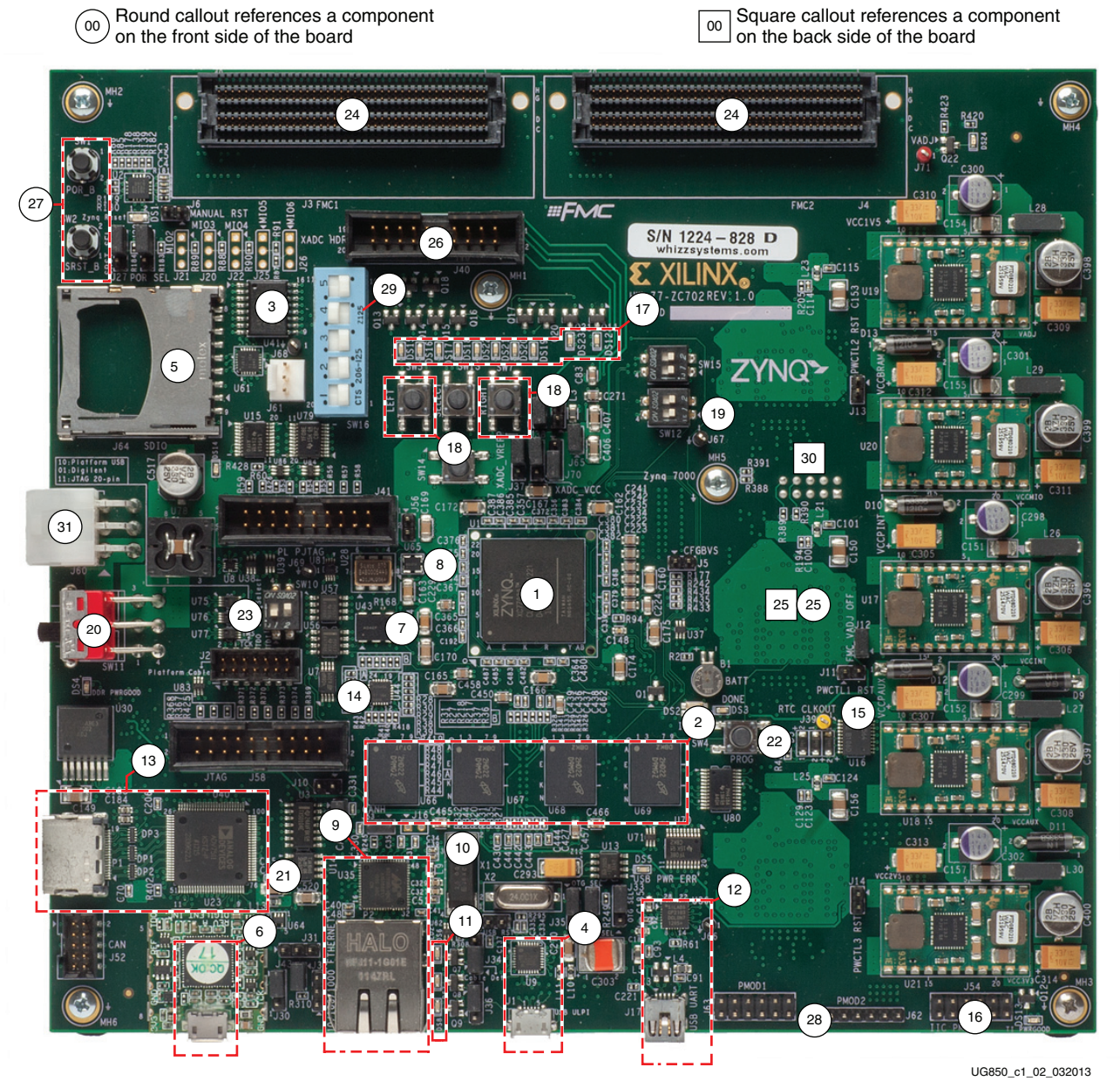


Figure 1-2: **ZC702 Board Component Locations**

Note: The image in Figure 1-2 is for reference only and might not reflect the current revision of the board.

Table 1-1: **ZC702 Board Component Descriptions**

Callout	Reference Designator	Component Description	Notes	Schematic[1] 0381449 Page Number
1	U1	Zynq-7000 XC7Z020 AP SoC	Xilinx part number: XC7Z020-1CLG484C	
2	U66–U69	DDR3 Component Memory, 1 GB	4 each 256Mb X 8 SDRAM Micron Technology Inc, MT41J256M8DA-107	16–19
3	U41	Quad-SPI Flash Memory, 128 Mb	Micron/Numonyx N25Q128A11ESF40G	20
4	U9, J1	USB 2.0 ULPI Transceiver, USB Mini-B connector	SMSC USB3320-EZK High-Speed USB transceiver	27
5	J64	SD Card Interface connector	Molex 67840-8001 SDIO Memory card connector	22
6	U23	Programmable Logic JTAG Programming Options with integrated Micro-B connector	Digilent USB JTAG Module	15
7	U43	System Clock, 200 MHz, 2.5V LVDS oscillator	SiTime SIT9102-243N25E200.0000	30
8	U28, U65	Programmable User Clock and Processing System Clock Source	Silicon Labs SI570BAB0000544DG, default 156.250MHz, PS fixed 33 MHz clock	30
9	U35, P2	10/100/1,000 MHz Tri-Speed Ethernet PHY, RJ45 w/magnetics	Marvell 88E1116RA0-NNC1C000, Halo HFJ11-1G01ERL	25–26
10	X1	Ethernet PHY Clock Source, 25.000 MHz	Epson MA-506-25.000m-CO:ROHS	25
11	DS6–DS8	Ethernet PHY User LEDs	Ethernet PHY User LEDs, GREEN	25
12	U36, J17	USB-to-UART Bridge, USB Mini-B connector	Silicon Labs CP2103GM, Molex 54819-0589	36
13	U40, P1	HDMI Video Output	Analog Devices ADV7511KSTZ-P HDMI transmitter, Molex 500254-1927 HDMI receptacle	28–29
14	U44	I2C Bus	TI PCA9548ARGER	32
15	U16	Real Time Clock	Epson RTC-8564JE:3:ROHS	33
16	J54	I/O Expansion Header driven from I^2C Expander U80	2-row pin header	33
17	DS15–DS22	User LEDs	GPIO LEDs, GREEN 0603	34
18	SW5, SW7	User Pushbuttons SW5 = Left, SW7 = Right	E-Switch TL3301EP100QG	34
19	SW12	GPIO DIP Switch	2-pole C&K SDA02H1SBD	34
20	SW11	Power On/Off Slide Switch	C and K 1201M2S3AQE2	47

Table 1-1: **ZC702 Board Component Descriptions *(Cont'd)***

Callout	Reference Designator	Component Description	Notes	Schematic[1] 0381449 Page Number
21	U14	High Speed CAN Transceiver	NXP TJA1040T/VM	21
22	SW4	Program_B Pushbutton	E-Switch TL3301EP100QG	34
23	SW10, J2	Programmable Logic JTAG Select Switch, JTAG Cable Connector	2-pole C and K SDA02H1SBD MOLEX 87832-1420	15
24	J3, J4	FPGA Mezzanine (FMC) Card Interface	Samtec ASP_134486_01	23, 24
25	U32, U33, U34	Power Management (bottom and top of board)	TI UCD9248PFC in conjunction with various regulators	39–47
26	J40	XADC Analog-to-Digital Converter	2X10 0.-inch male header	31
27	SW1, SW2	PS Power-On and System Reset Pushbuttons	Panasonic EVQ-11L07K 14	35, 36
28	J62, J63	User PMOD GPIO Headers	J63 2 x 6 0.1 inch J63 1 x 6 0.1 inch male headers	34, 35
29	SW16	5-pole SPDT MIO DIP switch	CTS 206-125. See Table 1-2 for switch settings.	14
30	J59	2x5 shrouded PMBus connector (bottom of board)	ASSMAN HW10G-0202	47
31	J60	12V power input 2x6 connector	MOLEX 39-30-1060	47

Notes:

1. The ZC702 board schematics are available for download from http://www.xilinx.com/products/boards-and-kits/EK-Z7-ZC702-G.htm.

Feature Descriptions

Detailed information for each feature shown in Figure 1-2 and listed in Table 1-1 is provided in this section.

Zynq-7000 XC7Z020 AP SoC

[Figure 1-2, callout 1]

The ZC702 board is populated with the Zynq-7000 XC7Z020-1CLG484C AP SoC. The XC7Z020 AP SoC consists of an SoC-style integrated processing system (PS) and programmable logic (PL) on a single die. The high-level block diagram is shown in Figure 1-3.

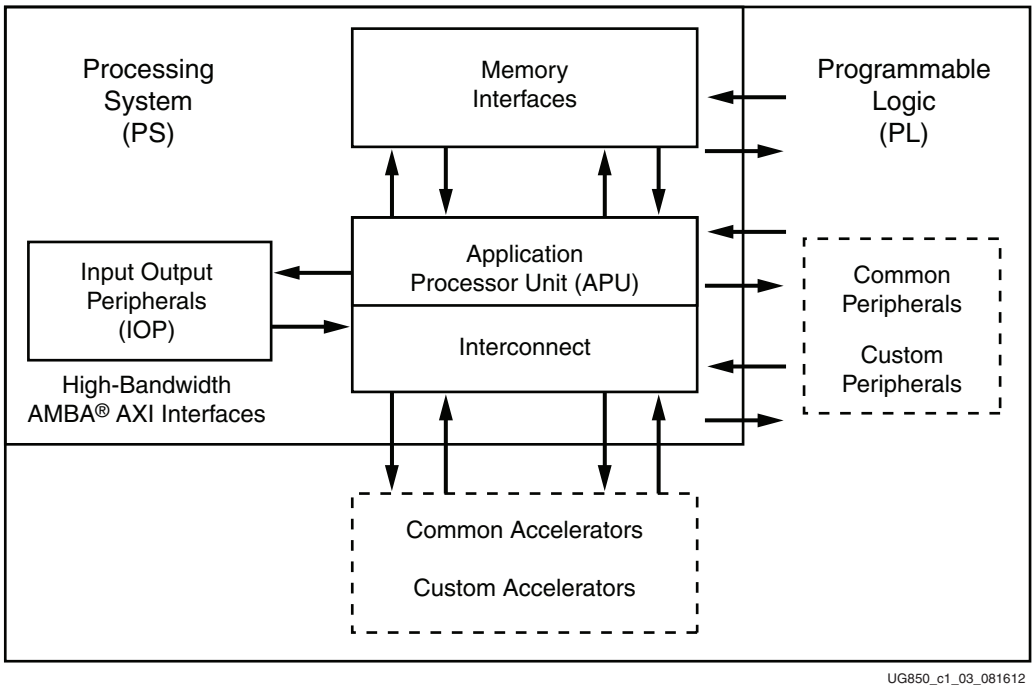


Figure 1-3: **High-Level Block Diagram**

The PS integrates two ARM® Cortex™-A9 MPCore™ application processors, AMBA® interconnect, internal memories, external memory interfaces, and peripherals including USB, Ethernet, SPI, SD/SDIO, I^2C, CAN, UART, and GPIO. The PS runs independently of the PL and boots at power-up or reset.

A system level block diagram is shown in Figure 1-4.

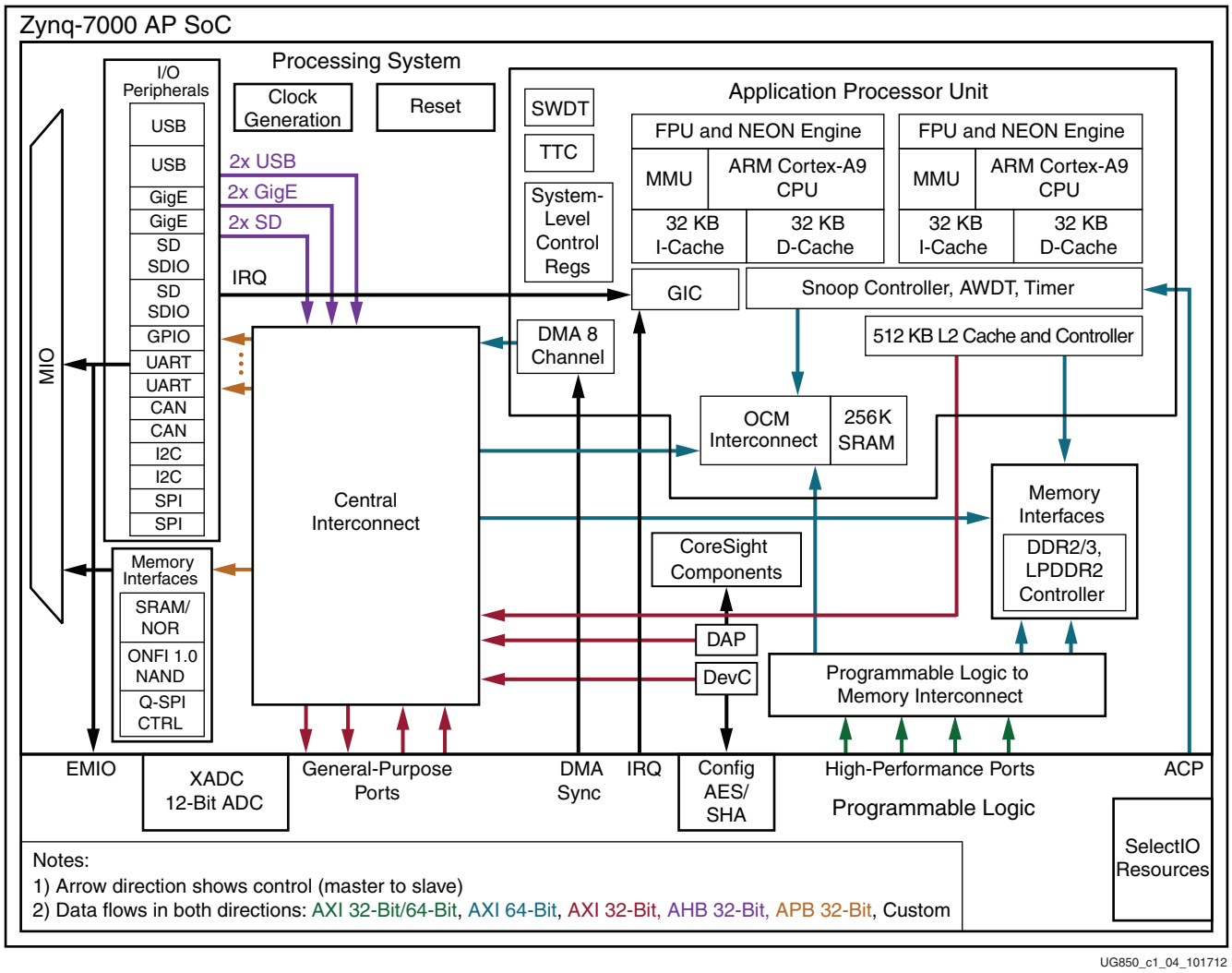


Figure 1-4: **Zynq-7000 AP SoC Block Diagram**

For additional information on Zynq-7000 AP SoC devices, see DS190, *Zynq-7000 All Programmable SoC Overview,* and UG585, *Zynq-7000 All Programmable SoC Technical Reference Manual* for more information about Zynq-7000 AP SoC configuration options.

Device Configuration

Zynq-7000 XC7Z020 AP SoC uses a multi-stage boot process that supports both a non-secure and a secure boot. The PS is the master of the boot and configuration process. For a secure boot, the PL must be powered on to enable the use of the security block located within the PL, which provides 256-bit AES and SHA decryption/authentication.

The ZC702 board supports these configuration options:

- PS Configuration: Quad SPI flash memory
- PS Configuration: Processor System Boot from SD Card (J64)

- PL Configuration: USB JTAG configuration port (Digilent module)
- PL Configuration: Platform cable header J2 and flying lead header J58 JTAG configuration ports

TIP: *Designs using serial configuration based on Quad-SPI flash memory can take advantage of low-cost commodity SPI flash memory.*

The JTAG configuration option is selected by setting SW16 as shown in Table 1-2 and SW10 as described in Programmable Logic JTAG Programming Options, page 25 for PL configuration details. SW10 is callout 23 in Figure 1-2.

Table 1-2: **Switch SW16 Configuration Option Settings**

Boot Mode	SW16.1	SW16.2	SW16.3	SW16.4	SW16.5
JTAG mode(1)	0	0	0	0	0
Independent JTAG mode	1	0	0	0	0
QSPI mode	0	0	0	1	0
SD mode	0	0	1	1	0
MIO configuration pin	MIO2	MIO3	MIO4	MIO5	MIO6

Notes:
1. Default switch setting

Note: For more information about Zynq-7000 AP SoC configuration settings, see UG585, *Zynq-7000 All Programmable SoC Technical Reference Manual*.

Encryption Key Backup Circuit

The XC7Z020 AP SoC U1 implements bitstream encryption key technology. The ZC702 board provides the encryption key backup battery circuit shown in Figure 1-5. The Seiko TS518FE rechargeable 1.5V lithium button-type battery B1 is soldered to the board with the positive output connected to the XC7Z020 AP SoC U1 VCCBATT pin G9. The battery supply current IBATT specification is 150 nA maximum when board power is off. B1 is charged from the VCCAUX 1.8V rail through a series diode with a typical forward voltage drop of 0.38V and 4.7 KΩ current limit resistor. The nominal charging voltage is 1.42V.

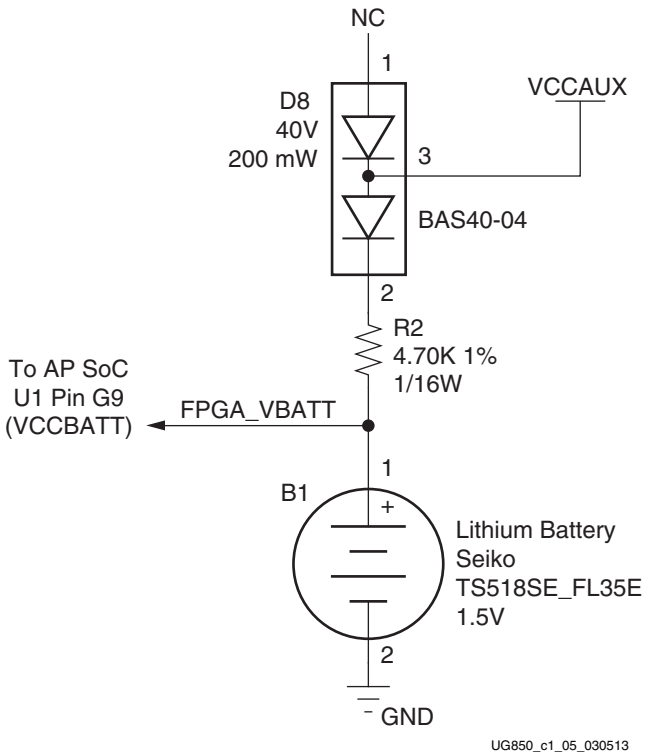


Figure 1-5: **Encryption Key Backup Circuit**

I/O Voltage Rails

There are four PL I/O banks available on the XC7Z020 AP SoC. The voltages applied to the XC7Z020 AP SoC I/O banks used by the ZC702 board are listed in Table 1-3.

Table 1-3: **I/O Voltage Rails**

XC7Z020 (U1) Bank	Net Name	Voltage	Connected To
PL Bank 0	VCC2V5_PL	2.5V	AP SoC Configuration Bank 0
PL Bank 13	VADJ(1)	2.5V	FMC2, GPIO, PL_PJTAG, IIC_MAIN
PL Bank 33			FMC2, HDMI Codec
PL Bank 34			FMC1, HDMI Codec
PL Bank 35			FMC1, HDMI Codec, XADC_GPIO, GPIO
PS Bank 500	VCCMIO_PS	1.8V	Quad-SPI flash memory, misc
PS Bank 501			Ethernet PHY, USB ULPI Transceiver, SDIO, CAN
PS Bank 502	VCC1V5_PS	1.5V	PS_DDR3 MEM

Notes:

1. The ZC702 board is shipped with V_{ADJ} set to 2.5V.

DDR3 Component Memory

[Figure 1-2, callout 2]

The 1 GB, 32-bit wide DDR3 memory system is comprised of four 256 Mb x 8 SDRAMs (Micron MT41J256M8HX-15E) at U66–U69. This memory system is connected to the XC7Z020 AP SoC processing system (PS) memory interface bank 502. The DDR3 0.75V V_{TT} termination voltage is sourced from linear regulator U22. The connections between the DDR3 memory and XC7Z020 AP SoC bank 502 are listed in Table 1-4.

Table 1-4: **DDR3 Component Memory Connections to the XC7Z020 AP SoC**

XC7Z020 (U1) Pin	Net Name	Component Memory		
		Pin Number	Pin Name	Reference Designator
E3	PS_DDR3_DQ0	B3	DQ0	U66
C3	PS_DDR3_DQ1	C7	DQ1	U66
F2	PS_DDR3_DQ2	C2	DQ2	U66
D1	PS_DDR3_DQ3	C8	DQ3	U66
F1	PS_DDR3_DQ4	E3	DQ4	U66
E1	PS_DDR3_DQ5	E8	DQ5	U66
B2	PS_DDR3_DQ6	D2	DQ6	U66
D3	PS_DDR3_DQ7	E7	DQ7	U66
G2	PS_DDR3_DQ8	B3	DQ8	U67
L1	PS_DDR3_DQ9	C7	DQ9	U67
G1	PS_DDR3_DQ10	C2	DQ10	U67
K1	PS_DDR3_DQ11	C8	DQ11	U67
L3	PS_DDR3_DQ12	E3	DQ12	U67
L2	PS_DDR3_DQ13	E8	DQ13	U67
J1	PS_DDR3_DQ14	D2	DQ14	U67
K3	PS_DDR3_DQ15	E7	DQ15	U67
M1	PS_DDR3_DQ16	B3	DQ16	U68
T3	PS_DDR3_DQ17	C7	DQ17	U68
N3	PS_DDR3_DQ18	C2	DQ18	U68
T1	PS_DDR3_DQ19	C8	DQ19	U68
R3	PS_DDR3_DQ20	E3	DQ20	U68
T2	PS_DDR3_DQ21	E8	DQ21	U68
M2	PS_DDR3_DQ22	D2	DQ22	U68
R1	PS_DDR3_DQ23	E7	DQ23	U68
U1	PS_DDR3_DQ24	B3	DQ24	U69

Table 1-4: **DDR3 Component Memory Connections to the XC7Z020 AP SoC *(Cont'd)***

XC7Z020 (U1) Pin	Net Name	Component Memory		
		Pin Number	Pin Name	Reference Designator
AA1	PS_DDR3_DQ25	C7	DQ25	U69
U2	PS_DDR3_DQ26	C2	DQ26	U69
AA3	PS_DDR3_DQ27	C8	DQ27	U69
W1	PS_DDR3_DQ28	E3	DQ28	U69
Y3	PS_DDR3_DQ29	E8	DQ29	U69
W3	PS_DDR3_DQ30	D2	DQ30	U69
Y1	PS_DDR3_DQ31	E7	DQ31	U69
B1	PS_DDR3_DM0	B7	DM0	U66
C2	PS_DDR3_DQS0_P	C3	DQS0_P	U66
D2	PS_DDR3_DQS0_N	D3	DQS0_N	U66
H3	PS_DDR3_DM1	B7	DM1	U67
H2	PS_DDR3_DQS1_P	C3	DQS1_P	U67
J2	PS_DDR3_DQS1_N	D3	DQS1_N	U67
P1	PS_DDR3_DM2	B7	DM2	U68
N2	PS_DDR3_DQS2_P	C3	DQS2_P	U68
P2	PS_DDR3_DQS2_N	D3	DQS2_N	U68
AA2	PS_DDR3_DM3	B7	DM3	U69
V2	PS_DDR3_DQS3_P	C3	DQS3_P	U69
W2	PS_DDR3_DQS3_N	D3	DQS3_N	U69
M4	PS_DDR3_A0	K3	A0	U66, U67, U68, U69
M5	PS_DDR3_A1	L7	A1	U66, U67, U68, U69
K4	PS_DDR3_A2	L3	A2	U66, U67, U68, U69
L4	PS_DDR3_A3	K2	A3	U66, U67, U68, U69
K6	PS_DDR3_A4	L8	A4	U66, U67, U68, U69
K5	PS_DDR3_A5	L2	A5	U66, U67, U68, U69
J7	PS_DDR3_A6	M8	A6	U66, U67, U68, U69
J6	PS_DDR3_A7	M2	A7	U66, U67, U68, U69
J5	PS_DDR3_A8	N8	A8	U66, U67, U68, U69
H5	PS_DDR3_A9	M3	A9	U66, U67, U68, U69
J3	PS_DDR3_A10	H7	A10	U66, U67, U68, U69
G5	PS_DDR3_A11	M7	A11	U66, U67, U68, U69
H4	PS_DDR3_A12	K7	A12	U66, U67, U68, U69
F4	PS_DDR3_A13	N3	A13	U66, U67, U68, U69

Table 1-4: **DDR3 Component Memory Connections to the XC7Z020 AP SoC *(Cont'd)***

XC7Z020 (U1) Pin	Net Name	Component Memory		
		Pin Number	Pin Name	Reference Designator
G4	PS_DDR3_A14	N7	A14	U66, U67, U68, U69
L7	PS_DDR3_BA0	J2	BA0	U66, U67, U68, U69
L6	PS_DDR3_BA1	K8	BA1	U66, U67, U68, U69
M6	PS_DDR3_BA2	J3	BA2	U66, U67, U68, U69
N4	PS_DDR3_CLK_P	F7	CK	U66, U67, U68, U69
N5	PS_DDR3_CLK_N	G7	CK_B	U66, U67, U68, U69
V3	PS_DDR3_CKE	G9	CKE	U66, U67, U68, U69
R4	PS_DDR3_WE_B	H3	WE_B	U66, U67, U68, U69
P3	PS_DDR3_CAS_B	G3	CAS_B	U66, U67, U68, U69
R5	PS_DDR3_RAS_B	F3	RAS_B	U66, U67, U68, U69
F3	PS_DDR3_RESET_B	N2	RESET_B	U66, U67, U68, U69
P6	PS_DDR3_CS_B	H2	CS_B	U66, U67, U68, U69
P5	PS_DDR3_ODT	G1	ODT	U66, U67, U68, U69
M7	PS_VRN			
N7	PS_VRP			
H7	VTTVREF_PS			
P7	VTTVREF_PS			

Note: The ZC702 DDR3 4x 8-bit component memory interface adheres to the constraints guidelines documented in the DDR3 Design Guidelines section of *7 Series FPGAs Memory Interface Solutions v1.8 User Guide* (UG586). The ZC702 DDR3 memory interface is a 40Ω impedance implementation. Other memory interface details are available in UG586 and *7 Series FPGAs Memory Resources User Guide* (UG473).

Quad-SPI Flash Memory

[Figure 1-2, callout 3]

The Quad-SPI flash memory located at U41 provides 128 Mb of non-volatile storage that can be used for configuration and data storage.

- Part number: N25Q128A11ESF40G (Micron/Numonyx)
- Supply voltage: 1.8V
- Data path width: 4 bits
- Data rate: Various depending on Single/Dual/Quad mode

The connections between the SPI flash memory and the XC7Z020 AP SoC are listed in Table 1-5.

Table 1-5: **Quad SPI Flash Memory Connections to the XC7Z020 AP SoC**

XC7Z020 (U1)			Schematic Net Name	Quad-SPI Flash Memory (U41)		MIO Select Header
Pin Name	Bank	Pin Number		Pin Number	Pin Name	
PS_MIO6	500	A4	QSPI_CLK	16	C	J26.2
PS_MIO5	500	A3	QSPI_IO3	1	DQ3_HOLD_B	J25.2
PS_MIO4	500	E4	QSPI_IO2	9	WP_B	J22.2
PS_MIO3	500	F6	QSPI_IO1	8	DQ1	J20.2
PS_MIO2	500	A2	QSPI_IO0	15	DQ0	J21.2
PS_MIO1	500	A1	QSPI_CS_B	7	S_B	NA

Notes:

Each three-pin MIO select header has pin 1 wired to VCCMIO and pin 3 wired to GND.

The configuration and QSPI section of UG585, *Zynq-7000 All Programmable SoC Technical Reference Manual* provides details on using the Quad-SPI flash memory.

Figure 1-6 shows the connections of the linear Quad-SPI flash memory on the ZC702 board. For more details, see the Numonyx N25Q128A11ESF40G data sheet at the Micron website [Ref 1].

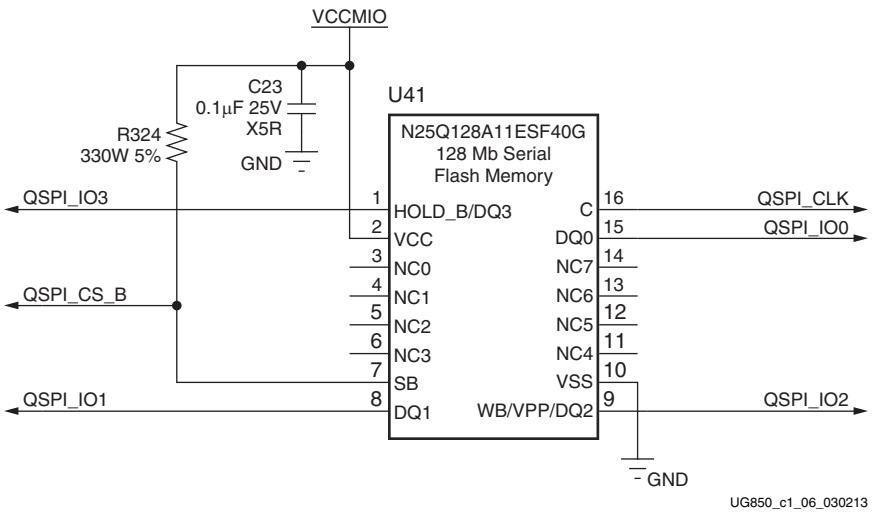


Figure 1-6: **128 Mb Quad-SPI Flash Memory (U41)**

USB 2.0 ULPI Transceiver

[Figure 1-2, callout 4]

The ZC702 board uses a Standard Microsystems Corporation USB3320 USB 2.0 ULPI Transceiver at U9 to support a USB connection to the host computer. A USB cable is supplied in the ZC702 Evaluation Kit (Standard-A connector to host computer, Mini-B connector to ZC702 board connector J1). The USB3320 is a high-speed USB 2.0 PHY supporting the UTMI+ low pin interface (ULPI) interface standard. The ULPI standard defines the interface between the USB controller IP and the PHY device which drives the physical USB bus. Use of the ULPI standard reduces the interface pin count between the USB controller IP and the PHY device.

The USB3320 is clocked by a 24 MHz crystal. Consult the Standard Microsystems Corporation (SMSC) USB3320 data sheet for clocking mode details [Ref 2].

The interface to the USB3320 transceiver is implemented through the IP in the XC7Z020 AP SoC Processor System.

Table 1-6 describes the jumper settings for the USB 2.0 circuit.

Table 1-6: **USB Jumper Settings**

Header	Function	Shunt Position
J44	USB PHY reset	Shunt ON = USB PHY reset Shunt OFF = USB PHY normal operation
J7	Host/OTG or device	Shunt ON = Host or OTG mode Shunt OFF = Device mode
J33	RVBUS select	Position 1–2 = Device mode (10 kΩ) Position 2–3 = Host or OTG mode (1 kΩ)
J35	CVBUS select	Position 1-2 = OTG and Device mode (1 µF) Position 2-3 = Host mode (120 µF)
J34	Cable ID select	Position 1-2 = A/B cable detect Position 2-3 = ID not used
J36	USB Micro-B	Position 1-2 = Shield connected to GND Position 2-3 = Shield floating

The connections between the USB Mini-B connector at J1 and the PHY at U9 are listed in Table 1-7.

Table 1-7: **USB Connector Pin Assignments and Signal Definitions Between J1 and U9**

USB Connector J1		Net Name	Description	USB3320 (U9) Pin
Pin	Name			
1	VBUS	USB_VBUS_SEL	+5V from host system	22
2	D_N	USB_D_N	Bidirectional differential serial data (N-side)	19
3	D_P	USB_D_P	Bidirectional differential serial data (P-side)	18
5	GND	GND	Signal ground	33

The connections between the USB 2.0 PHY at U9 and the XC7Z020 AP SoC are listed in Table 1-8.

Table 1-8: **USB 2.0 ULPI Transceiver Connections to the XC7Z020 AP SoC**

XC7Z020 (U1)			Schematic Net Name	USB3320 (U9) Pin
Pin Name	Bank	Pin Number		
PS_MIO36	501	A9	USB_CLKOUT	1
PS_MIO31	501	F9	USB_NXT	2
PS_MIO32	501	C7	USB_DATA0	3
PS_MIO33	501	G13	USB_DATA1	4
PS_MIO34	501	B12	USB_DATA2	5
PS_MIO35	501	F14	USB_DATA3	6
PS_MIO28	501	A12	USB_DATA4	7
PS_MIO37	501	B14	USB_DATA5	9
PS_MIO38	501	F13	USB_DATA6	10
PS_MIO39	501	C13	USB_DATA7	13
PS_MIO30	501	A11	USB_STP	29
PS_MIO29	501	E8	USB_DIR	31
PS_MIO7	500	D5	USB_RESET_B_AND	27 (via AND gate U62)

Figure 1-7 shows the USB 2.0 ULPI Transceiver circuitry. Note that the shield for the USB Mini-B connector (J1) can be tied to GND by a jumper on header J36 pins 1–2 (default). The USB shield can optionally be connected through a capacitor to GND by installing a capacitor (body size 0402) at location C202 and jumping pins 2-3 on header J36.

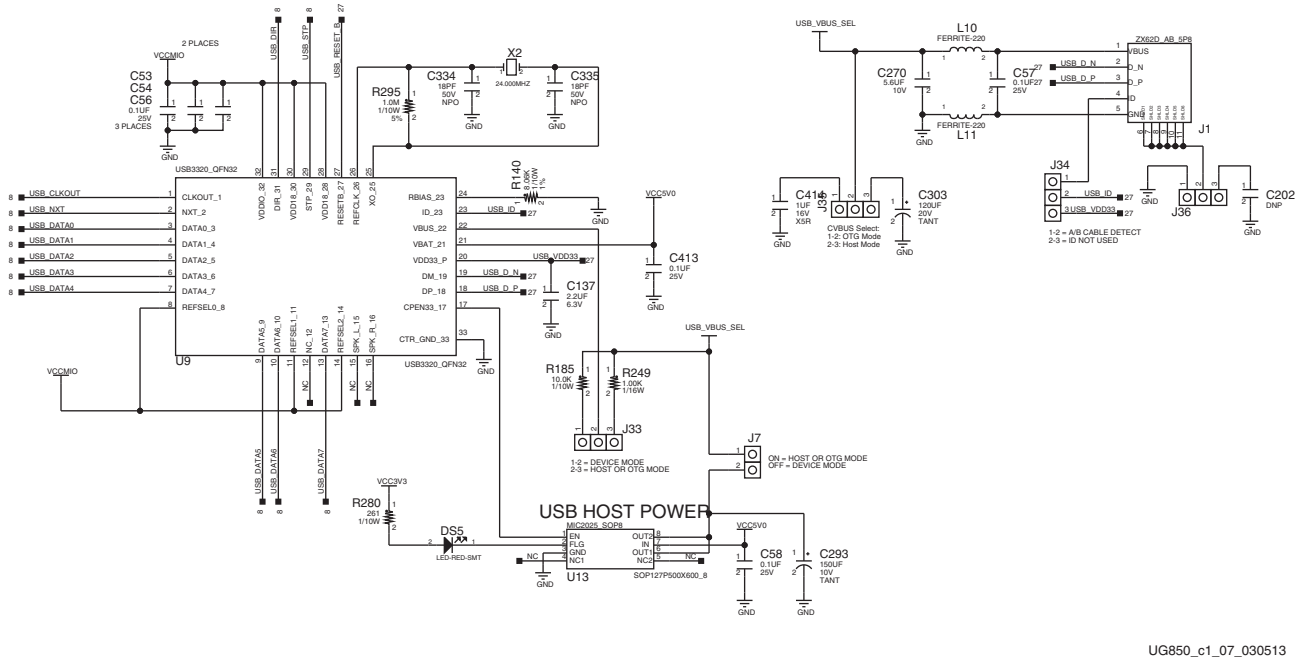


Figure 1-7: **USB 2.0 ULPI Transceiver**

SD Card Interface

[Figure 1-2, callout 5]

The ZC702 board includes a secure digital input/output (SDIO) interface to provide user-logic access to general purpose non-volatile SDIO memory cards and peripherals. Information for the SD I/O card specification can be found at the SanDisk Corporation [Ref 3] or SD Association [Ref 4] websites.

The SDIO signals are connected to XC7Z020 AP SoC PS bank 501 which has its VCCMIO set to 1.8V. A TXB02612 SDIO port expander with voltage-level translation (U61) is used between the XC7Z020 AP SoC and the SD card connector (J64).

Figure 1-8 shows the connections of the SD card interface on the ZC702 board.

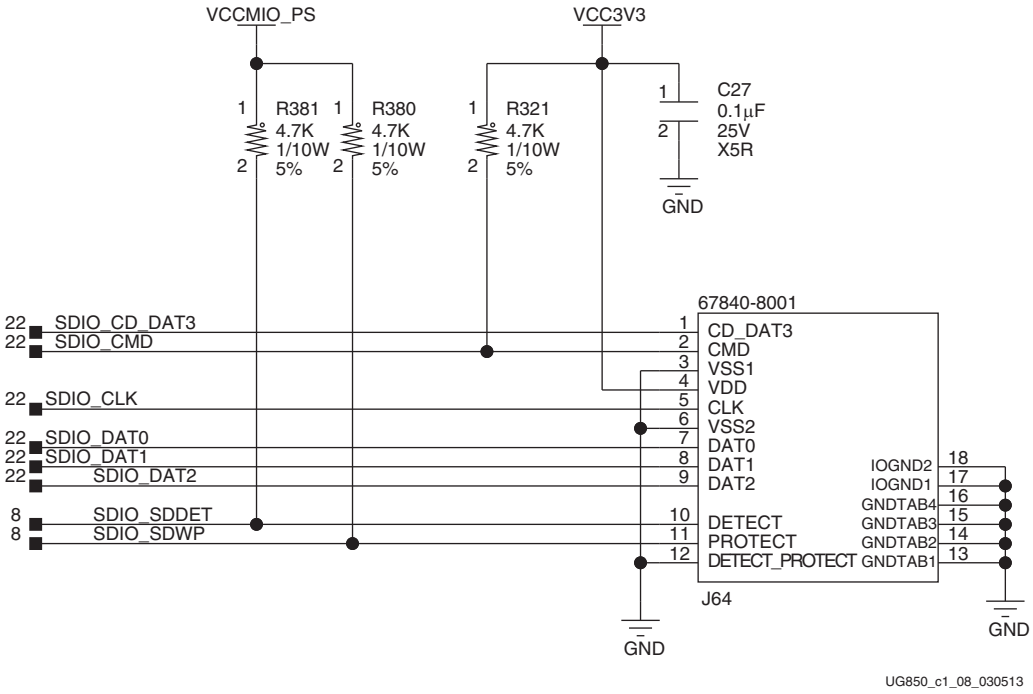


Figure 1-8: **SD Card Interface**

Table 1-9 lists the SD card interface connections to the XC7Z020 AP SoC.

Table 1-9: **SDIO Connections to the XC7Z020 AP SoC**

XC7Z020 (U1) Pin			Schematic Net Name	Level Shifter (U61)		SDIO Connector (J64)	
Pin Name	Bank	Pin Number		(A) Pin Number	(B) Pin Number	Pin Number	Pin Name
PS_MIO15	500	E6	SDIO_SDWP	N/A	N/A	11	PROTECT
PS_MIO0	500	G6	SDIO_SDDET	N/A	N/A	10	DETECT
PS_MIO41	501	C8	SDIO_CMD_LS	4	20	2	CMD
PS_MIO40	501	E14	SDIO_CLK_LS	9	19	5	CLK
PS_MIO42	501	D8	SDIO_DAT2_LS	1	23	9	DAT2
PS_MIO45	501	B9	SDIO_DAT1_LS	7	16	8	DAT1
PS_MIO44	501	E13	SDIO_DAT0_LS	6	18	7	DAT0
PS_MIO43	501	B11	SDIO_CD_DAT3_LS	3	22	1	CD_DAT3

Programmable Logic JTAG Programming Options

[Figure 1-2, callout 6]

The ZC702 board JTAG chain is shown in Figure 1-9.

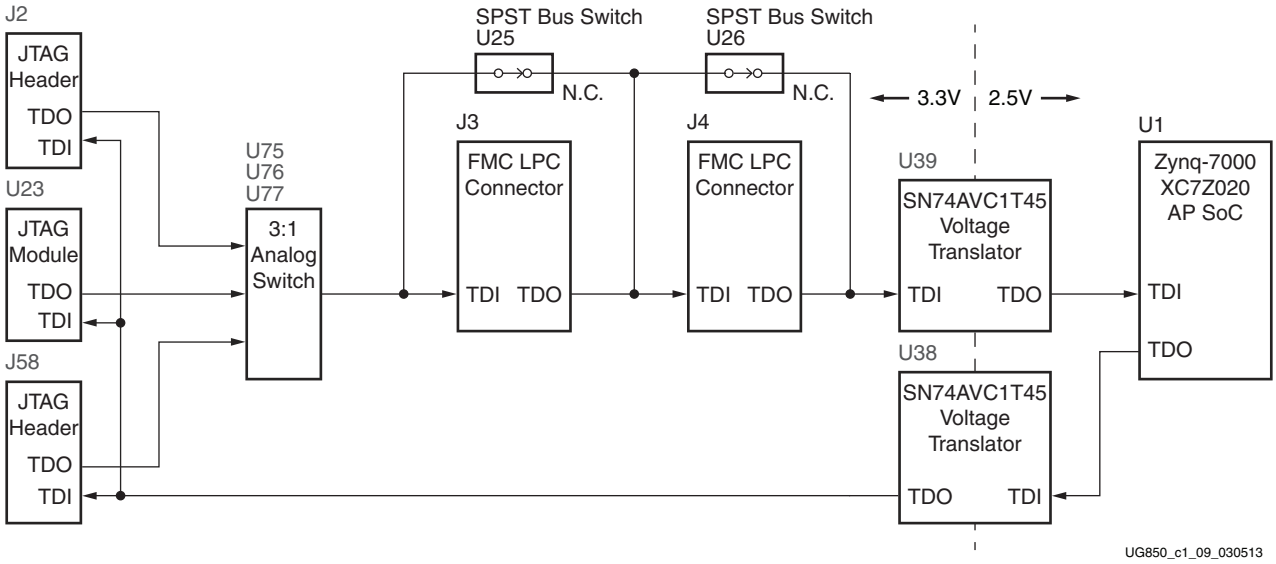


Figure 1-9: **JTAG Chain Block Diagram**

Programmable Logic JTAG Select Switch, JTAG Cable Connector

[Figure 1-2, callout 23]

The JTAG chain can be programmed by three different methods made available via a 3-to-1 analog switch (U75, U76, and U77) controlled by a 2-position DIP switch at SW10.

Figure 1-10 shows the JTAG analog switches and DIP switch SW10.

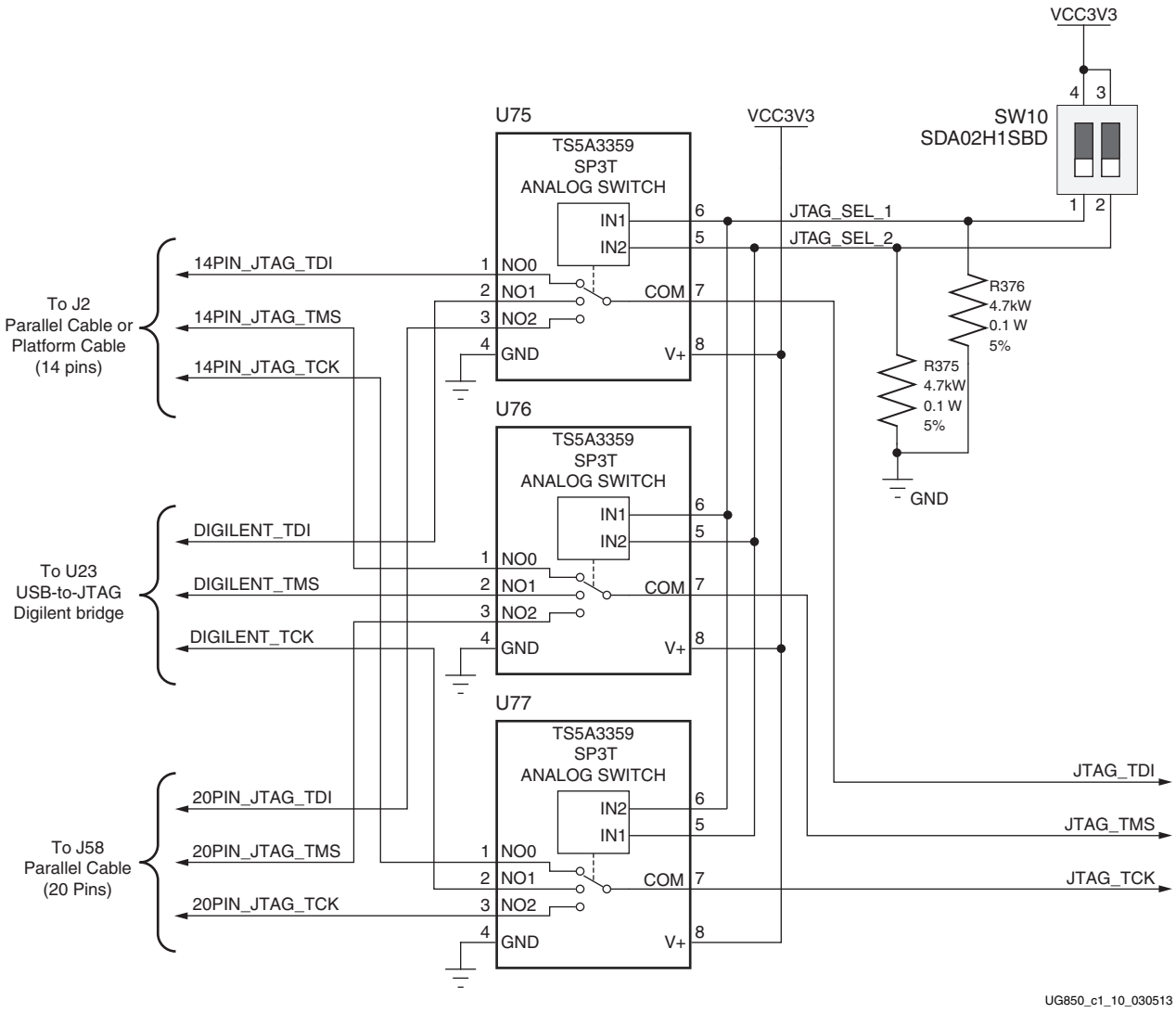


Figure 1-10: **PL JTAG Programming Source Analog Switch**

DIP switch SW10[1:2] setting `01` selects the 14-pin header J2 for configuration using either a Parallel Cable IV (PC4) or Platform Cable USB II. DIP switch SW10 setting `10` selects the USB-to-JTAG Digilent bridge U23 for configuration over a Standard-A to Micro-B USB cable. DIP switch SW10 setting `11` selects the JTAG 20-pin header at J58. The four JTAG signals TDI, TDO, TCK, and TMS would be connected to J58 via flying leads from a JTAG cable. The 3-to-1 analog switch settings are shown in Table 1-10.

Table 1-10: **Switch SW10 JTAG Configuration Option Settings**

Configuration Source	DIP Switch SW10[1:2]	
	Switch 1[(1)] JTAG_SEL_1	Switch 2[(1)] JTAG_SEL_2
None	0	0
Digilent USB-to-JTAG interface U23	1	0
Cable connector J2[(2)]	0	1
JTAG header J58	1	1

Notes:
1. 0 = open, 1 = closed
2. Default switch setting

FMC Connector JTAG Bypass

When an FPGA mezzanine card (FMC) is attached to J3 or J4 it is automatically added to the JTAG chain through electronically controlled single-pole single-throw (SPST) switches U25 and U26. The SPST switches are normally closed and transition to an open state when an FMC is attached. Switch U25 adds an attached FMC to the JTAG chain as determined by the FMC1_HPC_PRSNT_M2C_B signal. Switch U26 adds an attached FMC to the JTAG chain as determined by the FMC2_LPC_PRSNT_M2C_B signal.

Clock Generation

The ZC702 board provides three clock sources for the XC7Z020 AP SoC. Table 1-11 lists the source devices for each clock.

Table 1-11: **ZC702 Board Clock Sources**

Clock Name	Clock Source	Description
System Clock	U43	SiT9102 2.5V LVDS 200 MHz fixed-frequency oscillator (SiTime). See System Clock.
User Clock	U28	Si570 3.3V LVDS I^2C programmable oscillator, 156.250 MHz default (Silicon Labs). See Programmable User Clock.
PS Clock	U65	SIT8103 1.8V single-ended CMOS 33.3333 MHz fixed frequency oscillator (SiTime). See Processing System Clock Source.

Table 1-12 lists the pin-to-pin connections from each clock source to the XC7Z020 AP SoC.

Table 1-12: **Clock Connections, Source to XC7Z020 AP SoC**

Clock Source Pin	Net Name	XC7Z020 (U1) Pin
U43.5	SYSCLK_N	C19
U43.4	SYSCLK_P	D18
U28.5	USRCLK_N	Y8

Table 1-12: **Clock Connections, Source to XC7Z020 AP SoC**

Clock Source Pin	Net Name	XC7Z020 (U1) Pin
U28.4	USRCLK_P	Y9
J65.3	PS_CLK	F7 (Bank 500)

System Clock

[Figure 1-2, callout 7]

The system clock source is an LVDS 200 MHz oscillator at U43. It is wired to a multi-region clock capable (MRCC) input on programmable logic (PL) bank 35. The signal pair is named SYSCLK_P and SYSCLK_N and each signal is connected to U1 pins D18 and C19 respectively on the XC7Z020 AP SoC.

- Oscillator: SiTime SiT9102AI-243N25E200.00000 (200 MHz)
- Frequency jitter: 50 ppm
- Differential Output

For more details, see the SiTime SiT9102 data sheet [Ref 5]. The system clock circuit is shown in Figure 1-11.

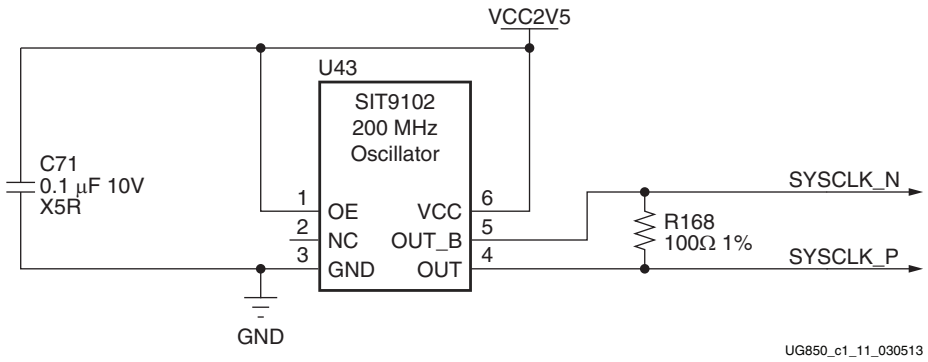


Figure 1-11: **System Clock Source**

Programmable User Clock

[Figure 1-2, callout 8]

The ZC702 board has a programmable low-jitter 3.3V LVDS differential oscillator (U28) connected to the MRCC inputs of bank 13. This USRCLK_P and USRCLK_N clock signal pair is connected to XC7Z020 AP SoC U1 pins Y9 and Y8 respectively. On power-up the user clock defaults to an output frequency of 156.250 MHz. User applications can change the output frequency within the range of 10 MHz to 810 MHz through an I^2C interface. Power cycling the ZC702 board reverts the user clock to the default frequency of 156.250 MHz.

- Programmable Oscillator: Silicon Labs Si570BAB0000544DG (10 MHz–810 MHz)

- LVDS Differential Output

The user clock circuit is shown in Figure 1-12.

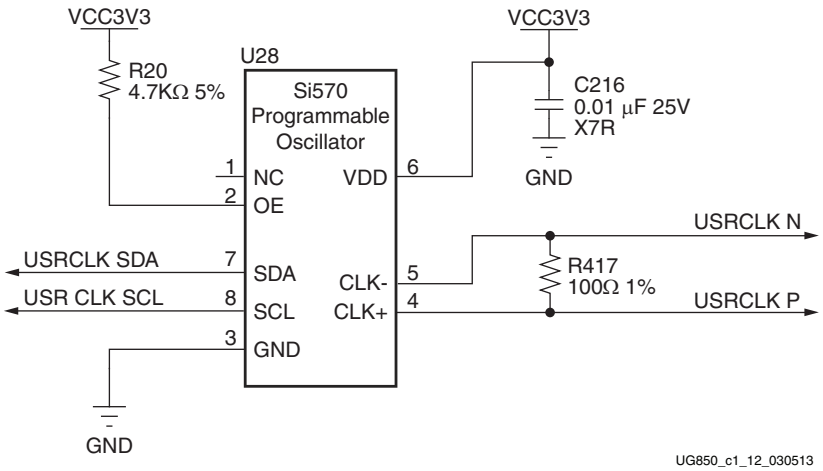


Figure 1-12: **User Clock Source**

The Silicon Labs Si570 data sheet is available on the Silicon Labs website [Ref 6].

Processing System Clock Source

[Figure 1-2, callout 8]

The Processing System (PS) clock source is a 1.8V LVCMOS single-ended fixed 33.33333 MHz oscillator at U65. It is wired to PS bank 500, pin F7 (PS_CLK), on the XC7Z020 AP SoC.

- Oscillator: SiTime SiT8103AC-23-18E-33.33333 (33.3 MHz)
- Frequency jitter: 50 ppm
- Single-ended output

For more details, see the SiTime SiT8103 data sheet [Ref 5].

The system clock circuit is shown in Figure 1-13.

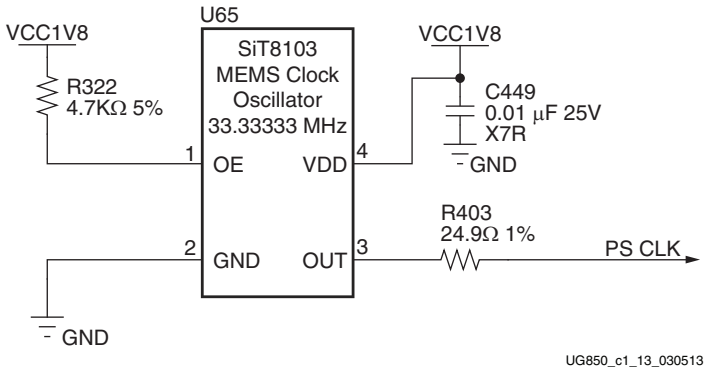


Figure 1-13: **Processing System Clock Source**

10/100/1,000 MHz Tri-Speed Ethernet PHY

[Figure 1-2, callout 9]

The ZC702 board uses the Marvell Alaska PHY device (88E1116R) at U35 for Ethernet communications at 10 Mb/s, 100 Mb/s, or 1,000 Mb/s. The board supports RGMII mode only. The PHY connection to a user-provided Ethernet cable is through a Halo HFJ11-1G01E RJ-45 connector (P2) with built-in magnetics.

On power-up, or on reset, the PHY is configured to operate in RGMII mode with PHY address `0b00111` using the settings shown in Table 1-13. These settings can be overwritten via software commands passed over the MDIO interface.

Table 1-13: **Board Connections for PHY Configuration Pins**

U35 Pin	Setting	Configuration	
CONFIG0	VCCO_MIO1	PHYAD[1]=1	PHYAD[0]=1
CONFIG1	EPHY_LED0	PHYAD[3]=0	PHYAD[2]=1
CONFIG2	GND	ENA_XC=0	PHYAD[4]=0
	EPHY_LED0	ENA_XC=0	PHYAD[4]=1
	VCCO_MIO1	ENA_XC=1	PHYAD[4]=1
CONFIG3	GND	RGMII_TX=0	RGMII_RX=0
	EPHY_LED0	RGMII_TX=0	RGMII_RX=1
	EPHY_LED1	RGMII_TX=1	RGMII_RX=0
	VCCO_MIO1	RGMII_TX=1	RGMII_RX=1

The Ethernet connections from the XC7Z020 AP SoC at U1 to the 88E1116R PHY device at U35 are listed in Table 1-14.

Table 1-14: **Ethernet Connections, XC7Z020 AP SoC to the PHY Device**

XC7Z020 (U1) Pin			Schematic Net Name	M88E1116R PHY U35	
Pin Name	Bank	Pin Number		Pin	Name
PS_MIO53	501	C12	PHY_MDIO	45	MDIO
PS_MIO52	501	D10	PHY_MDC	48	MDC
PS_MIO16	501	D6	PHY_TX_CLK	60	TX_CLK
PS_MIO21	501	F11	PHY_TX_CTRL	63	TX_CTRL
PS_MIO20	501	A8	PHY_TXD3	62	TXD3
PS_MIO19	501	E10	PHY_TXD2	61	TXD2
PS_MIO18	501	A7	PHY_TXD1	59	TXD1
PS_MIO17	501	E9	PHY_TXD0	58	TXD0
PS_MIO22	501	A14	PHY_RX_CLK	53	RX_CLK
PS_MIO27	501	D7	PHY_RX_CTRL	49	RX_CTRL
PS_MIO26	501	A13	PHY_RXD3	55	RXD3
PS_MIO25	501	F12	PHY_RXD2	54	RXD2
PS_MIO24	501	B7	PHY_RXD1	51	RXD1
PS_MIO23	501	E11	PHY_RXD0	50	RXD0

Ethernet PHY Clock Source

[Figure 1-2, callout 10]

A 25.00 MHz 50 ppm crystal at X1 is the clock source for the 88E1116R PHY at U35. Figure 1-14 shows the clock source.

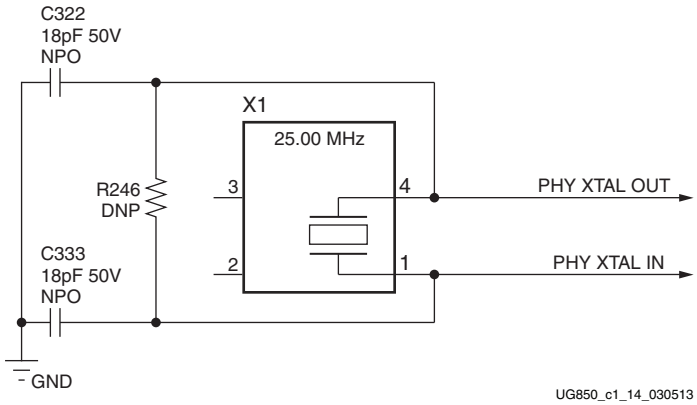


Figure 1-14: **Ethernet PHY Clock Source**

The data sheet can be obtained under NDA with Marvell. The Marvell site includes contact information [Ref 7],

USB-to-UART Bridge

[Figure 1-2, callout 12]

The ZC702 board contains a Silicon Labs CP2103GM USB-to-UART bridge device (U36) which allows a connection to a host computer with a USB port. The USB cable is supplied in the ZC702 Evaluation Kit (Standard-A end to host computer, Type Mini-B end to ZC702 board connector J17). The CP2103GM is powered by the USB 5V provided by the host PC when the USB cable is plugged into the USB port on the ZC702 board.

The CP2013GM TX and RX pins are wired to the UART_1 IP block within the XC7Z020 AP SoC PS I/O Peripherals set. The XC7Z020 AP SoC supports the USB-to-UART bridge using two signal pins: Transmit (TX) and Receive (RX).

Silicon Labs provides royalty-free Virtual COM Port (VCP) drivers for the host computer. These drivers permit the CP2103GM USB-to-UART bridge to appear as a COM port to communications application software (for example, TeraTerm or HyperTerm) that runs on the host computer. The VCP device drivers must be installed on the host PC prior to establishing communications with the ZC702 board.

The USB Connector pin assignments and signal definitions between J17 and U36 are listed in Table 1-15.

Table 1-15: **USB Connector J17 Pin Assignments and Signal Definitions**

USB Connector (J17)		Net Name	Description	CP2103GM (U36)	
Pin	Name			Pin	Name
1	VBUS	USB_UART_VBUS	+5V VBUS Powered	7	REGIN
				8	VBUS
2	D_N	USB_UART_D_N	Bidirectional differential serial data (N-side)	4	D –
3	D_P	USB_UART_D_P	Bidirectional differential serial data (P-side)	3	D +
5	GND	USB_UART_GND	Signal ground	2	GND1
				29	CNR_GND

Table 1-16 lists the USB connections between the XC7Z020 AP SoC PS Bank 501 and the CP2103 UART bridge.

Table 1-16: **XC7Z020 AP SoC to CP2103 Connections**

XC7Z020 AP SoC (U1)			UART Function	Net Name	CP2103GM (U36)	
Pin Name	Bank	Pin Number			Pin	UART Function
PS_MIO48	501	D11	TX, data out	USB_UART_RX	24	RXD, data in
PS_MIO49	501	C14	RX, data in	USB_UART_TX	25	TXD, data out

Refer to the Silicon Labs website for technical information on the CP2103GM and the VCP drivers [Ref 6].

HDMI Video Output

[Figure 1-2, callout 13]

The ZC702 board provides a high-definition multimedia interface (HDMI®) video output using an Analog Devices ADV7511KSTZ-P HDMI transmitter at U40. The HDMI output is provided on a Molex 500254-1927 HDMI type-A receptacle at P1. The ADV7511 supports 1080P 60Hz, YCbCr 4:2:2 encoding via 16-bit input data mapping.

The ZC702 board supports the following HDMI device interfaces:

- 16 data lines
- Independent VSYNC, HSYNC
- Single-ended input CLK
- Interrupt Out pin to XC7Z020 AP SoC
- I^2C
- SPDIF

Figure 1-15 shows the HDMI codec circuit.

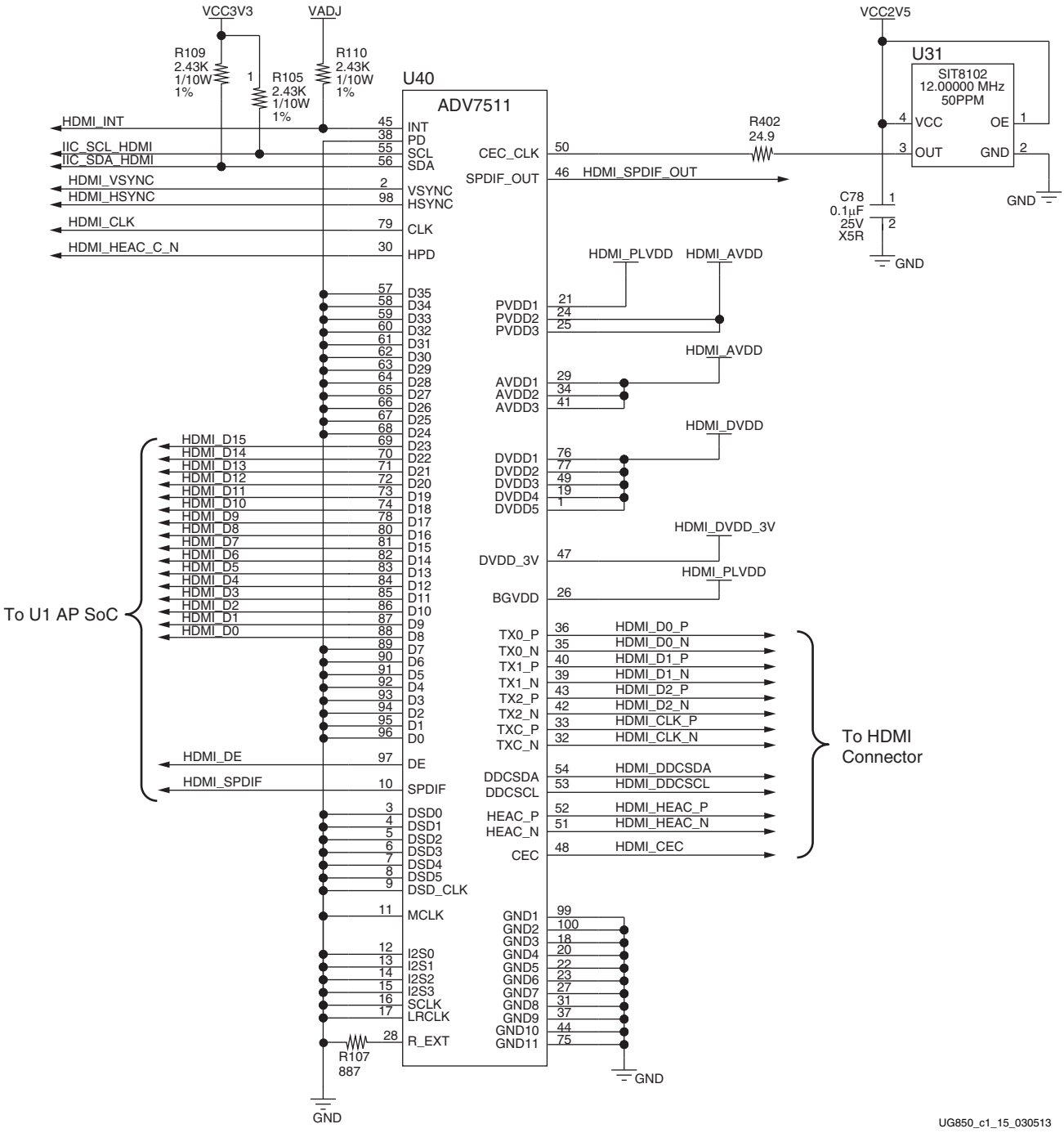


Figure 1-15: **HDMI Codec Circuit**

Table 1-17 lists the connections between the codec and the XC7Z020 AP SoC.

Table 1-17: **XC7Z020 AP SoC to HDMI Codec Connections (ADV7511)**

XC7Z020 (U1) Pin	Net Name	ADV7511 (U40)	
		Pin	Name
AB21	HDMI_D0	88	D8
AA21	HDMI_D1	87	D9
AB22	HDMI_D2	86	D10
AA22	HDMI_D3	85	D11
V19	HDMI_D4	84	D12
V18	HDMI_D5	83	D13
V20	HDMI_D6	82	D14
U20	HDMI_D7	81	D15
W21	HDMI_D8	80	D16
W20	HDMI_D9	78	D17
W18	HDMI_D10	74	D18
T19	HDMI_D11	73	D19
U19	HDMI_D12	72	D20
R19	HDMI_D13	71	D21
T17	HDMI_D14	70	D22
T16	HDMI_D15	69	D23
T18	HDMI_DE	97	DE
R15	HDMI_SPDIF	10	SPDIF
L16	HDMI_CLK	79	CLK
H15	HDMI_VSYNC	2	VSYNC
R18	HDMI_HSYNC	98	HSYNC
U14	HDMI_INT	45	INT
H20	HDMI_SPDIF_OUT	46	SPDIF_OUT

Table 1-18 lists the connections between the codec and the HDMI receptacle P1.

Table 1-18: **ADV7511 to HDMI Receptacle Connections**

ADV7511 (U40)	Net Name	HDMI Receptacle P1 Pin
36	HDMI_D0_P	7
35	HDMI_D0_N	9
40	HDMI_D1_P	4
39	HDMI_D1_N	6
43	HDMI_D2_P	1
42	HDMI_D2_N	3

Table 1-18: **ADV7511 to HDMI Receptacle Connections *(Cont'd)***

ADV7511 (U40)	Net Name	HDMI Receptacle P1 Pin
33	HDMI_CLK_P	10
32	HDMI_CLK_N	12
54	HDMI_DDCSDA	16
53	HDMI_DDCSCL	15
52	HDMI_HEAC_P	14
51	HDMI_HEAC_N	19
48	HDMI_CEC	13

Information about the ADV7511KSTZ-P is available on the Analog Devices website [Ref 8].

I2C Bus

[Figure 1-2, callout 14]

The ZC702 board implements a single I^{2}C port on the XC7Z020 AP SoC (IIC_SDA_MAIN, IIC_SDA_SCL), which is routed through an TI Semiconductor PCA9548 1-to-8 channel I^{2}C bus switch (U44). The bus switch can operate at speeds up to 400 kHz.

The bus switch I^{2}C address is `0x74` (`0b01110100`) and must be addressed and configured to select the desired downstream device.

The ZC702 board I^{2}C bus topology is shown in Figure 1-16.

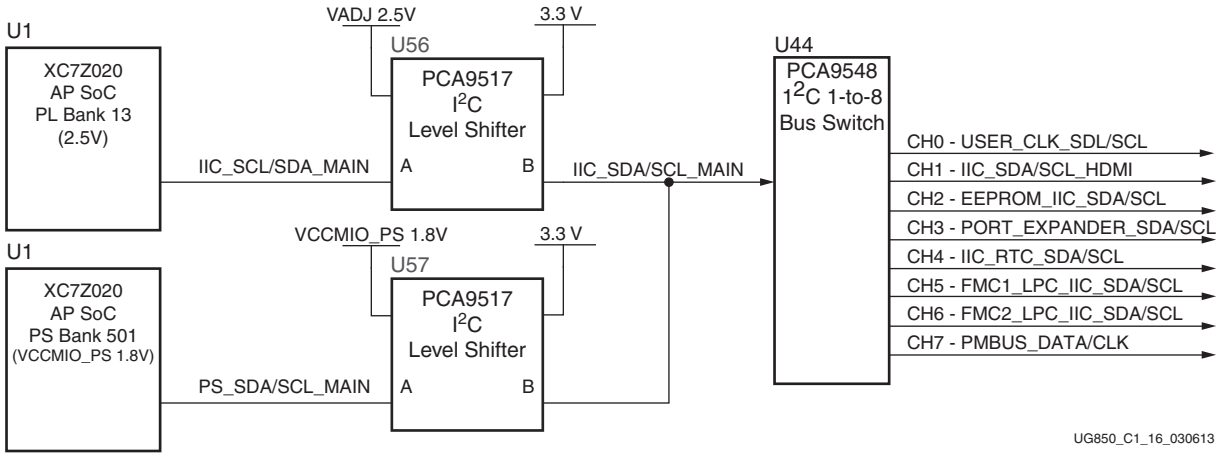


Figure 1-16: **I^{2}C Bus Topology**

User applications that communicate with devices on one of the downstream I^{2}C buses must first set up a path to the desired bus through the U44 bus switch at I^{2}C address `0x74` (`0b01110100`). Table 1-19 lists the address for each bus.

Table 1-19: **I²C Bus Addresses**

I²C Bus	I²C Switch Position	I²C Address
PCA9548 8-Channel bus switch	NA	0b1110100
USRCLK_SDA/SCL	0	0b1011101
IIC_SDA_HDMI	1	0b0111001
IIC_EEPROM_SDA/SCL	2	0b1010100
IIC_PORT_EXPANDER_SDA/SCL	3	0b0100001
IIC_RTC_SDA/SCL	4	0b1010001
FMC1_LPC_IIC_SDA/SCL	5	0bxxxxx00
FMC2_LPC_IIC_SDA/SCL	6	0bxxxxx00
PMBUS_DATA/CLOCK	7	0b1010[ADDR](1)

Notes:

1. This I²C address is the binary equivalent of the TI Power Controller PMBus address 52, 53, or 54 which corresponds to 010, 011 and 100 in the lower 3 bits.

Information about the PCA9548 is available on the TI Semiconductor website at [Ref 12].

Real Time Clock

[Figure 1-2, callout 15]

The Epson RTC-8564JE is an 1²C bus interface real-time clock that has a built-in 32.768 KHz oscillator with these features

- Frequency output options: 32.768 KHz, 1024 Hz, 32 Hz or 1 Hz
- Calendar output functions: Year, month, day, weekday, hour, minute and second
- Clock counter, alarm and fixed-cycle timer interrupt functions

Programming information for the RTC-8564JE is available in the *RTC-8564JE/NB Application Manual* at the Epson Electronics America website [Ref 9].

Figure 1-17 shows the real time clock circuit.

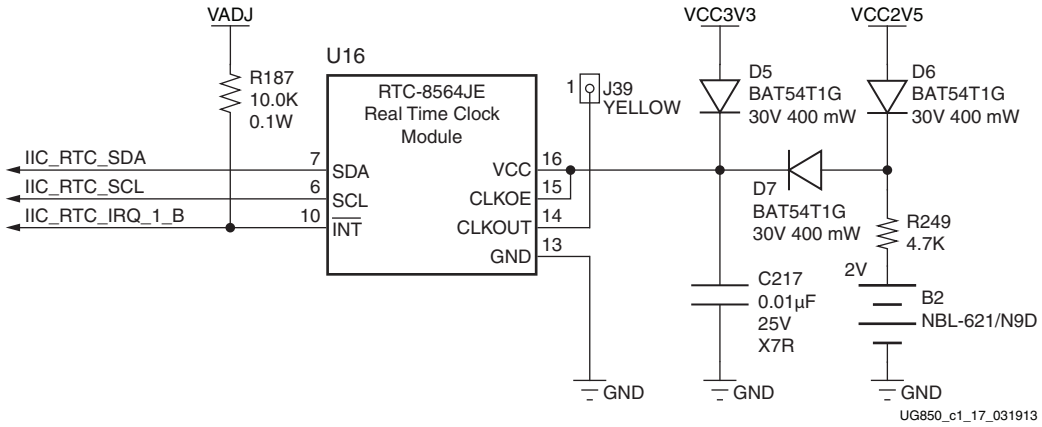


Figure 1-17: **Real Time Clock Circuit**

Real time clock connections to the XC7Z020 AP SoC and the PCA9548 8-Channel bus switch are listed in Table 1-20.

Table 1-20: **Real Time Clock Connections**

RTC-8564JE (U16) Pin	Net Name	Connects To
6	IIC_RTC_SCL	U44.11 (PCA9548 SC4)
7	IIC_RTC_SDA	U44.10 (PCA9548 SD4)
10	IIC_RTC_IRQ_1_B	U1.U7 (XC7Z020 AP SoC PL BANK 13)

Information about the RTC-8564JE is available at the Epson Electronics America website [Ref 9].

I/O Expansion Header

[Figure 1-2, callout 16]

The 2 x 6 I/O expansion header J54 supports Digilent Pmod Peripheral Modules. 8 pins (IIC_PMOD[0:7]) are connected to the TI TCA6416APWR I^2C expansion port device U80. See the Digilent website for information on Digilent Pmod Peripheral Modules [Ref 10].

The expansion header circuit is shown in Figure 1-18.

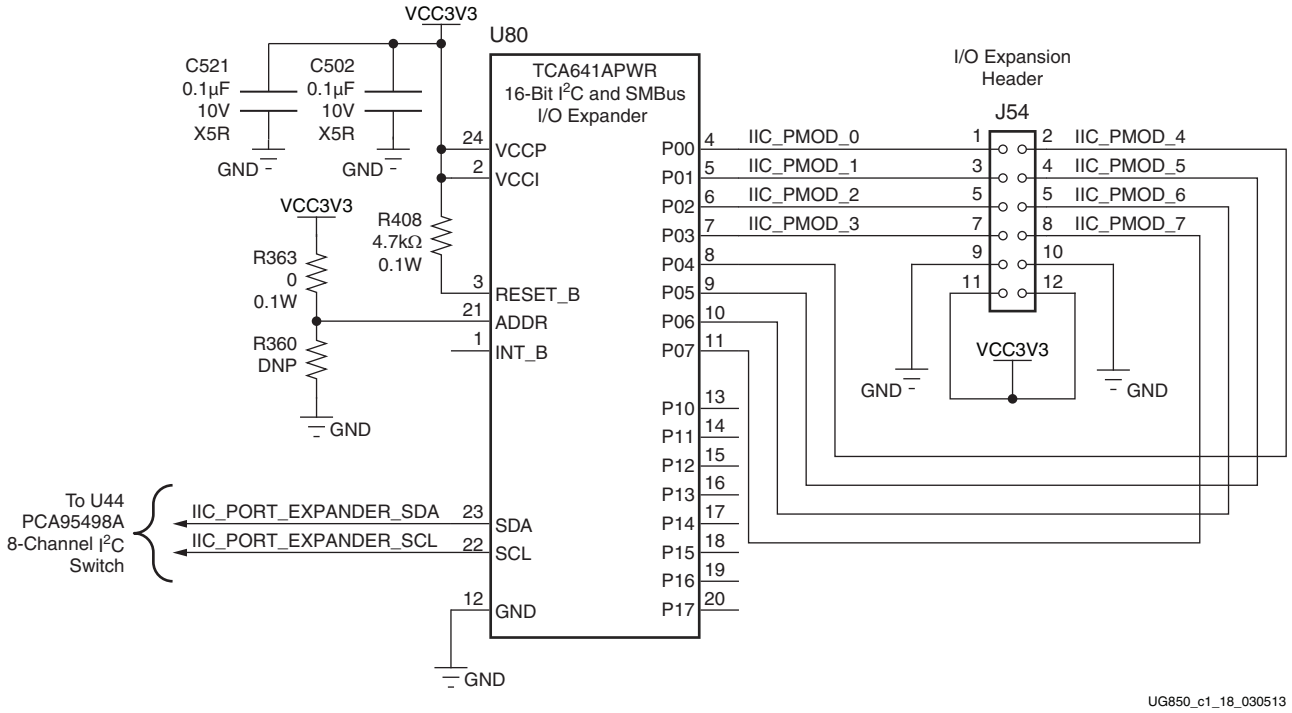


Figure 1-18: **I/O Expansion Header Circuit**

Information about the TCA641APWR is available at the Texas Instruments website [Ref 12].

High Speed CAN Transceiver

[Figure 1-2, callout 21]

The TJA1040 (U14) is an advanced high speed Controller Area Network (CAN) transceiver for use in automotive and general industrial applications. It supports the differential bus signal representation described in the international standard for in-vehicle high speed CAN applications (ISO 11898).

Figure 1-19 shows the controller area network (CAN) bus interface.

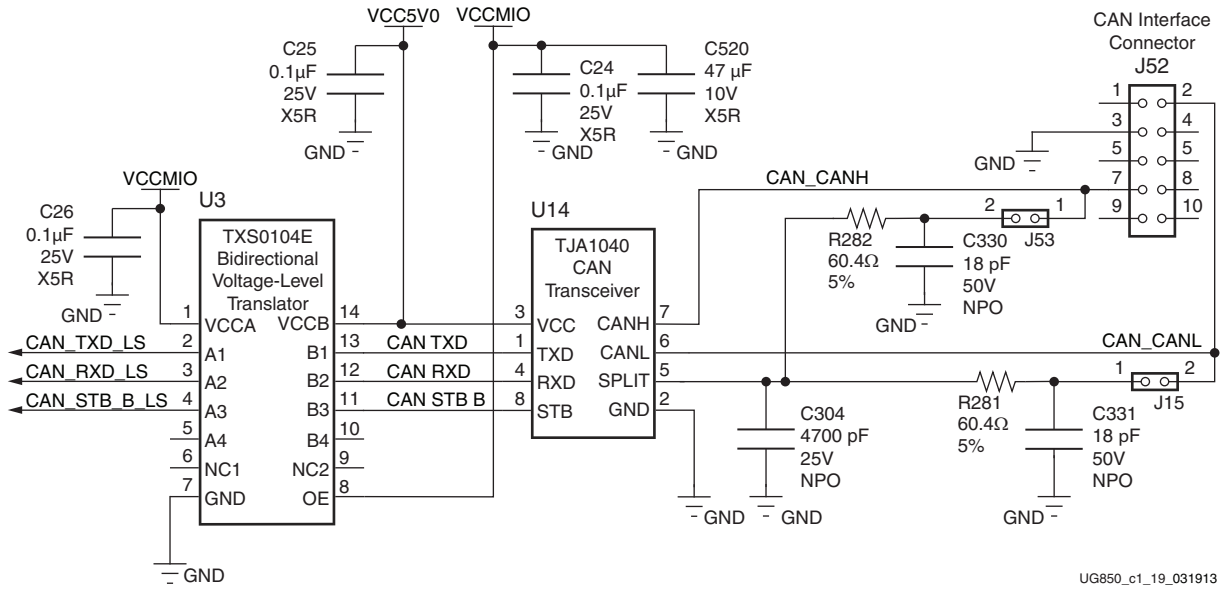


Figure 1-19: **CAN Bus Interface**

Information about the TXS0104E is available at the Texas Instruments website [Ref 12]. Data sheets and application notes for the TJA01040 CAN transceiver are available at the NXP Semiconductors website [Ref 11].

Table 1-21: **CAN Transceiver AP SoC Connections**

TJA1040 (U14)		TXS0104E Level Shifter (U3)	XC7Z020 AP SoC (U1)		
Pin	Net Name	Net Name	Low Side Net	Bank	Pin
1	CAN_TXD	CAN_TXD_LS	PS_MIO47	501	B10
4	CAN_RXD	CAN_RXD_LS	PS_MIO46	501	D12
8	CAN_STB_B	CAN_STB_B_LS	PS_MIO9	500	C4

Status LEDs

[Figure 1-2, callout 21]

Table 1-22 defines the status LEDs. For user controlled LEDs see User I/O, page 42.

Table 1-22: **Status LEDs**

Reference Designator	Net Name	LED Color	Description
DS1	POR	Red	Power on reset is active
DS2	FPGA_INIT_B	Green/Red	Green: FPGA initialization was successful
			Red: FPGA initialization is in progress
DS3	DONE	Green	FPGA bit file download is complete
DS4	PWRCTL_VCC1B_FLKT_LINEAR_PG	Green	DDR3 V_{TT} OK
DS5	U13_FLG	Red	USB Power Error
DS6	PHY_LED2	Green	Ethernet PHY (U35) User LED2
DS7	PHY_LED1	Green	Ethernet PHY (U35) User LED1
DS8	PHY_LED0	Green	Ethernet PHY (U35) User LED0
DS14	VCC12_P_IN	Green	$12V_{DC}$ Power ON
DS13	PWRCTL_PWRGOOD	Green	UCD9248 Power Controllers U32, U33, U34 Power Good (board supply voltages $\geq$ minimum operating voltage)
DS24	PWRCTL1_VCC4A_PG	Green	FMC1, FMC2 Power Good

Ethernet PHY User LEDs

[Figure 1-2, callout 11]

The three Ethernet PHY user LEDs shown in Figure 1-20 are located near the RJ45 Ethernet jack P2. The on/off state for each LED is software dependent and has no specific meaning at Ethernet PHY power on.

Refer to the Marvell 88E1116R Alaska Gigabit Ethernet transceiver data sheet for details concerning the use of the Ethernet PHY user LEDs. They are referred in the data sheet as LED0, LED1, and LED2. The data sheet and other product information for the Marvell 88E1116R Alaska Gigabit Ethernet Transceiver is available at the Marvell website [Ref 7].

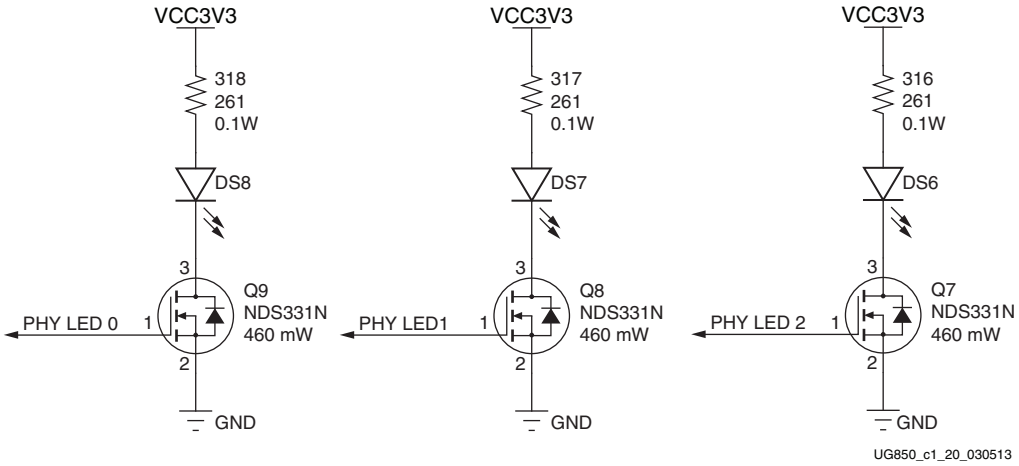


Figure 1-20: **Ethernet PHY User LEDs**

User I/O

[Figure 1-2, callout 17–28]

The ZC702 board provides the following user and general purpose I/O capabilities:

- Ten user LEDs (callout 17)
  - PMOD0 0–PMOD0 3 and PMOD1 0–PMOD1 3: DS15–DS22
  - PS_LED1: DS23 and PS_MIO8_LED0: DS12
- Two user pushbuttons and reset switch (callout 18)
  - GPIO_SW_N and GPIO_SW_S: SW5 and SW7
- 2-position user DIP switch (callout 24)
  - GPIO_DIP_SW1 and GPIO_DIP_SW0: SW12
- User PS switches (near callout 18)
  - Pushbutton SW13 wired in parallel to DIP switch SW15 switch 1
  - Pushbutton SW14 wired in parallel to DIP switch SW15 switch 2
- PS Power-On and System Reset pushbuttons (Switches, page 48)
  - SW1 (PS_POR_B)
  - SW2 (PS_SRST_B)
- Two user GPIO male pin headers (callout 28)
- 2 x 6 0.1 inch pitch PMOD1 J63
- 1 x 6 0.1 inch pitch PMOD2 J62

User LEDs

[Figure 1-2, callout 17]

The ZC702 board supports eight user LEDs connected to XC7Z020 AP SoC Banks 13, 33, 34, and 35 via level-shifters. Note that the LEDs are wired in parallel with headers J63 (PMOD1) and J62 (PMOD2). These headers are described in User PMOD GPIO Headers, page 47.

Figure 1-21 shows the user LED circuits.

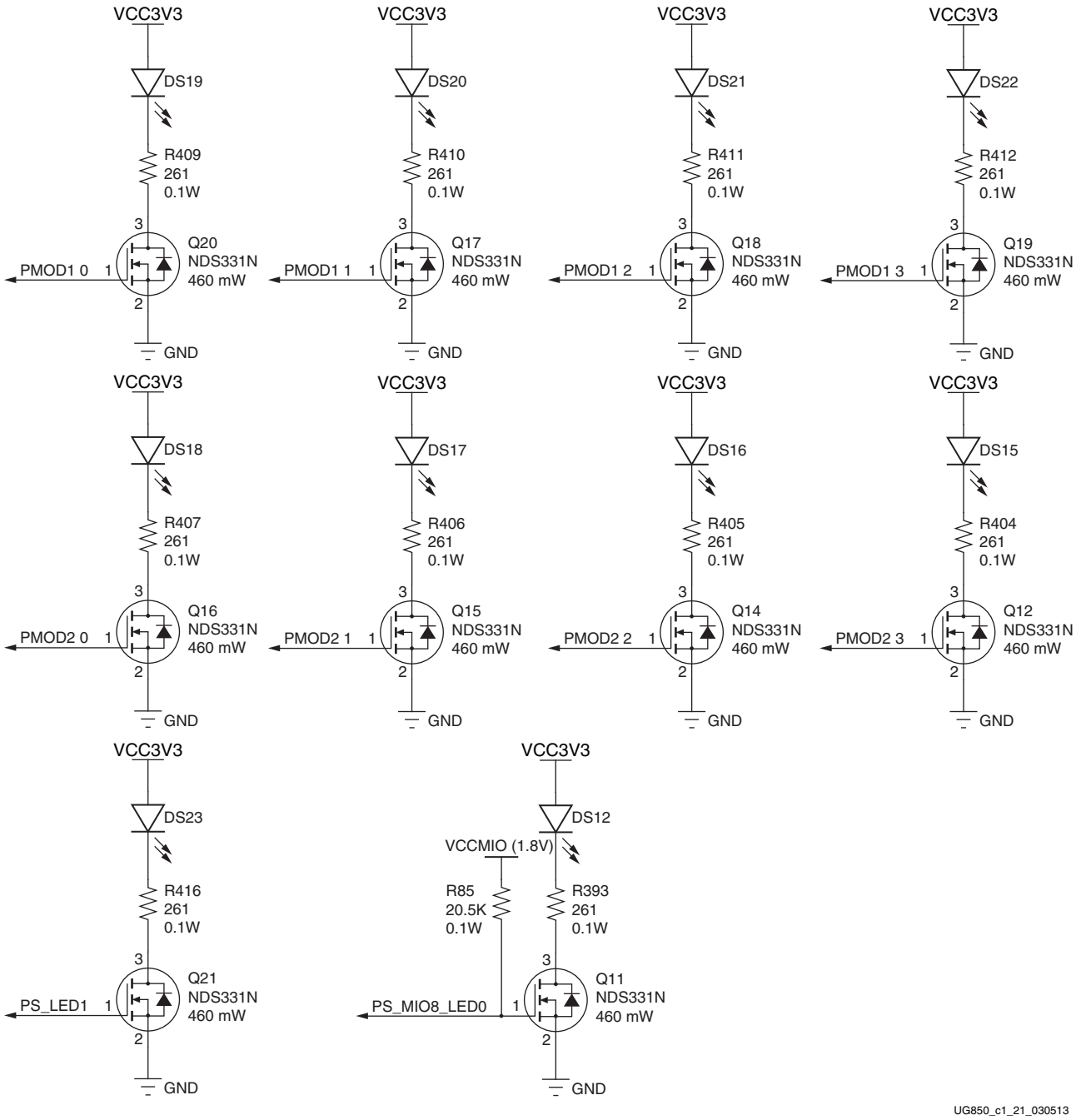


Figure 1-21: **User LEDs**

Table 1-23 lists the user LED connections to XC7Z020 AP SoC U1.

Table 1-23: **User LED Connections to XC7Z020 AP SoC U1**

XC7Z020 AP SoC (U1) Pin	Net Name	LED Reference
E15	PMOD1_0	DS19
D15	PMOD1_1	DS20
W17	PMOD1_2	DS21
W5	PMOD1_3	DS22
V7	PMOD2_0	DS18
W10	PMOD2_1	DS17
P18	PMOD2_2	DS16
P17	PMOD2_3	DS15
G7	PS_LED1	DS23
E5	PS_MIO8_LED0	DS12

User Pushbuttons

[Figure 1-2, callout 18]

Figure 1-22 shows the user pushbutton circuits.

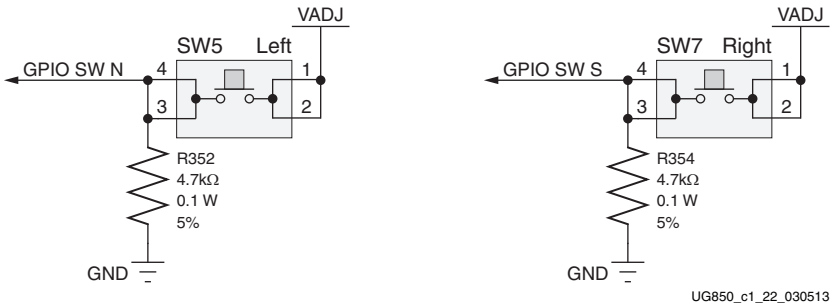


Figure 1-22: **User Pushbuttons**

Table 1-24 lists the user pushbutton connections to XC7Z020 AP SoC U1.

Table 1-24: **User Pushbutton Connections to XC7Z020 AP SoC U1**

XC7Z020 AP SoC (U1) Pin	Net Name	Pushbutton and Pin Reference
G19	GPIO_SW_N	SW5.3 (Left switch)
F19	GPIO_SW_S	SW7.3 (Right switch)

GPIO DIP Switch

[Figure 1-2, callout 19]

Figure 1-23 shows the GPIO DIP switch circuit.

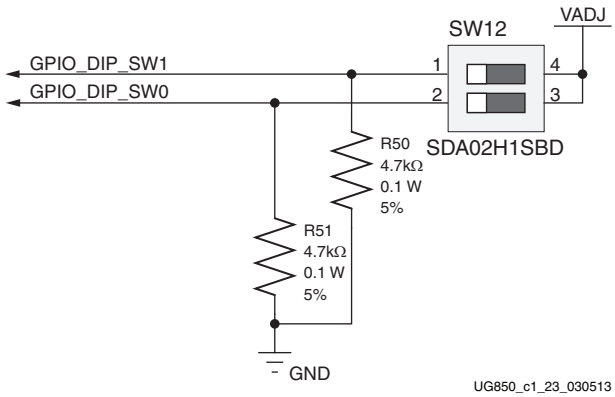


Figure 1-23: **GPIO DIP Switch**

Table 1-25 lists the GPIO DIP switch connections to XC7Z020 AP SoC U1.

Table 1-25: **GPIO DIP Switch Connections to XC7Z020 AP SoC at U1**

XC7Z020 AP SoC (U1) Pin	Net Name	DIP Switch SW12 Pin
W6	GPIO_DIP_SW0	2
W7	GPIO_DIP_SW1	1

User PS Switches

[Figure 1-2, near callout 18]

Figure 1-25 shows the user PS pushbutton and DIP switch circuit.

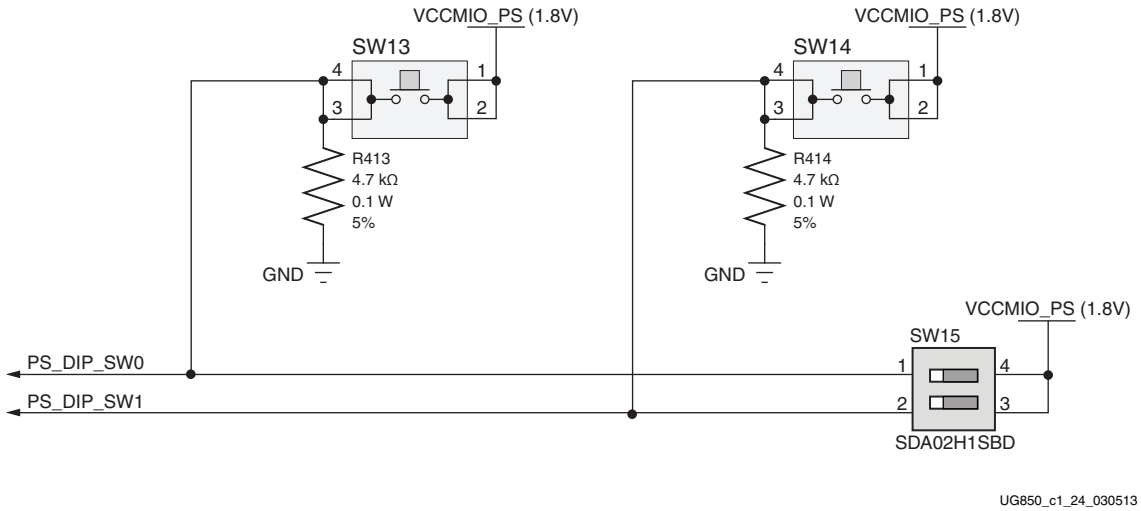


Figure 1-24: **User PS Pushbutton and DIP Switch Circuit**

Table 1-26 lists the user pushbutton connections to XC7Z020 AP SoC U1.

Table 1-26: **User PS Switch Connections to XC7Z020 AP SoC U1**

XC7Z020 AP SoC (U1) Pin	Net Name	Switch and Pin Reference
B6	PS_DIP_SW0	SW13.4 and SW15.1
C5	PS_DIP_SW1	SW14.4 and SW15.2

User PMOD GPIO Headers

[Figure 1-2, callout 28]

The ZC702 board supports two GPIO headers J62 and J63. The PMOD nets connected to these headers are dual-purpose, with the User LEDs, page 43 wired in parallel to the header pins.

J63 has a second dual-purpose function. The even numbered pins are wired in parallel to the ARM PJTAG header J41 pins TDI, TIMS, TCK, and TDO. The J41 PJTAG signals are connected to AP SoC Bank 13 GPIO pins which simultaneously drive J41 and J63. When J41 is used for ARM PJTAG functionality, the J63 even numbered pin should not be used. When J63 even numbered pins are used as GPIO, connector J41 should not be used.

Figure 1-25 shows the user GPIO male pin header circuits.

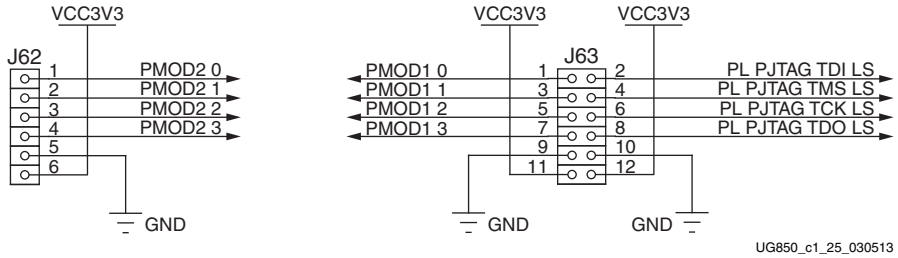


Figure 1-25: **User GPIO Headers**

Table 1-27 lists the GPIO Header connections to XC7Z020 AP SoC U1.

Table 1-27: **GPIO Header Connections to XC7Z020 AP SoC at U1**

XC7Z020 AP SoC (U1) Pin	Net Name	GPIO Header and Pin
E15	PMOD1_0	J63.1
D15	PMOD1_1	J63.3
W17	PMOD1_2	J63.5
W5	PMOD1_3	J63.7
V7	PMOD2_0	J62.1
W10	PMOD2_1	J62.2
P18	PMOD2_2	J62.3
P17	PMOD2_3	J62.4

Refer to UG585, *Zynq-7000 All Programmable SoC Technical Reference Manual* for information about the PS PJTAG functionality.

Switches

[Figure 1-2, callout 22–26]

The ZC702 board includes a power and a configuration switch:

- Power On/Off slide switch SW11 (callout 26)
- SW4 (FPGA_PROG_B), active-Low pushbutton (callout 22)

Power On/Off Slide Switch

[Figure 1-2, callout 20]

The ZC702 board power switch is SW11. Sliding the switch actuator from the Off to On position applies 12V power from J60, a 6-pin mini-fit connector. Green LED DS14 illuminates when the ZC702 board power is on. See Power Management for details on the onboard power system.

CAUTION! *Do NOT plug a PC ATX power supply 6-pin connector into J60 on the ZC702 board. The ATX 6-pin connector has a different pinout than J60. Connecting an ATX 6-pin connector into J60 will damage the ZC702 board and void the board warranty.*

Figure 1-26 shows the power connector J60, power switch SW11 and indicator LED DS14.

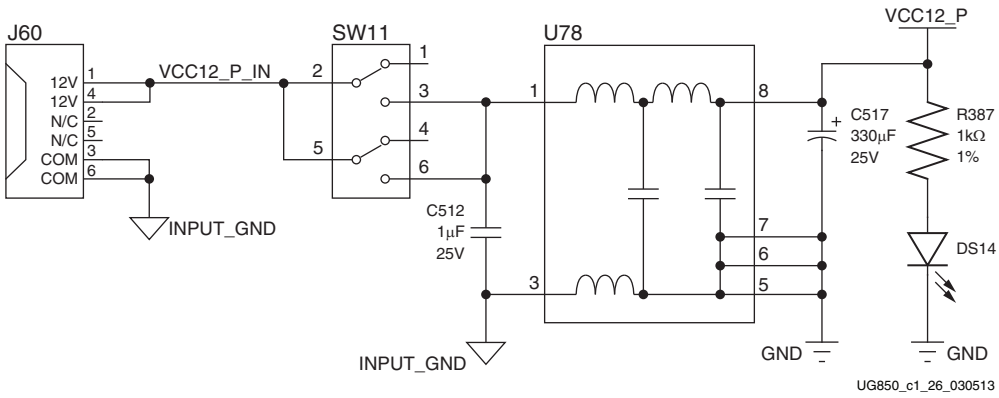


Figure 1-26: **Power On/Off Switch SW11**

Program_B Pushbutton

[Figure 1-2, callout 22]

Switch SW4 grounds the XC7Z020 AP SoC PROG_B pin when pressed. This action clears programmable logic configuration, which the PS software can then act on. The FPGA_PROG_B signal is connected to XC7Z020 AP SoC U1 pin T11.

See UG470, *7 Series FPGAs Configuration User Guide* for further details on configuring the 7 series FPGAs.

Figure 1-27 shows SW4.

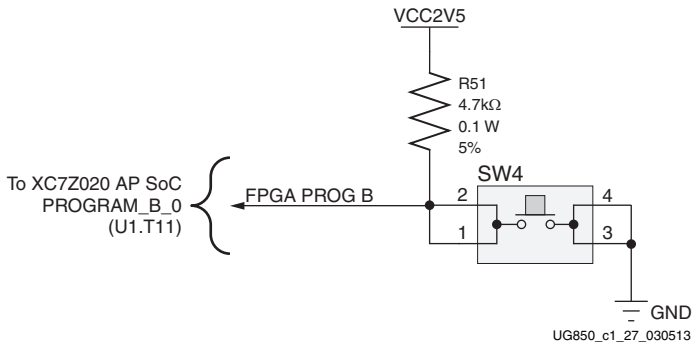


Figure 1-27: **PROG_B Pushbutton SW4**

PS Power-On and System Reset Pushbuttons

[Figure 1-2, callout 27]

Figure 1-28 shows the reset circuitry for the processing system.

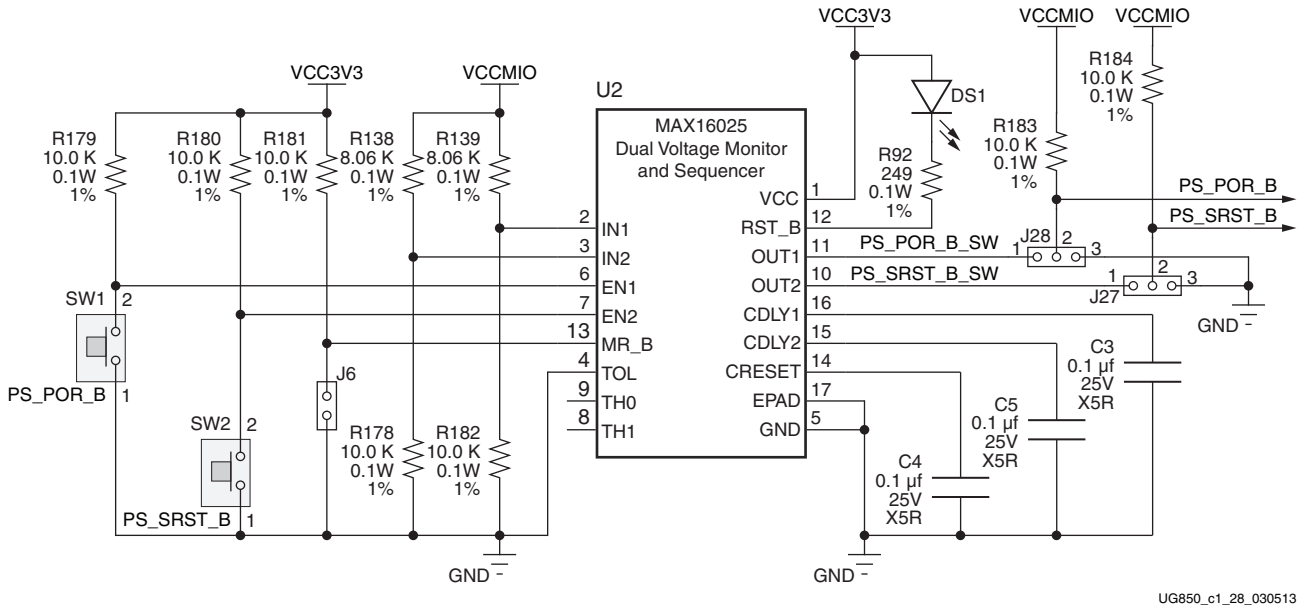


Figure 1-28: **PS Power On and System Reset Circuitry**

Depressing and then releasing pushbutton SW1 causes PS_POR_B_SW to strobe low.

PS_POR_B: This reset is used to hold the PS in reset until all PS power supplies are at the required voltage levels. It must be held Low through PS power-up. PS_POR_B should be generated by the power supply *power-good* signal.

Depressing and then releasing pushbutton SW2 causes PS_SRST_B_SW to strobe low.

PS_SRST_B: This reset is used to force a system reset. It can be tied or pulled High, and can be High during the PS supply power ramps.

Refer to UG585, *Zynq-7000 All Programmable SoC Technical Reference Manual* for information concerning the resets.

FPGA Mezzanine (FMC) Card Interface

[Figure 1-2, callout 24]

The ZC702 board supports the VITA 57.1 FPGA Mezzanine Card (FMC) specification by providing subset implementations of low pin count (LPC) connectors at J3 and J4. Both connectors use a 10 x 40 form factor that is partially populated with 160 pins. The connectors are keyed so that a the mezzanine card faces away from the ZC702 board when connected.

Signaling Speed Ratings:

- Single-ended: 9 GHz (18 Gb/s)
- Differential Optimal Vertical: 9 GHz (18 Gb/s)
- Differential Optimal Horizontal: 16 GHz (32 Gb/s)
- High Density Vertical: 7 GHz (15 Gb/s)

The Samtec connector system is rated for signaling speeds up to 9 GHz (18 Gb/s) based on a –3 dB insertion loss point within a two-level signaling environment.

Connector Type:

- Samtec SEAF Series, 1.27 mm (0.050 in) pitch. Mates with SEAM series connector

For more information about SEAF series connectors, go to the Samtec website [Ref 13].

LPC Connectors J3 and J4

[Figure 1-2, callout 24]

The 160-pin LPC connector defined by the FMC specification (Figure B-1, page 65) provides connectivity for up to:

- 68 single-ended or 34 differential user-defined signals (34 LA pairs, LA00–LA33)
- 1 GTX transceiver
- 1 GTX clock
- 2 differential clocks
- 61 ground and 10 power connections

The LPC connections between FMC1 (J3) and XC7Z020 AP SoC U1 (Table 1-28) and between FMC2 (J4) and XC7Z020 AP SoC U1 (Table 1-29) both implement a subset of this connectivity:

- 68 single-ended or 34 differential user-defined signals (34 LA pairs, LA00–LA33)
- 0 GTX transceivers
- 0 GTX clocks
- 2 differential clocks
- 61 ground and 9 power connections

Table 1-28 shows the LPC connections between J3 and XC7Z020 AP SoC U1.

Table 1-28: **LPC Connections, FMC1 (J3) to XC7Z020 AP SoC U1**

FMC1 J3 Pin	Net Name	XC7Z020 (U1) Pin	J3 Pin	Net Name	XC7Z020 (U1) Pin
C2	NC		D1	PWRCTL1_VCC4A_PG	
C3	NC		D4	NC	
C6	NC		D5	NC	
C7	NC		D8	FMC1_LPC_LA01_CC_P	N19
C10	FMC1_LPC_LA06_P	J18	D9	FMC1_LPC_LA01_CC_N	N20
C11	FMC1_LPC_LA06_N	K18	D11	FMC1_LPC_LA05_P	N17
C14	FMC1_LPC_LA10_P	L17	D12	FMC1_LPC_LA05_N	N18
C15	FMC1_LPC_LA10_N	M17	D14	FMC1_LPC_LA09_P	M15
C18	FMC1_LPC_LA14_P	J16	D15	FMC1_LPC_LA09_N	M16
C19	FMC1_LPC_LA14_N	J17	D17	FMC1_LPC_LA13_P	P16
C22	FMC1_LPC_LA18_CC_P	D20	D18	FMC1_LPC_LA13_N	R16
C23	FMC1_LPC_LA18_CC_N	C20	D20	FMC1_LPC_LA17_CC_P	B19
C26	FMC1_LPC_LA27_P	C17	D21	FMC1_LPC_LA17_CC_N	B20
C27	FMC1_LPC_LA27_N	C18	D23	FMC1_LPC_LA23_P	G15
C30	FMC1_LPC_IIC_SCL		D24	FMC1_LPC_LA23_N	G16
C31	FMC1_LPC_IIC_SDA		D26	FMC1_LPC_LA26_P	F18
C34	GND		D27	FMC1_LPC_LA26_N	E18
C35	VCC12_P		D29	FMC1_LPC_TCK_BUF	
C37	VCC12_P		D30	FMC_TDI_BUF	
C39	VCC3V3		D31	FMC1_LPC_TDO_FMC2_LPC_TDI	
			D32	VCC3V3	
			D33	FMC1_LPC_TMS_BUF	
			D34	NC	

Table 1-28: **LPC Connections, FMC1 (J3) to XC7Z020 AP SoC U1 *(Cont'd)***

FMC1 J3 Pin	Net Name	XC7Z020 (U1) Pin	J3 Pin	Net Name	XC7Z020 (U1) Pin
			D35	GND	
			D36	VCC3V3	
			D38	VCC3V3	
			D40	VCC3V3	
G2	FMC1_LPC_CLK1_M2C_P	M19	H1	NC	
G3	FMC1_LPC_CLK1_M2C_N	M20	H2	FMC1_LPC_PRSNT_M2C_B	
G6	FMC1_LPC_LA00_CC_P	K19	H4	FMC1_LPC_CLK0_M2C_P	L18
G7	FMC1_LPC_LA00_CC_N	K20	H5	FMC1_LPC_CLK0_M2C_N	L19
G9	FMC1_LPC_LA03_P	J20	H7	FMC1_LPC_LA02_P	L21
G10	FMC1_LPC_LA03_N	K21	H8	FMC1_LPC_LA02_N	L22
G12	FMC1_LPC_LA08_P	J21	H10	FMC1_LPC_LA04_P	M21
G13	FMC1_LPC_LA08_N	J22	H11	FMC1_LPC_LA04_N	M22
G15	FMC1_LPC_LA12_P	N22	H13	FMC1_LPC_LA07_P	J15
G16	FMC1_LPC_LA12_N	P22	H14	FMC1_LPC_LA07_N	K15
G18	FMC1_LPC_LA16_P	N15	H16	FMC1_LPC_LA11_P	R20
G19	FMC1_LPC_LA16_N	P15	H17	FMC1_LPC_LA11_N	R21
G21	FMC1_LPC_LA20_P	G20	H19	FMC1_LPC_LA15_P	P20
G22	FMC1_LPC_LA20_N	G21	H20	FMC1_LPC_LA15_N	P21
G24	FMC1_LPC_LA22_P	G17	H22	FMC1_LPC_LA19_P	E19
G25	FMC1_LPC_LA22_N	F17	H23	FMC1_LPC_LA19_N	E20
G27	FMC1_LPC_LA25_P	C15	H25	FMC1_LPC_LA21_P	F21
G28	FMC1_LPC_LA25_N	B15	H26	FMC1_LPC_LA21_N	F22
G30	FMC1_LPC_LA29_P	B16	H28	FMC1_LPC_LA24_P	A21
G31	FMC1_LPC_LA29_N	B17	H29	FMC1_LPC_LA24_N	A22
G33	FMC1_LPC_LA31_P	A16	H31	FMC1_LPC_LA28_P	D22
G34	FMC1_LPC_LA31_N	A17	H32	FMC1_LPC_LA28_N	C22
G36	FMC1_LPC_LA33_P	A18	H34	FMC1_LPC_LA30_P	E21
G37	FMC1_LPC_LA33_N	A19	H35	FMC1_LPC_LA30_N	D21
G39	VADJ		H37	FMC1_LPC_LA32_P	B21
			H38	FMC1_LPC_LA32_N	B22
			H40	VADJ	

Table 1-29 shows the LPC connections between FMC2 (J4) and AP SoC U1.

Table 1-29: **LPC Connections, FMC2 (J4) to AP SoC U1**

FMC2 J4 Pin	Net Name	XC7Z020 (U1) Pin	J4 Pin	Net Name	XC7Z020 (U1) Pin
C2	NC		D1	PWRCTL1_VCC4A_PG	
C3	NC		D4	NC	
C6	NC		D5	NC	
C7	NC		D8	FMC2_LPC_LA01_CC_P	W16
C10	FMC2_LPC_LA06_P	U17	D9	FMC2_LPC_LA01_CC_N	Y16
C11	FMC2_LPC_LA06_N	V17	D11	FMC2_LPC_LA05_P	AB19
C14	FMC2_LPC_LA10_P	Y20	D12	FMC2_LPC_LA05_N	AB20
C15	FMC2_LPC_LA10_N	Y21	D14	FMC2_LPC_LA09_P	U15
C18	FMC2_LPC_LA14_P	T22	D15	FMC2_LPC_LA09_N	U16
C19	FMC2_LPC_LA14_N	U22	D17	FMC2_LPC_LA13_P	V22
C22	FMC2_LPC_LA18_CC_P	AA9	D18	FMC2_LPC_LA13_N	W22
C23	FMC2_LPC_LA18_CC_N	AA8	D20	FMC2_LPC_LA17_CC_P	AA7
C26	FMC2_LPC_LA27_P	AB2	D21	FMC2_LPC_LA17_CC_N	AA6
C27	FMC2_LPC_LA27_N	AB1	D23	FMC2_LPC_LA23_P	V12
C30	FMC2_LPC_IIC_SCL		D24	FMC2_LPC_LA23_N	W12
C31	FMC2_LPC_IIC_SDA		D26	FMC2_LPC_LA26_P	U12
C34	GND		D27	FMC2_LPC_LA26_N	U11
C35	VCC12_P		D29	FMC2_LPC_TCK_BUF	
C37	VCC12_P		D30	FMC1_LPC_TDO_FMC2_LPC_TDI	
C39	VCC3V3		D31	FMC2_LPC_TDO_FPGA_TDI	
			D32	VCC3V3	
			D33	FMC2_LPC_TMS_BUF	
			D34	NC	
			D35	GND	
			D36	VCC3V3	
			D38	VCC3V3	
			D40	VCC3V3	
G2	FMC2_LPC_CLK1_M2C_P		H1	NC	
G3	FMC2_LPC_CLK1_M2C_N		H2	FMC2_LPC_PRSNT_M2C_B	
G6	FMC2_LPC_LA00_CC_P	Y19	H4	FMC2_LPC_CLK0_M2C_P	Y18
G7	FMC2_LPC_LA00_CC_N	AA19	H5	FMC2_LPC_CLK0_M2C_N	AA18
G9	FMC2_LPC_LA03_P	AA16	H7	FMC2_LPC_LA02_P	V14

Table 1-29: **LPC Connections, FMC2 (J4) to AP SoC U1 *(Cont'd)***

FMC2 J4 Pin	Net Name	XC7Z020 (U1) Pin	J4 Pin	Net Name	XC7Z020 (U1) Pin
G10	FMC2_LPC_LA03_N	AB16	H8	FMC2_LPC_LA02_N	V15
G12	FMC2_LPC_LA08_P	AA17	H10	FMC2_LPC_LA04_P	V13
G13	FMC2_LPC_LA08_N	AB17	H11	FMC2_LPC_LA04_N	W13
G15	FMC2_LPC_LA12_P	W15	H13	FMC2_LPC_LA07_P	T21
G16	FMC2_LPC_LA12_N	Y15	H14	FMC2_LPC_LA07_N	U21
G18	FMC2_LPC_LA16_P	AB14	H16	FMC2_LPC_LA11_P	Y14
G19	FMC2_LPC_LA16_N	AB15	H17	FMC2_LPC_LA11_N	AA14
G21	FMC2_LPC_LA20_P	T4	H19	FMC2_LPC_LA15_P	Y13
G22	FMC2_LPC_LA20_N	U4	H20	FMC2_LPC_LA15_N	AA13
G24	FMC2_LPC_LA22_P	U10	H22	FMC2_LPC_LA19_P	R6
G25	FMC2_LPC_LA22_N	U9	H23	FMC2_LPC_LA19_N	T6
G27	FMC2_LPC_LA25_P	AA12	H25	FMC2_LPC_LA21_P	V5
G28	FMC2_LPC_LA25_N	AB12	H26	FMC2_LPC_LA21_N	V4
G30	FMC2_LPC_LA29_P	AA11	H28	FMC2_LPC_LA24_P	U6
G31	FMC2_LPC_LA29_N	AB11	H29	FMC2_LPC_LA24_N	U5
G33	FMC2_LPC_LA31_P	AB10	H31	FMC2_LPC_LA28_P	AB5
G34	FMC2_LPC_LA31_N	AB9	H32	FMC2_LPC_LA28_N	AB4
G36	FMC2_LPC_LA33_P	Y11	H34	FMC2_LPC_LA30_P	AB7
G37	FMC2_LPC_LA33_N	Y10	H35	FMC2_LPC_LA30_N	AB6
G39	VADJ		H37	FMC2_LPC_LA32_P	Y4
			H38	FMC2_LPC_LA32_N	AA4
			H40	VADJ	

Power Management

[Figure 1-2, callout 25]

TheZC702 PCB layout and power system design meets the recommended criteria described in *Zynq-7000 All Programmable SoC PCB Design and Pin Planning Guide* (UG933).

The ZC702 board power distribution diagram is shown in Figure 1-29.

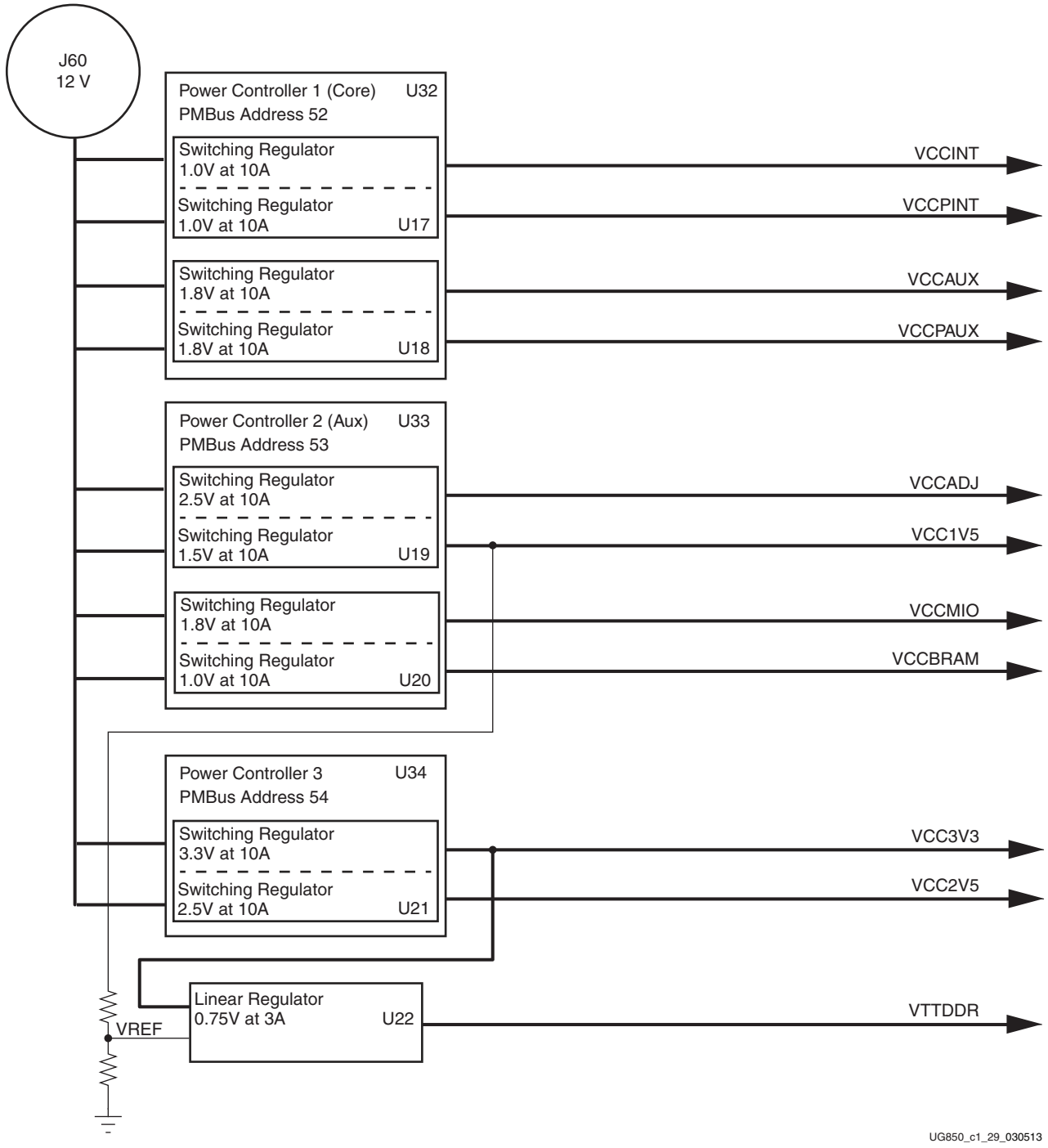


Figure 1-29: **Onboard Power Regulators**

The ZC702 board uses power regulators and a PMBus compliant system controller from Texas Instruments to supply core and auxiliary voltages as listed in Table 1-30. The Texas Instruments Fusion Digital Power graphical user interface is used to monitor the voltage and current levels of the board power modules.

Table 1-30: **Onboard Power System Devices**

Device Type	Reference Designator	Description	Power Rail Net Name	Power Rail Voltage	Schematic Page
Core voltage controller and regulators					
UCD9248PFC	U32	PMBus Controller—Core (Addr = 52)			39
PTD08D210W—VoutA	U17	Dual 10A 0.6V—3.6V Adj. Switching Regulator	VCCINT	1.00V	40
PTD08D210W—VoutB		Dual 10A 0.6V—3.6V Adj. Switching Regulator	VCCPINT	1.00V	40
PTD08D210W—VoutA	U18	Dual 10A 0.6V—3.6V Adj. Switching Regulator	VCCAUX	1.80V	41
PTD08D210W—VoutB		Dual 10A 0.6V—3.6V Adj. Switching Regulator	VCCPAUX	1.80V	41
Auxiliary voltage controller and regulators					
UCD9248PFC	U33	PMBus Controller—Aux (Addr = 53)			42
PTD08D210W—VoutA	U19	Dual 10A 0.6V—3.6V Adj. Switching Regulator (set to 1.8V, 2.5V or 3.3V)	VADJ	2.50V	43
PTD08D210W—VoutB		Dual 10A 0.6V—3.6V Adj. Switching Regulator	VCC1V5	1.50V	43
PTD08D210W—VoutA	U20	Dual 10A 0.6V—3.6V Adj. Switching Regulator	VCCMIO_PS	1.80V	44
PTD08D210W—VoutB		Dual 10A 0.6V—3.6V Adj. Switching Regulator	VCCBRAM	1.00V	44
UCD9248PFC	U34	PMBus Controller—Aux (Addr = 53)			45
PTD08D210W—VoutA	U21	Dual 10A 0.6V—3.6V Adj. Switching Regulator	VCC3V3	3.30V	46
PTD08D210W—VoutB		Dual 10A 0.6V—3.6V Adj. Switching Regulator	VCC2V5/ VCC2V5_PL	2.50V	46
Linear regulator					
TPS51200DR	U22	3A Tracking Regulator	VTTDDR_PS	0.75V	37

VADJ Voltage Control

The VADJ rail is set to 2.5V. When the ZC702 board is powered on, the state of the FMC_VADJ_ON_B signal wired to header J12 is sampled by the TI UCD9248 controller U33. If a jumper is installed on J12 signal FMC_VADJ_ON_B is held low, and the TI controller U33 energizes the VADJ rail at power on.

Because the rail turn on decision is made at power on time based on the presence of the J12 jumper, removing the jumper at J12 after the board is powered up does not affect the 2.5V power delivered to the VADJ rail and it remains on.

A jumper installed at J12 is the default setting.

If a jumper is not installed on J12, signal FMC_VADJ_ON_B is high, and the ZC702 board does not energize the VADJ 2.5V at power on. In this mode the user can control when to turn on VADJ and to what voltage level (1.8V, 2.5V or 3.3V only). With VADJ off, the XC7Z020 AP SoC still configures and has access to the TI controller PMBUS along with the FMC_VADJ_ON_B signal. The combination of these allows the user to develop code to command the VADJ rail to be set to something other than the default setting of 2.5V. Once the new VADJ voltage level has been programmed into TI controller U33, the FMC_VADJ_ON_B signal can be driven low by the user logic and the VADJ rail comes up at the new VADJ voltage level. Installing a jumper at J12 after a ZC702 board powers up in this mode turns on the VADJ rail.

The FMC_VADJ_ON_B signal is sourced by the TCA6416APWR I^2C port expander U80 pin 13 (see Figure 1-18, page 39).

The I^2C port expander IIC_PORT_EXPANDER SDA/SCL bus is wired to the PCA9548ARGER I^2C bus switch (see I2C Bus, page 36).

Documentation describing PMBUS programming for the UCD9248 digital power controller is available at TI page www.ti.com/fusiondocs.

Monitoring Voltage and Current

Voltage and current monitoring and control are available for selected power rails through Texas Instruments' Fusion Digital Power graphical user interface. The three onboard TI power controllers (U32 at address 52, U33 at address 53, and U34 at address 54) are wired to the same PMBus. The PMBus connector, J59, is provided for use with the TI USB Interface Adapter PMBus pod (TI part number EVM USB-TO-GPIO, which can be ordered from the Texas Instruments website www.ti.com/xilinx_usb and associated TI Fusion Digital Power Designer GUI (downloadable from http://www.ti.com/fusion-gui). This is the simplest and most convenient way to monitor the voltage and current values for the power rail listed in Table 1-31, Table 1-32, and Table 1-33.

In each of these the three tables (one per controller), the Power Good (PG) On Threshold is the setpoint at or above which the particular rail is deemed “good”. The PG Off Threshold is the setpoint at or below which the particular rail is no longer deemed “good”. The controller internally OR's these PG conditions together and drives an output PG pin high only if all active rail PG states are “good”. The On and Off Delay and rise and fall times are relative to when the board power on-off slide switch SW12 is turned on and off.

Table 1-31 defines the voltage and current values for each power rail controlled by the UCD9248 PMBus controller at address 52 (U32).

Table 1-31: **Power Rail Specifications for UCD9248 PMBus Controller at Address 52**

Rail Number	Rail Name	Rail Name	Nominal V_{OUT} (V)	PG On Threshold (V)	PG Off Threshold (V)	On Delay (ms)	Rise Time (ms)	Off Delay (ms)	Fall Time (ms)	Shutdown Threshold[1]		
										V_{OUT} Over Fault (V)	I_{OUT} Over Fault (A)	Temp Over Fault (°C)
1	Rail #1	VCCINT	1	0.9	0.85	0	5	10	1	1.15	20	90
2	Rail #2	VCCPINT	1	0.9	0.85	0	5	10	1	1.15	20	90
3	Rail #3	VCCAUX	1.8	1.62	1.53	0	5	5	1	2.07	10.41	90
4	Rail #4	VCCPAUX	1.8	1.62	1.53	0	5	5	1	2.07	10.41	90

Notes:

1. The values defined in these columns are the voltage, current, and temperature thresholds that causes the regulator to shut down if the value is exceeded.

Table 1-32 defines the voltage and current values for each power rail controlled by the UCD9248 PMBus controller at address 53 (U33).

Table 1-32: **Power Rail Specifications for UCD9248 PMBus Controller at Address 53**

Rail Number	Rail Name	Schematic Rail Name	Nominal V_{OUT} (V)	PG On Threshold (V)	PG Off Threshold (V)	On Delay (ms)	Rise Time (ms)	Off Delay (ms)	Fall Time (ms)	Shutdown Threshold[1]		
										V_{OUT} Over Fault (V)	I_{OUT} Over Fault (A)	Temp Over Fault (°C)
1	Rail #1	VADJ	2.5	2.25	2.125	0	5	1	1	2.875	10.41	90
2	Rail #2	VCC1V5	1.5	1.35	1.275	0	5	0	1	1.725	10.41	90
3	Rail #3	VCCMIO_PS	1.8	1.62	1.53	0	5	5	1	2.07	10.41	90
4	Rail #4	VCCBRAM	1	0.9	0.85	0	5	10	1	1.15	20	90

Notes:

1. The values defined in these columns are the voltage, current, and temperature thresholds that causes the regulator to shut down if the value is exceeded.

Table 1-33 defines the voltage and current values for each power rail controlled by the UCD9248 PMBus controller at address 54 (U34).

Table 1-33: **Power Rail Specifications for UCD9248 PMBus Controller at Address 54**

Rail Number	Rail Name	Schematic Rail Name	Nominal V_{OUT} (V)	PG On Threshold (V)	PG Off Threshold (V)	On Delay (ms)	Rise Time (ms)	Off Delay (ms)	Fall Time (ms)	Shutdown Threshold[1]		
										V_{OUT} Over Fault (V)	I_{OUT} Over Fault (A)	Temp Over Fault (°C)
1	Rail #1	VCC3V3	3.3	2.97	2.805	0	5	4	1	3.795	10.41	90
2	Rail #2	VCC2V5	2.5	2.25	2.125	0	5	1	1	2.875	10.41	90

Notes:

1. The values defined in these columns are the voltage, current, and temperature thresholds that causes the regulator to shut down if the value is exceeded.

Cooling Fan

The XC7Z020 AP SoC cooling fan connector J61 is wired directly to $12V_{DC}$ as shown in Figure 1-30.

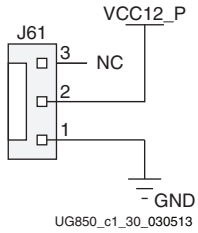


Figure 1-30: **Cooling Fan Circuit**

More information about the power system components used by the ZC702 board are available from the Texas Instruments digital power website [Ref 12].

XADC Analog-to-Digital Converter

[Figure 1-2, callout 26]

The XC7Z020 AP SoC provides an Analog Front End XADC block. The XADC block includes a dual 12-bit, 1 MSPS Analog-to-Digital Convertor (ADC) and on-chip sensors. See UG480, *7 Series FPGAs XADC Dual 12-Bit 1MSPS Analog-to-Digital Converter User Guide* for details on the capabilities of the analog front end. Figure 1-31 shows the XADC block diagram.

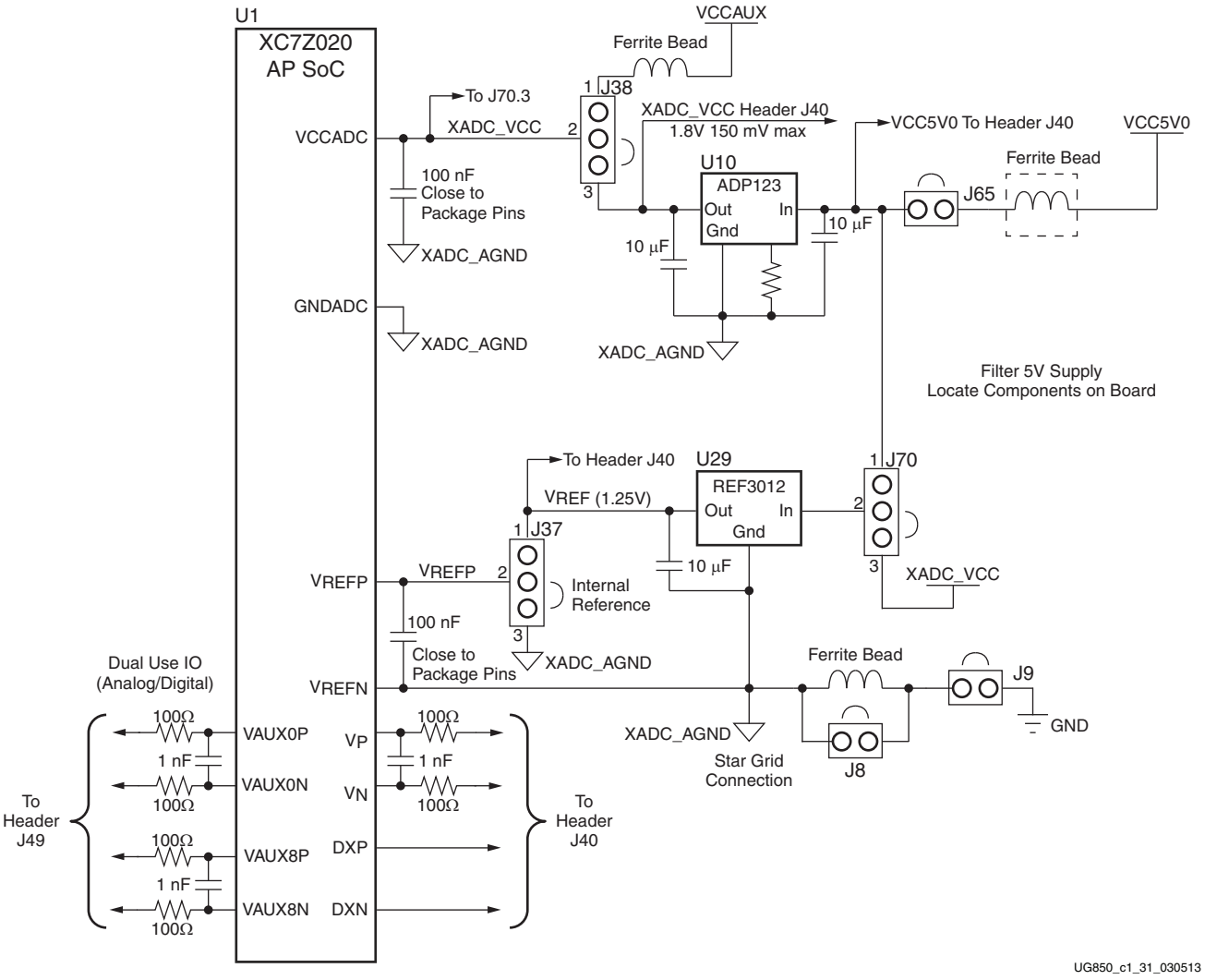


Figure 1-31: **XADC Block Diagram**

The ZC702 board supports both the internal XC7Z020 AP SoC sensor measurements and the external measurement capabilities of the XADC. Internal measurements of the die temperature, VCCINT, VCCAUX, and VCCBRAM are available.

Jumper J37 can be used to select either an external voltage reference (VREF) or on-chip voltage reference for the analog-to-digital converter.

For external measurements an XADC header (J19) is provided. This header can be used to provide analog inputs to the XC7Z020 AP SoC's dedicated VP/VN channel, and to the VAUXP[0]/VAUXN[0], VAUXP[8]/VAUXN[8] auxiliary analog input channels. Simultaneous sampling of Channel 0 and Channel 8 is supported.

A user-provided analog signal multiplexer card can be used to sample additional external analog inputs using the 4 GPIO pins available on the XADC header as multiplexer address lines. Figure 1-32 shows the XADC header connections.

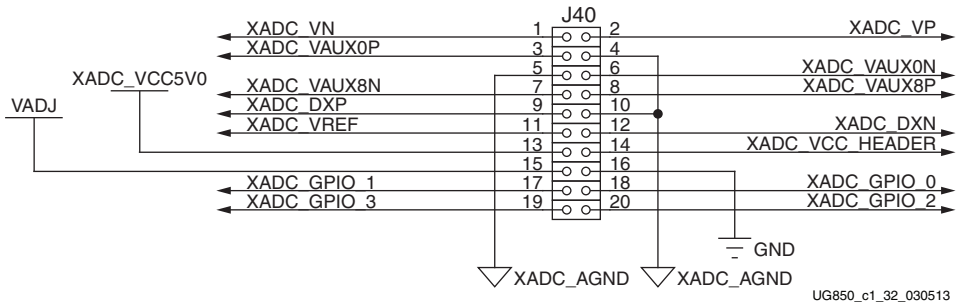


Figure 1-32: **XADC Header (J40)**

Table 1-34 describes the XADC header J40 pin functions.

Table 1-34: **XADC Header J40 Pinout**

Net Name	J19 Pin Number	Description
VN, VP	1, 2	Dedicated analog input channel for the XADC.
XADC_VAUX0P, N	3, 6	Auxiliary analog input channel 0. Also supports use as I/O inputs when anti alias capacitor is not present.
XADC_VAUX8N, P	7, 8	Auxiliary analog input channel 8. Also supports use as I/O inputs when anti alias capacitor is not present.
DXP, DXN	9, 12	Access to thermal diode.
XADC_AGND	4, 5, 10	Analog ground reference.
XADC_VREF	11	1.25V reference from the board.
XADC_VCC5V0	13	Filtered 5V supply from board.
XADC_VCC_HEADER	14	Analog 1.8V supply for XADC.
VADJ	15	VCCO supply for bank which is the source of DIO pins.
GND	16	Digital Ground (board) Reference
XADC_GPIO_3, 2, 1, 0	19, 20, 17, 18	Digital I/O. These pins should come from the same bank. These IOs should not be shared with other functions because they are required to support three-state operation.

Default Switch and Jumper Settings

Switches

[Figure 1-2, callout 24]

Default switch settings are listed in Table A-1.

Table A-1: **Default Switch Settings**

Switch	Position	Setting	Figure 1-2 Callout
SW10 (JTAG chain input select two-position DIP switch)	1	Off	23
	2	On	
SW12 (two-position DIP switch)	1	Off	19
	2	Off	
SW15 (two-position DIP switch)	1	Off	19
	2	Off	
SW16 (five-position DIP switch)	1	Right	29
	2	Right	
	3	Right	
	4	Right	
	5	Right	

Jumpers

[Figure 1-2, callout 24]

Default jumper positions are listed in Table A-2.

Table A-2: **Default Jumper Settings**

Jumper	Function	Default Position
HDR_1 X 2		
J5	CFGBVS short to GND	OFF

Table A-2: **Default Jumper Settings *(Cont'd)***

Jumper	Function	Default Position
J6	POR Master Reset	OFF
J7	USB 2.0 USB_VBUS_SEL	1-2
J8	XADC GND L3 BYPASS	OFF
J9	XADC GND	ON
J10	ARM HDR J41 PIN 2 TO VADJ	OFF
J11	UCD9248 U32 ADDR52 RESET_B	OFF
J12	FMC_VADJ_ON_B	ON
J13	UCD9248 U33 ADDR53 RESET_B	OFF
J14	UCD9248 U34 ADDR54 RESET_B	OFF
J15	CAN BUS COMMON-MODE CANH HDR	1-2
J43	ETHERNET PHY HDR	1-2
J44	USB 2.0 USB_RESET_B	OFF
J53	CAN BUS COMMON-MODE CANL HDR	1-2
J56	JTAG HDR J58 PIN 2 3.3V SEL	OFF
J65	XADC_VCC5V0 = VCC5V0	ON
HDR_1 X 3		
J20	MIO3/QSPI_IO1	OFF
J21	MIO2/QSPI_IO0	OFF
J22	MIO4/QSPI_IO2	OFF
J25	MIO5/QSPI_IO3	OFF
J26	MIO6/QSPI_CLK	OFF
J27	PS_SRST_B	1-2
J28	PS_POR_B	1-2
J30	ETHERNET PHY HDR	1-2
J31	ETHERNET PHY HDR	NONE
J32	ETHERNET PHY HDR	NONE
J33	USB 2.0 MODE	2-3
J34	USB 2.0 J1 ID SEL	1-2
J35	USB 2.0 J1 VBUS CAP SEL	1-2
J36	USB 2.0 J1 GND SEL	1-2
J37	XADC_VREP SEL	1-2
J38	XADC_VCC SEL	2-3
J70	XADC_VREF SOURCE SEL	2-3

VITA 57.1 FMC Connector Pinouts

Figure B-1 shows the pinout of the FPGA mezzanine card (FMC) low pin count (LPC) connector defined by the VITA 57.1 FMC specification. For a description of how the ZC702 board implements the FMC specification, see FPGA Mezzanine (FMC) Card Interface, page 51 and LPC Connectors J3 and J4, page 51.

	K	J	H	G	F	E	D	C	B	A
1	NC	NC	VREF_A_M2C	GND	NC	NC	PG_C2M	GND	NC	NC
2	NC	NC	PRSNT_M2C_L	CLK1_M2C_P	NC	NC	GND	DP0_C2M_P	NC	NC
3	NC	NC	GND	CLK1_M2C_N	NC	NC	GND	DP0_C2M_N	NC	NC
4	NC	NC	CLK0_M2C_P	GND	NC	NC	GBTCLK0_M2C_P	GND	NC	NC
5	NC	NC	CLK0_M2C_N	GND	NC	NC	GBTCLK0_M2C_N	GND	NC	NC
6	NC	NC	GND	LA00_P_CC	NC	NC	GND	DP0_M2C_P	NC	NC
7	NC	NC	LA02_P	LA00_N_CC	NC	NC	GND	DP0_M2C_N	NC	NC
8	NC	NC	LA02_N	GND	NC	NC	LA01_P_CC	GND	NC	NC
9	NC	NC	GND	LA03_P	NC	NC	LA01_N_CC	GND	NC	NC
10	NC	NC	LA04_P	LA03_N	NC	NC	GND	LA06_P	NC	NC
11	NC	NC	LA04_N	GND	NC	NC	LA05_P	LA06_N	NC	NC
12	NC	NC	GND	LA08_P	NC	NC	LA05_N	GND	NC	NC
13	NC	NC	LA07_P	LA08_N	NC	NC	GND	GND	NC	NC
14	NC	NC	LA07_N	GND	NC	NC	LA09_P	LA10_P	NC	NC
15	NC	NC	GND	LA12_P	NC	NC	LA09_N	LA10_N	NC	NC
16	NC	NC	LA11_P	LA12_N	NC	NC	GND	GND	NC	NC
17	NC	NC	LA11_N	GND	NC	NC	LA13_P	GND	NC	NC
18	NC	NC	GND	LA16_P	NC	NC	LA13_N	LA14_P	NC	NC
19	NC	NC	LA15_P	LA16_N	NC	NC	GND	LA14_N	NC	NC
20	NC	NC	LA15_N	GND	NC	NC	LA17_P_CC	GND	NC	NC
21	NC	NC	GND	LA20_P	NC	NC	LA17_N_CC	GND	NC	NC
22	NC	NC	LA19_P	LA20_N	NC	NC	GND	LA18_P_CC	NC	NC
23	NC	NC	LA19_N	GND	NC	NC	LA23_P	LA18_N_CC	NC	NC
24	NC	NC	GND	LA22_P	NC	NC	LA23_N	GND	NC	NC
25	NC	NC	LA21_P	LA22_N	NC	NC	GND	GND	NC	NC
26	NC	NC	LA21_N	GND	NC	NC	LA26_P	LA27_P	NC	NC
27	NC	NC	GND	LA25_P	NC	NC	LA26_N	LA27_N	NC	NC
28	NC	NC	LA24_P	LA25_N	NC	NC	GND	GND	NC	NC
29	NC	NC	LA24_N	GND	NC	NC	TCK	GND	NC	NC
30	NC	NC	GND	LA29_P	NC	NC	TDI	SCL	NC	NC
31	NC	NC	LA28_P	LA29_N	NC	NC	TDO	SDA	NC	NC
32	NC	NC	LA28_N	GND	NC	NC	3P3VAUX	GND	NC	NC
33	NC	NC	GND	LA31_P	NC	NC	TMS	GND	NC	NC
34	NC	NC	LA30_P	LA31_N	NC	NC	TRST_L	GA0	NC	NC
35	NC	NC	LA30_N	GND	NC	NC	GA1	12P0V	NC	NC
36	NC	NC	GND	LA33_P	NC	NC	3P3V	GND	NC	NC
37	NC	NC	LA32_P	LA33_N	NC	NC	GND	12P0V	NC	NC
38	NC	NC	LA32_N	GND	NC	NC	3P3V	GND	NC	NC
39	NC	NC	GND	VADJ	NC	NC	GND	3P3V	NC	NC
40	NC	NC	VADJ	GND	NC	NC	3P3V	GND	NC	NC

UG850_aB_01_081612

Figure B-1: **FMC LPC Connector Pinout**

Master UCF Listing

Overview

The ZC702 master user constraints file (UCF) template provides for designs targeting the ZC702 board. Net names in the constraints listed below correlate with net names on the latest ZC702 board schematic. Users must identify the appropriate pins and replace the net names below with net names in the user RTL.

Users can refer to the UCF files generated by tools such as Memory Interface Generator (MIG) for memory interfaces and Base System Builder (BSB) for more detailed I/O standards information required for each particular interface. The FMC connectors J3 and J4 are connected to 2.5V V_{ADJ} banks. Because each user's FMC card implements customer-specific circuitry, the FMC bank I/O standards must be uniquely defined by each customer.

Note: The UCF file listed in this appendix might not be the latest version. Always refer to the ZC702 Evaluation Kit product page (www.xilinx.com/products/boards-and-kits/EK-Z7-ZC702-G.htm) for the latest FPGA pins constraints file.

ZC702 Board UCF Listing

```
#NET   FPGA_DONE           LOC = T12   ; # Bank 0 - DONE_0
#NET   XADC_DXP            LOC = N11   ; # Bank 0 - DXP_0
#NET   XADC_AGND           LOC = K12   ; # Bank 0 - GNDADC_0
#NET   XADC_VCC            LOC = K11   ; # Bank 0 - VCCADC_0
#NET   XADC_VREFP          LOC = M11   ; # Bank 0 - VREFP_0
#NET   XADC_VN_R           LOC = M12   ; # Bank 0 - VN_0
#NET   FPGA_VBATT          LOC = G9    ; # Bank 0 - VCCBATT_0
#NET   FPGA_TCK_BUF        LOC = G11   ; # Bank 0 - TCK_0
#NET   XADC_DXN            LOC = N12   ; # Bank 0 - DXN_0
#NET   XADC_AGND           LOC = L12   ; # Bank 0 - VREFN_0
#NET   XADC_VP_R           LOC = L11   ; # Bank 0 - VP_0
#NET   GND                 LOC = G10   ; # Bank 0 - RSVDGND
#NET   VCC2V5              LOC = T10   ; # Bank 0 - RSVDVCC
#NET   VCC2V5              LOC = T8    ; # Bank 0 - RSVDVCC
#NET   FPGA_INIT_B         LOC = T14   ; # Bank 0 - INIT_B_0
#NET   FPGA_TDI_BUF        LOC = H13   ; # Bank 0 - TDI_0
#NET   JTAG_TDO_BUF        LOC = G14   ; # Bank 0 - TDO_0
#NET   VCC2V5              LOC = T7    ; # Bank 0 - RSVDVCC
#NET   3N579               LOC = T13   ; # Bank 0 - CFGBVS_0
#NET   FPGA_PROG_B         LOC = T11   ; # Bank 0 - PROGRAM_B_0
#NET   FPGA_TMS_BUF        LOC = G12   ; # Bank 0 - TMS_0
NET   PL_PJTAG_TDO_R       LOC = R7    | IOSTANDARD=LVCMOS25; # Bank 13  VCCO - VADJ - IO_0_13
NET   PL_PJTAG_TCK         LOC = V10   | IOSTANDARD=LVCMOS25; # Bank 13  VCCO - VADJ - IO_L1P_T0_13
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NET  PL_PJTAG_TMS          LOC = V9   | IOSTANDARD=LVCMOS25; # Bank 13  VCCO - VADJ - IO_L1N_T0_13
NET  PL_PJTAG_TDI          LOC = V8   | IOSTANDARD=LVCMOS25; # Bank 13  VCCO - VADJ - IO_L2P_T0_13
NET  IIC_SDA_MAIN_LS       LOC = W8   | IOSTANDARD=LVCMOS25; # Bank 13  VCCO - VADJ - IO_L2N_T0_13
NET  IIC_SCL_MAIN_LS       LOC = W11  | IOSTANDARD=LVCMOS25; # Bank 13  VCCO - VADJ - IO_L3P_T0_DQS_13
NET  PMOD2_1_LS            LOC = W10  | IOSTANDARD=LVCMOS25; # Bank 13  VCCO - VADJ - IO_L3N_T0_DQS_13
NET  FMC2_LPC_LA23_P       LOC = V12  | IOSTANDARD=LVCMOS25; # Bank 13  VCCO - VADJ - IO_L4P_T0_13
NET  FMC2_LPC_LA23_N       LOC = W12  | IOSTANDARD=LVCMOS25; # Bank 13  VCCO - VADJ - IO_L4N_T0_13
NET  FMC2_LPC_LA26_P       LOC = U12  | IOSTANDARD=LVCMOS25; # Bank 13  VCCO - VADJ - IO_L5P_T0_13
NET  FMC2_LPC_LA26_N       LOC = U11  | IOSTANDARD=LVCMOS25; # Bank 13  VCCO - VADJ - IO_L5N_T0_13
NET  FMC2_LPC_LA22_P       LOC = U10  | IOSTANDARD=LVCMOS25; # Bank 13  VCCO - VADJ - IO_L6P_T0_13
NET  FMC2_LPC_LA22_N       LOC = U9   | IOSTANDARD=LVCMOS25; # Bank 13  VCCO - VADJ - IO_L6N_T0_VREF_13
NET  FMC2_LPC_LA25_P       LOC = AA12 | IOSTANDARD=LVCMOS25; # Bank 13  VCCO - VADJ - IO_L7P_T1_13
NET  FMC2_LPC_LA25_N       LOC = AB12 | IOSTANDARD=LVCMOS25; # Bank 13  VCCO - VADJ - IO_L7N_T1_13
NET  FMC2_LPC_LA29_P       LOC = AA11 | IOSTANDARD=LVCMOS25; # Bank 13  VCCO - VADJ - IO_L8P_T1_13
NET  FMC2_LPC_LA29_N       LOC = AB11 | IOSTANDARD=LVCMOS25; # Bank 13  VCCO - VADJ - IO_L8N_T1_13
NET  FMC2_LPC_LA31_P       LOC = AB10 | IOSTANDARD=LVCMOS25; # Bank 13  VCCO - VADJ - IO_L9P_T1_DQS_13
NET  FMC2_LPC_LA31_N       LOC = AB9  | IOSTANDARD=LVCMOS25; # Bank 13  VCCO - VADJ - IO_L9N_T1_DQS_13
NET  FMC2_LPC_LA33_P       LOC = Y11  | IOSTANDARD=LVCMOS25; # Bank 13  VCCO - VADJ - IO_L10P_T1_13
NET  FMC2_LPC_LA33_N       LOC = Y10  | IOSTANDARD=LVCMOS25; # Bank 13  VCCO - VADJ - IO_L10N_T1_13
NET  FMC2_LPC_LA18_CC_P    LOC = AA9  | IOSTANDARD=LVCMOS25; # Bank 13  VCCO - VADJ - IO_L11P_T1_SRCC_13
NET  FMC2_LPC_LA18_CC_N    LOC = AA8  | IOSTANDARD=LVCMOS25; # Bank 13  VCCO - VADJ - IO_L11N_T1_SRCC_13
NET  USRCLK_P              LOC = Y9   | IOSTANDARD=LVDS_25;  # Bank 13  VCCO - VADJ - IO_L12P_T1_MRCC_13
NET  USRCLK_N              LOC = Y8   | IOSTANDARD=LVDS_25;  # Bank 13  VCCO - VADJ - IO_L12N_T1_MRCC_13
NET  FMC2_LPC_CLK1_M2C_P   LOC = Y6   | IOSTANDARD=LVCMOS25; # Bank 13  VCCO - VADJ - IO_L13P_T2_MRCC_13
NET  FMC2_LPC_CLK1_M2C_N   LOC = Y5   | IOSTANDARD=LVCMOS25; # Bank 13  VCCO - VADJ - IO_L13N_T2_MRCC_13
NET  FMC2_LPC_LA17_CC_P    LOC = AA7  | IOSTANDARD=LVCMOS25; # Bank 13  VCCO - VADJ - IO_L14P_T2_SRCC_13
NET  FMC2_LPC_LA17_CC_N    LOC = AA6  | IOSTANDARD=LVCMOS25; # Bank 13  VCCO - VADJ - IO_L14N_T2_SRCC_13
NET  FMC2_LPC_LA27_P       LOC = AB2  | IOSTANDARD=LVCMOS25; # Bank 13  VCCO - VADJ - IO_L15P_T2_DQS_13
NET  FMC2_LPC_LA27_N       LOC = AB1  | IOSTANDARD=LVCMOS25; # Bank 13  VCCO - VADJ - IO_L15N_T2_DQS_13
NET  FMC2_LPC_LA28_P       LOC = AB5  | IOSTANDARD=LVCMOS25; # Bank 13  VCCO - VADJ - IO_L16P_T2_13
NET  FMC2_LPC_LA28_N       LOC = AB4  | IOSTANDARD=LVCMOS25; # Bank 13  VCCO - VADJ - IO_L16N_T2_13
NET  FMC2_LPC_LA30_P       LOC = AB7  | IOSTANDARD=LVCMOS25; # Bank 13  VCCO - VADJ - IO_L17P_T2_13
NET  FMC2_LPC_LA30_N       LOC = AB6  | IOSTANDARD=LVCMOS25; # Bank 13  VCCO - VADJ - IO_L17N_T2_13
NET  FMC2_LPC_LA32_P       LOC = Y4   | IOSTANDARD=LVCMOS25; # Bank 13  VCCO - VADJ - IO_L18P_T2_13
NET  FMC2_LPC_LA32_N       LOC = AA4  | IOSTANDARD=LVCMOS25; # Bank 13  VCCO - VADJ - IO_L18N_T2_13
NET  FMC2_LPC_LA19_P       LOC = R6   | IOSTANDARD=LVCMOS25; # Bank 13  VCCO - VADJ - IO_L19P_T3_13
NET  FMC2_LPC_LA19_N       LOC = T6   | IOSTANDARD=LVCMOS25; # Bank 13  VCCO - VADJ - IO_L19N_T3_VREF_13
NET  FMC2_LPC_LA20_P       LOC = T4   | IOSTANDARD=LVCMOS25; # Bank 13  VCCO - VADJ - IO_L20P_T3_13
NET  FMC2_LPC_LA20_N       LOC = U4   | IOSTANDARD=LVCMOS25; # Bank 13  VCCO - VADJ - IO_L20N_T3_13
NET  FMC2_LPC_LA21_P       LOC = V5   | IOSTANDARD=LVCMOS25; # Bank 13  VCCO - VADJ - IO_L21P_T3_DQS_13
NET  FMC2_LPC_LA21_N       LOC = V4   | IOSTANDARD=LVCMOS25; # Bank 13  VCCO - VADJ - IO_L21N_T3_DQS_13
NET  FMC2_LPC_LA24_P       LOC = U6   | IOSTANDARD=LVCMOS25; # Bank 13  VCCO - VADJ - IO_L22P_T3_13
NET  FMC2_LPC_LA24_N       LOC = U5   | IOSTANDARD=LVCMOS25; # Bank 13  VCCO - VADJ - IO_L22N_T3_13
NET  PMOD2_0_LS            LOC = V7   | IOSTANDARD=LVCMOS25; # Bank 13  VCCO - VADJ - IO_L23P_T3_13
NET  GPIO_DIP_SW1          LOC = W7   | IOSTANDARD=LVCMOS25; # Bank 13  VCCO - VADJ - IO_L23N_T3_13
NET  GPIO_DIP_SW0          LOC = W6   | IOSTANDARD=LVCMOS25; # Bank 13  VCCO - VADJ - IO_L24P_T3_13
NET  PMOD1_3_LS            LOC = W5   | IOSTANDARD=LVCMOS25; # Bank 13  VCCO - VADJ - IO_L24N_T3_13
NET  IIC_RTC_IRQ_1_B       LOC = U7   | IOSTANDARD=LVCMOS25; # Bank 13  VCCO - VADJ - IO_25_13
NET  HDMI_R_D12            LOC = U19  | IOSTANDARD=LVCMOS25; # Bank 33  VCCO - VADJ - IO_0_33
NET  FMC2_LPC_LA07_P       LOC = T21  | IOSTANDARD=LVCMOS25; # Bank 33  VCCO - VADJ - IO_L1P_T0_33
NET  FMC2_LPC_LA07_N       LOC = U21  | IOSTANDARD=LVCMOS25; # Bank 33  VCCO - VADJ - IO_L1N_T0_33
NET  FMC2_LPC_LA14_P       LOC = T22  | IOSTANDARD=LVCMOS25; # Bank 33  VCCO - VADJ - IO_L2P_T0_33
NET  FMC2_LPC_LA14_N       LOC = U22  | IOSTANDARD=LVCMOS25; # Bank 33  VCCO - VADJ - IO_L2N_T0_33
NET  FMC2_LPC_LA13_P       LOC = V22  | IOSTANDARD=LVCMOS25; # Bank 33  VCCO - VADJ - IO_L3P_T0_DQS_33
NET  FMC2_LPC_LA13_N       LOC = W22  | IOSTANDARD=LVCMOS25; # Bank 33  VCCO - VADJ - IO_L3N_T0_DQS_33
NET  HDMI_R_D9             LOC = W20  | IOSTANDARD=LVCMOS25; # Bank 33  VCCO - VADJ - IO_L4P_T0_33
NET  HDMI_R_D8             LOC = W21  | IOSTANDARD=LVCMOS25; # Bank 33  VCCO - VADJ - IO_L4N_T0_33
NET  HDMI_R_D7             LOC = U20  | IOSTANDARD=LVCMOS25; # Bank 33  VCCO - VADJ - IO_L5P_T0_33
NET  HDMI_R_D6             LOC = V20  | IOSTANDARD=LVCMOS25; # Bank 33  VCCO - VADJ - IO_L5N_T0_33
NET  HDMI_R_D5             LOC = V18  | IOSTANDARD=LVCMOS25; # Bank 33  VCCO - VADJ - IO_L6P_T0_33
NET  HDMI_R_D4             LOC = V19  | IOSTANDARD=LVCMOS25; # Bank 33  VCCO - VADJ - IO_L6N_T0_VREF_33
NET  HDMI_R_D3             LOC = AA22 | IOSTANDARD=LVCMOS25; # Bank 33  VCCO - VADJ - IO_L7P_T1_33
NET  HDMI_R_D2             LOC = AB22 | IOSTANDARD=LVCMOS25; # Bank 33  VCCO - VADJ - IO_L7N_T1_33
NET  HDMI_R_D1             LOC = AA21 | IOSTANDARD=LVCMOS25; # Bank 33  VCCO - VADJ - IO_L8P_T1_33
NET  HDMI_R_D0             LOC = AB21 | IOSTANDARD=LVCMOS25; # Bank 33  VCCO - VADJ - IO_L8N_T1_33
NET  FMC2_LPC_LA10_P       LOC = Y20  | IOSTANDARD=LVCMOS25; # Bank 33  VCCO - VADJ - IO_L9P_T1_DQS_33
NET  FMC2_LPC_LA10_N       LOC = Y21  | IOSTANDARD=LVCMOS25; # Bank 33  VCCO - VADJ - IO_L9N_T1_DQS_33
NET  FMC2_LPC_LA05_P       LOC = AB19 | IOSTANDARD=LVCMOS25; # Bank 33  VCCO - VADJ - IO_L10P_T1_33
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NET  FMC2_LPC_LA05_N      LOC = AB20 | IOSTANDARD=LVCMOS25; # Bank 33  VCCO - VADJ - IO_L10N_T1_33
NET  FMC2_LPC_LA00_CC_P   LOC = Y19  | IOSTANDARD=LVCMOS25; # Bank 33  VCCO - VADJ - IO_L11P_T1_SRCC_33
NET  FMC2_LPC_LA00_CC_N   LOC = AA19 | IOSTANDARD=LVCMOS25; # Bank 33  VCCO - VADJ - IO_L11N_T1_SRCC_33
NET  FMC2_LPC_CLK0_M2C_P  LOC = Y18  | IOSTANDARD=LVCMOS25; # Bank 33  VCCO - VADJ - IO_L12P_T1_MRCC_33
NET  FMC2_LPC_CLK0_M2C_N  LOC = AA18 | IOSTANDARD=LVCMOS25; # Bank 33  VCCO - VADJ - IO_L12N_T1_MRCC_33
NET  PMOD1_2_LS           LOC = W17  | IOSTANDARD=LVCMOS25; # Bank 33  VCCO - VADJ - IO_L13P_T2_MRCC_33
NET  HDMI_R_D10           LOC = W18  | IOSTANDARD=LVCMOS25; # Bank 33  VCCO - VADJ - IO_L13N_T2_MRCC_33
NET  FMC2_LPC_LA01_CC_P   LOC = W16  | IOSTANDARD=LVCMOS25; # Bank 33  VCCO - VADJ - IO_L14P_T2_SRCC_33
NET  FMC2_LPC_LA01_CC_N   LOC = Y16  | IOSTANDARD=LVCMOS25; # Bank 33  VCCO - VADJ - IO_L14N_T2_SRCC_33
NET  FMC2_LPC_LA09_P      LOC = U15  | IOSTANDARD=LVCMOS25; # Bank 33  VCCO - VADJ - IO_L15P_T2_DQS_33
NET  FMC2_LPC_LA09_N      LOC = U16  | IOSTANDARD=LVCMOS25; # Bank 33  VCCO - VADJ - IO_L15N_T2_DQS_33
NET  FMC2_LPC_LA06_P      LOC = U17  | IOSTANDARD=LVCMOS25; # Bank 33  VCCO - VADJ - IO_L16P_T2_33
NET  FMC2_LPC_LA06_N      LOC = V17  | IOSTANDARD=LVCMOS25; # Bank 33  VCCO - VADJ - IO_L16N_T2_33
NET  FMC2_LPC_LA08_P      LOC = AA17 | IOSTANDARD=LVCMOS25; # Bank 33  VCCO - VADJ - IO_L17P_T2_33
NET  FMC2_LPC_LA08_N      LOC = AB17 | IOSTANDARD=LVCMOS25; # Bank 33  VCCO - VADJ - IO_L17N_T2_33
NET  FMC2_LPC_LA03_P      LOC = AA16 | IOSTANDARD=LVCMOS25; # Bank 33  VCCO - VADJ - IO_L18P_T2_33
NET  FMC2_LPC_LA03_N      LOC = AB16 | IOSTANDARD=LVCMOS25; # Bank 33  VCCO - VADJ - IO_L18N_T2_33
NET  FMC2_LPC_LA02_P      LOC = V14  | IOSTANDARD=LVCMOS25; # Bank 33  VCCO - VADJ - IO_L19P_T3_33
NET  FMC2_LPC_LA02_N      LOC = V15  | IOSTANDARD=LVCMOS25; # Bank 33  VCCO - VADJ - IO_L19N_T3_VREF_33
NET  FMC2_LPC_LA04_P      LOC = V13  | IOSTANDARD=LVCMOS25; # Bank 33  VCCO - VADJ - IO_L20P_T3_33
NET  FMC2_LPC_LA04_N      LOC = W13  | IOSTANDARD=LVCMOS25; # Bank 33  VCCO - VADJ - IO_L20N_T3_33
NET  FMC2_LPC_LA12_P      LOC = W15  | IOSTANDARD=LVCMOS25; # Bank 33  VCCO - VADJ - IO_L21P_T3_DQS_33
NET  FMC2_LPC_LA12_N      LOC = Y15  | IOSTANDARD=LVCMOS25; # Bank 33  VCCO - VADJ - IO_L21N_T3_DQS_33
NET  FMC2_LPC_LA11_P      LOC = Y14  | IOSTANDARD=LVCMOS25; # Bank 33  VCCO - VADJ - IO_L22P_T3_33
NET  FMC2_LPC_LA11_N      LOC = AA14 | IOSTANDARD=LVCMOS25; # Bank 33  VCCO - VADJ - IO_L22N_T3_33
NET  FMC2_LPC_LA15_P      LOC = Y13  | IOSTANDARD=LVCMOS25; # Bank 33  VCCO - VADJ - IO_L23P_T3_33
NET  FMC2_LPC_LA15_N      LOC = AA13 | IOSTANDARD=LVCMOS25; # Bank 33  VCCO - VADJ - IO_L23N_T3_33
NET  FMC2_LPC_LA16_P      LOC = AB14 | IOSTANDARD=LVCMOS25; # Bank 33  VCCO - VADJ - IO_L24P_T3_33
NET  FMC2_LPC_LA16_N      LOC = AB15 | IOSTANDARD=LVCMOS25; # Bank 33  VCCO - VADJ - IO_L24N_T3_33
NET  HDMI_INT             LOC = U14  | IOSTANDARD=LVCMOS25; # Bank 33  VCCO - VADJ - IO_25_33
NET  HDMI_R_VSYNC         LOC = H15  | IOSTANDARD=LVCMOS25; # Bank 34  VCCO - VADJ - IO_0_34
NET  FMC1_LPC_LA07_P      LOC = J15  | IOSTANDARD=LVCMOS25; # Bank 34  VCCO - VADJ - IO_L1P_T0_34
NET  FMC1_LPC_LA07_N      LOC = K15  | IOSTANDARD=LVCMOS25; # Bank 34  VCCO - VADJ - IO_L1N_T0_34
NET  FMC1_LPC_LA14_P      LOC = J16  | IOSTANDARD=LVCMOS25; # Bank 34  VCCO - VADJ - IO_L2P_T0_34
NET  FMC1_LPC_LA14_N      LOC = J17  | IOSTANDARD=LVCMOS25; # Bank 34  VCCO - VADJ - IO_L2N_T0_34
NET  6N1412               LOC = K16  | IOSTANDARD=LVCMOS25; # Bank 34  VCCO - VADJ - IO_L3P_T0_DQS_PUDC_B_34
NET  HDMI_R_CLK           LOC = L16  | IOSTANDARD=LVCMOS25; # Bank 34  VCCO - VADJ - IO_L3N_T0_DQS_34
NET  FMC1_LPC_LA10_P      LOC = L17  | IOSTANDARD=LVCMOS25; # Bank 34  VCCO - VADJ - IO_L4P_T0_34
NET  FMC1_LPC_LA10_N      LOC = M17  | IOSTANDARD=LVCMOS25; # Bank 34  VCCO - VADJ - IO_L4N_T0_34
NET  FMC1_LPC_LA05_P      LOC = N17  | IOSTANDARD=LVCMOS25; # Bank 34  VCCO - VADJ - IO_L5P_T0_34
NET  FMC1_LPC_LA05_N      LOC = N18  | IOSTANDARD=LVCMOS25; # Bank 34  VCCO - VADJ - IO_L5N_T0_34
NET  FMC1_LPC_LA09_P      LOC = M15  | IOSTANDARD=LVCMOS25; # Bank 34  VCCO - VADJ - IO_L6P_T0_34
NET  FMC1_LPC_LA09_N      LOC = M16  | IOSTANDARD=LVCMOS25; # Bank 34  VCCO - VADJ - IO_L6N_T0_VREF_34
NET  FMC1_LPC_LA06_P      LOC = J18  | IOSTANDARD=LVCMOS25; # Bank 34  VCCO - VADJ - IO_L7P_T1_34
NET  FMC1_LPC_LA06_N      LOC = K18  | IOSTANDARD=LVCMOS25; # Bank 34  VCCO - VADJ - IO_L7N_T1_34
NET  FMC1_LPC_LA08_P      LOC = J21  | IOSTANDARD=LVCMOS25; # Bank 34  VCCO - VADJ - IO_L8P_T1_34
NET  FMC1_LPC_LA08_N      LOC = J22  | IOSTANDARD=LVCMOS25; # Bank 34  VCCO - VADJ - IO_L8N_T1_34
NET  FMC1_LPC_LA03_P      LOC = J20  | IOSTANDARD=LVCMOS25; # Bank 34  VCCO - VADJ - IO_L9P_T1_DQS_34
NET  FMC1_LPC_LA03_N      LOC = K21  | IOSTANDARD=LVCMOS25; # Bank 34  VCCO - VADJ - IO_L9N_T1_DQS_34
NET  FMC1_LPC_LA02_P      LOC = L21  | IOSTANDARD=LVCMOS25; # Bank 34  VCCO - VADJ - IO_L10P_T1_34
NET  FMC1_LPC_LA02_N      LOC = L22  | IOSTANDARD=LVCMOS25; # Bank 34  VCCO - VADJ - IO_L10N_T1_34
NET  FMC1_LPC_LA00_CC_P   LOC = K19  | IOSTANDARD=LVCMOS25; # Bank 34  VCCO - VADJ - IO_L11P_T1_SRCC_34
NET  FMC1_LPC_LA00_CC_N   LOC = K20  | IOSTANDARD=LVCMOS25; # Bank 34  VCCO - VADJ - IO_L11N_T1_SRCC_34
NET  FMC1_LPC_CLK0_M2C_P  LOC = L18  | IOSTANDARD=LVCMOS25; # Bank 34  VCCO - VADJ - IO_L12P_T1_MRCC_34
NET  FMC1_LPC_CLK0_M2C_N  LOC = L19  | IOSTANDARD=LVCMOS25; # Bank 34  VCCO - VADJ - IO_L12N_T1_MRCC_34
NET  FMC1_LPC_CLK1_M2C_P  LOC = M19  | IOSTANDARD=LVCMOS25; # Bank 34  VCCO - VADJ - IO_L13P_T2_MRCC_34
NET  FMC1_LPC_CLK1_M2C_N  LOC = M20  | IOSTANDARD=LVCMOS25; # Bank 34  VCCO - VADJ - IO_L13N_T2_MRCC_34
NET  FMC1_LPC_LA01_CC_P   LOC = N19  | IOSTANDARD=LVCMOS25; # Bank 34  VCCO - VADJ - IO_L14P_T2_SRCC_34
NET  FMC1_LPC_LA01_CC_N   LOC = N20  | IOSTANDARD=LVCMOS25; # Bank 34  VCCO - VADJ - IO_L14N_T2_SRCC_34
NET  FMC1_LPC_LA04_P      LOC = M21  | IOSTANDARD=LVCMOS25; # Bank 34  VCCO - VADJ - IO_L15P_T2_DQS_34
NET  FMC1_LPC_LA04_N      LOC = M22  | IOSTANDARD=LVCMOS25; # Bank 34  VCCO - VADJ - IO_L15N_T2_DQS_34
NET  FMC1_LPC_LA12_P      LOC = N22  | IOSTANDARD=LVCMOS25; # Bank 34  VCCO - VADJ - IO_L16P_T2_34
NET  FMC1_LPC_LA12_N      LOC = P22  | IOSTANDARD=LVCMOS25; # Bank 34  VCCO - VADJ - IO_L16N_T2_34
NET  FMC1_LPC_LA11_P      LOC = R20  | IOSTANDARD=LVCMOS25; # Bank 34  VCCO - VADJ - IO_L17P_T2_34
NET  FMC1_LPC_LA11_N      LOC = R21  | IOSTANDARD=LVCMOS25; # Bank 34  VCCO - VADJ - IO_L17N_T2_34
NET  FMC1_LPC_LA15_P      LOC = P20  | IOSTANDARD=LVCMOS25; # Bank 34  VCCO - VADJ - IO_L18P_T2_34
NET  FMC1_LPC_LA15_N      LOC = P21  | IOSTANDARD=LVCMOS25; # Bank 34  VCCO - VADJ - IO_L18N_T2_34
NET  FMC1_LPC_LA16_P      LOC = N15  | IOSTANDARD=LVCMOS25; # Bank 34  VCCO - VADJ - IO_L19P_T3_34
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NET  FMC1_LPC_LA16_N      LOC = P15  | IOSTANDARD=LVCMOS25; # Bank 34  VCCO - VADJ - IO_L19N_T3_VREF_34
NET  PMOD2_3_LS           LOC = P17  | IOSTANDARD=LVCMOS25; # Bank 34  VCCO - VADJ - IO_L20P_T3_34
NET  PMOD2_2_LS           LOC = P18  | IOSTANDARD=LVCMOS25; # Bank 34  VCCO - VADJ - IO_L20N_T3_34
NET  HDMI_R_D15           LOC = T16  | IOSTANDARD=LVCMOS25; # Bank 34  VCCO - VADJ - IO_L21P_T3_DQS_34
NET  HDMI_R_D14           LOC = T17  | IOSTANDARD=LVCMOS25; # Bank 34  VCCO - VADJ - IO_L21N_T3_DQS_34
NET  HDMI_R_D13           LOC = R19  | IOSTANDARD=LVCMOS25; # Bank 34  VCCO - VADJ - IO_L22P_T3_34
NET  HDMI_R_D11           LOC = T19  | IOSTANDARD=LVCMOS25; # Bank 34  VCCO - VADJ - IO_L22N_T3_34
NET  HDMI_R_HSYNC         LOC = R18  | IOSTANDARD=LVCMOS25; # Bank 34  VCCO - VADJ - IO_L23P_T3_34
NET  HDMI_R_DE            LOC = T18  | IOSTANDARD=LVCMOS25; # Bank 34  VCCO - VADJ - IO_L23N_T3_34
NET  FMC1_LPC_LA13_P      LOC = P16  | IOSTANDARD=LVCMOS25; # Bank 34  VCCO - VADJ - IO_L24P_T3_34
NET  FMC1_LPC_LA13_N      LOC = R16  | IOSTANDARD=LVCMOS25; # Bank 34  VCCO - VADJ - IO_L24N_T3_34
NET  HDMI_R_SPDIF         LOC = R15  | IOSTANDARD=LVCMOS25; # Bank 34  VCCO - VADJ - IO_25_34
NET  XADC_GPIO_0          LOC = H17  | IOSTANDARD=LVCMOS25; # Bank 35  VCCO - VADJ - IO_0_35
NET  XADC_VAUX0P_R        LOC = F16  | IOSTANDARD=LVCMOS25; # Bank 35  VCCO - VADJ - IO_L1P_T0_AD0P_35
NET  XADC_VAUX0N_R        LOC = E16  | IOSTANDARD=LVCMOS25; # Bank 35  VCCO - VADJ - IO_L1N_T0_AD0N_35
NET  XADC_VAUX8P_R        LOC = D16  | IOSTANDARD=LVCMOS25; # Bank 35  VCCO - VADJ - IO_L2P_T0_AD8P_35
NET  XADC_VAUX8N_R        LOC = D17  | IOSTANDARD=LVCMOS25; # Bank 35  VCCO - VADJ - IO_L2N_T0_AD8N_35
NET  PMOD1_0_LS           LOC = E15  | IOSTANDARD=LVCMOS25; # Bank 35  VCCO - VADJ - IO_L3P_T0_DQS_AD1P_35
NET  PMOD1_1_LS           LOC = D15  | IOSTANDARD=LVCMOS25; # Bank 35  VCCO - VADJ - IO_L3N_T0_DQS_AD1N_35
NET  FMC1_LPC_LA23_P      LOC = G15  | IOSTANDARD=LVCMOS25; # Bank 35  VCCO - VADJ - IO_L4P_T0_35
NET  FMC1_LPC_LA23_N      LOC = G16  | IOSTANDARD=LVCMOS25; # Bank 35  VCCO - VADJ - IO_L4N_T0_35
NET  FMC1_LPC_LA26_P      LOC = F18  | IOSTANDARD=LVCMOS25; # Bank 35  VCCO - VADJ- IO_L5P_T0_AD9P_35
NET  FMC1_LPC_LA26_N      LOC = E18  | IOSTANDARD=LVCMOS25; # Bank 35  VCCO - VADJ - IO_L5N_T0_AD9N_35
NET  FMC1_LPC_LA22_P      LOC = G17  | IOSTANDARD=LVCMOS25; # Bank 35  VCCO - VADJ - IO_L6P_T0_35
NET  FMC1_LPC_LA22_N      LOC = F17  | IOSTANDARD=LVCMOS25; # Bank 35  VCCO - VADJ - IO_L6N_T0_VREF_35
NET  FMC1_LPC_LA25_P      LOC = C15  | IOSTANDARD=LVCMOS25; # Bank 35  VCCO - VADJ - IO_L7P_T1_AD2P_35
NET  FMC1_LPC_LA25_N      LOC = B15  | IOSTANDARD=LVCMOS25; # Bank 35  VCCO - VADJ - IO_L7N_T1_AD2N_35
NET  FMC1_LPC_LA29_P      LOC = B16  | IOSTANDARD=LVCMOS25; # Bank 35  VCCO - VADJ - IO_L8P_T1_AD10P_35
NET  FMC1_LPC_LA29_N      LOC = B17  | IOSTANDARD=LVCMOS25; # Bank 35  VCCO - VADJ - IO_L8N_T1_AD10N_35
NET  FMC1_LPC_LA31_P      LOC = A16  | IOSTANDARD=LVCMOS25; # Bank 35  VCCO - VADJ - IO_L9P_T1_DQS_AD3P_35
NET  FMC1_LPC_LA31_N      LOC = A17  | IOSTANDARD=LVCMOS25; # Bank 35  VCCO - VADJ - IO_L9N_T1_DQS_AD3N_35
NET  FMC1_LPC_LA33_P      LOC = A18  | IOSTANDARD=LVCMOS25; # Bank 35  VCCO - VADJ - IO_L10P_T1_AD11P_35
NET  FMC1_LPC_LA33_N      LOC = A19  | IOSTANDARD=LVCMOS25; # Bank 35  VCCO - VADJ - IO_L10N_T1_AD11N_35
NET  FMC1_LPC_LA27_P      LOC = C17  | IOSTANDARD=LVCMOS25; # Bank 35  VCCO - VADJ - IO_L11P_T1_SRCC_35
NET  FMC1_LPC_LA27_N      LOC = C18  | IOSTANDARD=LVCMOS25; # Bank 35  VCCO - VADJ - IO_L11N_T1_SRCC_35
NET  SYSCLK_P             LOC = D18  | IOSTANDARD=LVDS_25;  # Bank 35  VCCO - VADJ - IO_L12P_T1_MRCC_35
NET  SYSCLK_N             LOC = C19  | IOSTANDARD=LVDS_25;  # Bank 35  VCCO - VADJ - IO_L12N_T1_MRCC_35
NET  FMC1_LPC_LA17_CC_P   LOC = B19  | IOSTANDARD=LVCMOS25; # Bank 35  VCCO - VADJ - IO_L13P_T2_MRCC_35
NET  FMC1_LPC_LA17_CC_N   LOC = B20  | IOSTANDARD=LVCMOS25; # Bank 35  VCCO - VADJ - IO_L13N_T2_MRCC_35
NET  FMC1_LPC_LA18_CC_P   LOC = D20  | IOSTANDARD=LVCMOS25; # Bank 35  VCCO - VADJ - IO_L14P_T2_AD4P_SRCC_35
NET  FMC1_LPC_LA18_CC_N   LOC = C20  | IOSTANDARD=LVCMOS25; # Bank 35  VCCO - VADJ - IO_L14N_T2_AD4N_SRCC_35
NET  FMC1_LPC_LA24_P      LOC = A21  | IOSTANDARD=LVCMOS25; # Bank 35  VCCO - VADJ - IO_L15P_T2_DQS_AD12P_35
NET  FMC1_LPC_LA24_N      LOC = A22  | IOSTANDARD=LVCMOS25; # Bank 35  VCCO - VADJ - IO_L15N_T2_DQS_AD12N_35
NET  FMC1_LPC_LA28_P      LOC = D22  | IOSTANDARD=LVCMOS25; # Bank 35  VCCO - VADJ - IO_L16P_T2_35
NET  FMC1_LPC_LA28_N      LOC = C22  | IOSTANDARD=LVCMOS25; # Bank 35  VCCO - VADJ - IO_L16N_T2_35
NET  FMC1_LPC_LA30_P      LOC = E21  | IOSTANDARD=LVCMOS25; # Bank 35  VCCO - VADJ - IO_L17P_T2_AD5P_35
NET  FMC1_LPC_LA30_N      LOC = D21  | IOSTANDARD=LVCMOS25; # Bank 35  VCCO - VADJ - IO_L17N_T2_AD5N_35
NET  FMC1_LPC_LA32_P      LOC = B21  | IOSTANDARD=LVCMOS25; # Bank 35  VCCO - VADJ - IO_L18P_T2_AD13P_35
NET  FMC1_LPC_LA32_N      LOC = B22  | IOSTANDARD=LVCMOS25; # Bank 35  VCCO - VADJ - IO_L18N_T2_AD13N_35
NET  FMC_C2M_PG_LS        LOC = H19  | IOSTANDARD=LVCMOS25; # Bank 35  VCCO - VADJ - IO_L19P_T3_35
NET  HDMI_SPDIF_OUT_LS    LOC = H20  | IOSTANDARD=LVCMOS25; # Bank 35  VCCO - VADJ - IO_L19N_T3_VREF_35
NET  GPIO_SW_N            LOC = G19  | IOSTANDARD=LVCMOS25; # Bank 35  VCCO - VADJ - IO_L20P_T3_AD6P_35
NET  GPIO_SW_S            LOC = F19  | IOSTANDARD=LVCMOS25; # Bank 35  VCCO - VADJ - IO_L20N_T3_AD6N_35
NET  FMC1_LPC_LA19_P      LOC = E19  | IOSTANDARD=LVCMOS25; # Bank 35  VCCO - VADJ - IO_L21P_T3_DQS_AD14P_35
NET  FMC1_LPC_LA19_N      LOC = E20  | IOSTANDARD=LVCMOS25; # Bank 35  VCCO - VADJ - IO_L21N_T3_DQS_AD14N_35
NET  FMC1_LPC_LA20_P      LOC = G20  | IOSTANDARD=LVCMOS25; # Bank 35  VCCO - VADJ - IO_L22P_T3_AD7P_35
NET  FMC1_LPC_LA20_N      LOC = G21  | IOSTANDARD=LVCMOS25; # Bank 35  VCCO - VADJ - IO_L22N_T3_AD7N_35
NET  FMC1_LPC_LA21_P      LOC = F21  | IOSTANDARD=LVCMOS25; # Bank 35  VCCO - VADJ - IO_L23P_T3_35
NET  FMC1_LPC_LA21_N      LOC = F22  | IOSTANDARD=LVCMOS25; # Bank 35  VCCO - VADJ - IO_L23N_T3_35
NET  XADC_GPIO_1          LOC = H22  | IOSTANDARD=LVCMOS25; # Bank 35  VCCO - VADJ - IO_L24P_T3_AD15P_35
NET  XADC_GPIO_2          LOC = G22  | IOSTANDARD=LVCMOS25; # Bank 35  VCCO - VADJ - IO_L24N_T3_AD15N_35
NET  XADC_GPIO_3          LOC = H18  | IOSTANDARD=LVCMOS25; # Bank 35  VCCO - VADJ - IO_25_35
#NET  PS_CLK               LOC = F7   ; # Bank 500 - PS_CLK_500
#NET  8N2                  LOC = F8   ; # Bank 501 - PS_MIO_VREF_501
#NET  PS_POR_B             LOC = B5   ; # Bank 500 - PS_POR_B_500
#NET  SDIO_SDWP            LOC = E6   ; # Bank 500 - PS_MIO15_500
#NET  PHY_TXD0             LOC = E9   ; # Bank 501 - PS_MIO17_501
#NET  PHY_TXD2             LOC = E10  ; # Bank 501 - PS_MIO19_501
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#NET  PHY_TX_CTRL          LOC = F11  ; # Bank 501 - PS_MIO21_501
#NET  PHY_RXD0             LOC = E11  ; # Bank 501 - PS_MIO23_501
#NET  PHY_RXD2             LOC = F12  ; # Bank 501 - PS_MIO25_501
#NET  PHY_RX_CTRL          LOC = D7   ; # Bank 501 - PS_MIO27_501
#NET  USB_DIR              LOC = E8   ; # Bank 501 - PS_MIO29_501
#NET  USB_NXT              LOC = F9   ; # Bank 501 - PS_MIO31_501
#NET  USB_DATA1            LOC = G13  ; # Bank 501 - PS_MIO33_501
#NET  USB_DATA3            LOC = F14  ; # Bank 501 - PS_MIO35_501
#NET  USB_DATA6            LOC = F13  ; # Bank 501 - PS_MIO38_501
#NET  SDIO_CLK_LS          LOC = E14  ; # Bank 501 - PS_MIO40_501
#NET  SDIO_DAT0_LS         LOC = D8   ; # Bank 501 - PS_MIO42_501
#NET  SDIO_DAT2_LS         LOC = E13  ; # Bank 501 - PS_MIO44_501
#NET  CAN_RXD_LS           LOC = D12  ; # Bank 501 - PS_MIO46_501
#NET  USB_UART_RX          LOC = D11  ; # Bank 501 - PS_MIO48_501
#NET  PS_SCL_MAIN          LOC = D13  ; # Bank 501 - PS_MIO50_501
#NET  PHY_MDC              LOC = D10  ; # Bank 501 - PS_MIO52_501
#NET  PS_SRST_B            LOC = C9   ; # Bank 501 - PS_SRST_B_501
#NET  PS_DIP_SW0           LOC = B6   ; # Bank 500 - PS_MIO14_500
#NET  PHY_TX_CLK           LOC = D6   ; # Bank 501 - PS_MIO16_501
#NET  PHY_TXD1             LOC = A7   ; # Bank 501 - PS_MIO18_501
#NET  PHY_TXD3             LOC = A8   ; # Bank 501 - PS_MIO20_501
#NET  PHY_RX_CLK           LOC = A14  ; # Bank 501 - PS_MIO22_501
#NET  PHY_RXD1             LOC = B7   ; # Bank 501 - PS_MIO24_501
#NET  PHY_RXD3             LOC = A13  ; # Bank 501 - PS_MIO26_501
#NET  USB_DATA4            LOC = A12  ; # Bank 501 - PS_MIO28_501
#NET  USB_STP              LOC = A11  ; # Bank 501 - PS_MIO30_501
#NET  USB_DATA0            LOC = C7   ; # Bank 501 - PS_MIO32_501
#NET  USB_DATA2            LOC = B12  ; # Bank 501 - PS_MIO34_501
#NET  USB_CLKOUT           LOC = A9   ; # Bank 501 - PS_MIO36_501
#NET  USB_DATA5            LOC = B14  ; # Bank 501 - PS_MIO37_501
#NET  USB_DATA7            LOC = C13  ; # Bank 501 - PS_MIO39_501
#NET  SDIO_CMD_LS          LOC = C8   ; # Bank 501 - PS_MIO41_501
#NET  SDIO_DAT1_LS         LOC = B11  ; # Bank 501 - PS_MIO43_501
#NET  SDIO_CD_DAT3_LS      LOC = B9   ; # Bank 501 - PS_MIO45_501
#NET  CAN_TXD_LS           LOC = B10  ; # Bank 501 - PS_MIO47_501
#NET  USB_UART_TX          LOC = C14  ; # Bank 501 - PS_MIO49_501
#NET  PS_SDA_MAIN          LOC = C10  ; # Bank 501 - PS_MIO51_501
#NET  PHY_MDIO             LOC = C12  ; # Bank 501 - PS_MIO53_501
#NET  IIC_MUX_RESET_B_LS   LOC = A6   ; # Bank 500 - PS_MIO13_500
#NET  PS_DIP_SW1           LOC = C5   ; # Bank 500 - PS_MIO12_500
#NET  PHY_RESET_B_AND      LOC = B4   ; # Bank 500 - PS_MIO11_500
#NET  PS_LED1              LOC = G7   ; # Bank 500 - PS_MIO10_500
#NET  CAN_STB_B_LS         LOC = C4   ; # Bank 500 - PS_MIO9_500
#NET  PS_MIO8_LED0         LOC = E5   ; # Bank 500 - PS_MIO8_500
#NET  USB_RESET_B_AND      LOC = D5   ; # Bank 500 - PS_MIO7_500
#NET  QSPI_CLK             LOC = A4   ; # Bank 500 - PS_MIO6_500
#NET  QSPI_IO3             LOC = A3   ; # Bank 500 - PS_MIO5_500
#NET  QSPI_IO2             LOC = E4   ; # Bank 500 - PS_MIO4_500
#NET  QSPI_IO1             LOC = F6   ; # Bank 500 - PS_MIO3_500
#NET  QSPI_IO0             LOC = A2   ; # Bank 500 - PS_MIO2_500
#NET  QSPI_CS_B            LOC = A1   ; # Bank 500 - PS_MIO1_500
#NET  SDIO_SDDET           LOC = G6   ; # Bank 500 - PS_MIO0_500
#NET  PS_DDR3_RESET_B      LOC = F3   ; # Bank 502 - PS_DDR_DRST_B_502
#NET  PS_DDR3_DQ3          LOC = D1   ; # Bank 502 - PS_DDR_DQ0_502
#NET  PS_DDR3_DQ1          LOC = C3   ; # Bank 502 - PS_DDR_DQ1_502
#NET  PS_DDR3_DQ6          LOC = B2   ; # Bank 502 - PS_DDR_DQ2_502
#NET  PS_DDR3_DQ7          LOC = D3   ; # Bank 502 - PS_DDR_DQ3_502
#NET  PS_DDR3_DM0          LOC = B1   ; # Bank 502 - PS_DDR_DM0_502
#NET  PS_DDR3_DQS0_P       LOC = C2   ; # Bank 502 - PS_DDR_DQS_P0_502
#NET  PS_DDR3_DQS0_N       LOC = D2   ; # Bank 502 - PS_DDR_DQS_N0_502
#NET  PS_DDR3_DQ0          LOC = E3   ; # Bank 502 - PS_DDR_DQ4_502
#NET  PS_DDR3_DQ5          LOC = E1   ; # Bank 502 - PS_DDR_DQ5_502
#NET  PS_DDR3_DQ2          LOC = F2   ; # Bank 502 - PS_DDR_DQ6_502
#NET  PS_DDR3_DQ4          LOC = F1   ; # Bank 502 - PS_DDR_DQ7_502
#NET  PS_DDR3_DQ8          LOC = G2   ; # Bank 502 - PS_DDR_DQ8_502
#NET  PS_DDR3_DQ10         LOC = G1   ; # Bank 502 - PS_DDR_DQ9_502
#NET  PS_DDR3_DQ9          LOC = L1   ; # Bank 502 - PS_DDR_DQ10_502
#NET  PS_DDR3_DQ13         LOC = L2   ; # Bank 502 - PS_DDR_DQ11_502
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#NET  PS_DDR3_DM1          LOC = H3   ; # Bank 502 - PS_DDR_DM1_502
#NET  PS_DDR3_DQS1_P       LOC = H2   ; # Bank 502 - PS_DDR_DQS_P1_502
#NET  PS_DDR3_DQS1_N       LOC = J2   ; # Bank 502 - PS_DDR_DQS_N1_502
#NET  PS_DDR3_DQ12         LOC = L3   ; # Bank 502 - PS_DDR_DQ12_502
#NET  PS_DDR3_DQ11         LOC = K1   ; # Bank 502 - PS_DDR_DQ13_502
#NET  PS_DDR3_DQ14         LOC = J1   ; # Bank 502 - PS_DDR_DQ14_502
#NET  PS_DDR3_DQ15         LOC = K3   ; # Bank 502 - PS_DDR_DQ15_502
#NET  PS_DDR3_A14          LOC = G4   ; # Bank 502 - PS_DDR_A14_502
#NET  PS_DDR3_A13          LOC = F4   ; # Bank 502 - PS_DDR_A13_502
#NET  PS_DDR3_A12          LOC = H4   ; # Bank 502 - PS_DDR_A12_502
#NET  PS_DDR3_A11          LOC = G5   ; # Bank 502 - PS_DDR_A11_502
#NET  PS_DDR3_A10          LOC = J3   ; # Bank 502 - PS_DDR_A10_502
#NET  PS_DDR3_A9           LOC = H5   ; # Bank 502 - PS_DDR_A9_502
#NET  PS_DDR3_A8           LOC = J5   ; # Bank 502 - PS_DDR_A8_502
#NET  PS_DDR3_A7           LOC = J6   ; # Bank 502 - PS_DDR_A7_502
#NET  PS_DDR3_A6           LOC = J7   ; # Bank 502 - PS_DDR_A6_502
#NET  PS_DDR3_A5           LOC = K5   ; # Bank 502 - PS_DDR_A5_502
#NET  PS_DDR3_A4           LOC = K6   ; # Bank 502 - PS_DDR_A4_502
#NET  PS_DDR3_A3           LOC = L4   ; # Bank 502 - PS_DDR_A3_502
#NET  PS_VRN               LOC = M7   ; # Bank 502 - PS_DDR_VRN_502
#NET  PS_VRP               LOC = N7   ; # Bank 502 - PS_DDR_VRP_502
#NET  PS_DDR3_CLK_P        LOC = N4   ; # Bank 502 - PS_DDR_CKP_502
#NET  PS_DDR3_CLK_N        LOC = N5   ; # Bank 502 - PS_DDR_CKN_502
#NET  PS_DDR3_A2           LOC = K4   ; # Bank 502 - PS_DDR_A2_502
#NET  PS_DDR3_A1           LOC = M5   ; # Bank 502 - PS_DDR_A1_502
#NET  PS_DDR3_A0           LOC = M4   ; # Bank 502 - PS_DDR_A0_502
#NET  PS_DDR3_BA2          LOC = M6   ; # Bank 502 - PS_DDR_BA2_502
#NET  PS_DDR3_BA1          LOC = L6   ; # Bank 502 - PS_DDR_BA1_502 = 1.5v
#NET  PS_DDR3_BA0          LOC = L7   ; # Bank 502 - PS_DDR_BA0_502
#NET  PS_DDR3_ODT          LOC = P5   ; # Bank 502 - PS_DDR_ODT_502
#NET  PS_DDR3_CS_B         LOC = P6   ; # Bank 502 - PS_DDR_CS_B_502
#NET  PS_DDR3_CKE          LOC = V3   ; # Bank 502 - PS_DDR_CKE_502
#NET  PS_DDR3_WE_B         LOC = R4   ; # Bank 502 - PS_DDR_WE_B_502
#NET  PS_DDR3_CAS_B        LOC = P3   ; # Bank 502 - PS_DDR_CAS_B_502
#NET  PS_DDR3_RAS_B        LOC = R5   ; # Bank 502 - PS_DDR_RAS_B_502
#NET  PS_DDR3_DQ16         LOC = M1   ; # Bank 502 - PS_DDR_DQ16_502
#NET  PS_DDR3_DQ17         LOC = T3   ; # Bank 502 - PS_DDR_DQ17_502
#NET  PS_DDR3_DQ18         LOC = N3   ; # Bank 502 - PS_DDR_DQ18_502
#NET  PS_DDR3_DQ19         LOC = T1   ; # Bank 502 - PS_DDR_DQ19_502
#NET  PS_DDR3_DM2          LOC = P1   ; # Bank 502 - PS_DDR_DM2_502
#NET  PS_DDR3_DQS2_P       LOC = N2   ; # Bank 502 - PS_DDR_DQS_P2_502
#NET  PS_DDR3_DQS2_N       LOC = P2   ; # Bank 502 - PS_DDR_DQS_N2_502
#NET  PS_DDR3_DQ20         LOC = R3   ; # Bank 502 - PS_DDR_DQ20_502
#NET  PS_DDR3_DQ21         LOC = T2   ; # Bank 502 - PS_DDR_DQ21_502
#NET  PS_DDR3_DQ22         LOC = M2   ; # Bank 502 - PS_DDR_DQ22_502
#NET  PS_DDR3_DQ23         LOC = R1   ; # Bank 502 - PS_DDR_DQ23_502
#NET  PS_DDR3_DQ27         LOC = AA3  ; # Bank 502 - PS_DDR_DQ24_502
#NET  PS_DDR3_DQ24         LOC = U1   ; # Bank 502 - PS_DDR_DQ25_502
#NET  PS_DDR3_DQ25         LOC = AA1  ; # Bank 502 - PS_DDR_DQ26_502
#NET  PS_DDR3_DQ26         LOC = U2   ; # Bank 502 - PS_DDR_DQ27_502
#NET  PS_DDR3_DM3          LOC = AA2  ; # Bank 502 - PS_DDR_DM3_502
#NET  PS_DDR3_DQS3_P       LOC = V2   ; # Bank 502 - PS_DDR_DQS_P3_502
#NET  PS_DDR3_DQS3_N       LOC = W2   ; # Bank 502 - PS_DDR_DQS_N3_502
#NET  PS_DDR3_DQ28         LOC = W1   ; # Bank 502 - PS_DDR_DQ28_502
#NET  PS_DDR3_DQ29         LOC = Y3   ; # Bank 502 - PS_DDR_DQ29_502
#NET  PS_DDR3_DQ30         LOC = W3   ; # Bank 502 - PS_DDR_DQ30_502
#NET  PS_DDR3_DQ31         LOC = Y1   ; # Bank 502 - PS_DDR_DQ31_502
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Board Specifications

Dimensions

Width: 7.750 in. (19.685 cm)

Length: 7.150 in. (18.161 cm)

Environmental

Temperature

Operating: 0°C to +45°C

Storage: –25°C to +60°C

Humidity

10% to 90% non-condensing

Operating Voltage

+12 V_{DC}

Appendix E

Additional Resources

Xilinx Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see the Xilinx Support website at:

www.xilinx.com/support.

For continual updates, add the Answer Record to your myAlerts:

www.xilinx.com/support/myalerts.

For a glossary of technical terms used in Xilinx documentation, see:

www.xilinx.com/company/terms.htm.

Solution Centers

See the Xilinx Solution Centers for support on devices, software tools, and intellectual property at all stages of the design cycle. Topics include design assistance, advisories, and troubleshooting tips.

Further Resources

The most up to date information related to the ZC702 board and its documentation is available on the following websites.

The Xilinx Zynq-7000 AP SoC ZC702 Evaluation Kit product page:

www.xilinx.com/products/boards-and-kits/EK-Z7-ZC702-G.htm

The Zynq-7000 AP SoC ZC702 Evaluation Kit - Known Issues and Release Notes Master Answer Record:

www.xilinx.com/support/answers/47864.htm

These Xilinx documents provide supplemental material useful with this guide:

DS190, *Zynq-7000 All Programmable SoC Overview*

DS187, *Zynq-7000 All Programmable SoC (XC7Z010 and XC7Z020): DC and AC Switching Characteristics*

UG138, *LogiCORE IP Tri-Mode Ethernet MAC v4.5 User Guide*

UG470, *7 Series FPGAs Configuration User Guide*

UG473, *7 Series FPGAs Memory Resources User Guide*

UG476, *7 Series FPGAs GTX/GTH Transceivers User Guide*

UG477, *7 Series FPGAs Integrated Block for PCI Express User Guide*

UG480, *7 Series FPGAs XADC Dual 12-Bit 1MSPS Analog-to-Digital Converter User Guide*

UG585, *Zynq-7000 All Programmable SoC Technical Reference Manual*

UG586, *7 Series FPGAs Memory Interface Solutions v1.8 User Guide*

UG865, *Zynq-7000 All Programmable SoC Packaging and Pinout User Guide*

UG886, *AMS101 Evaluation Card User Guide*

UG933, *Zynq-7000 All Programmable SoC PCB Design and Pin Planning Guide*

References

The following websites provide supplemental material useful with this guide:

1. Micron Semiconductor: www.micron.com
   (Numonyx N25Q128A11ESF40G)
2. Standard Microsystems Corporation: www.smsc.com/
   (USB3320)
3. SanDisk Corporation: www.sandisk.com
4. SD Association: www.sdcard.org
5. SiTime: www.sitime.com
   (SiT9102)
6. Silicon Labs: www.silabs.com
   (Si570, Si5324C)

7. Marvell Semiconductor: www.marvell.com
(88E1116R)

8. Analog Devices: www.analog.com/en/index.html
(ADV7511KSTZ-P, ADP123)

9. Epson Electronics America: www.eea.epson.com and
www.eea.epson.com/portal/pls/portal/docs/1/1413485.PDF
(RTC-8564JE)

10. Digilent: www.digilentinc.com and
www.digilentinc.com/Products/Catalog.cfm?NavPath=2,401&Cat=9
(Pmod Peripheral Modules)

11. NXP Semiconductors: ics.nxp.com
(TJA01040)

12. Texas Instruments: www.ti.com, www.ti.com/fusiondocs, and
www.ti.com/ww/en/analog/digital-power/index.html
(UCD9248PFC, PTD08A010W, PTD08A020W, PTD08D210W, LMZ12002, TL1962ADC, TPS51200DR, PCA9548)

13. Samtec: www.samtec.com.
(SEAF series connectors)

14. Integrated Device Technology: www.idt.com
(ICS844021I)

Regulatory and Compliance Information

This product is designed and tested to conform to the European Union directives and standards described in this section.

Refer to the ZC702 board master answer record concerning the CE requirements for the PC Test Environment:

www.xilinx.com/support/answers/47864.htm

Declaration of Conformity

To view the Declaration of Conformity online, visit:

www.xilinx.com/support/documentation/boards_and_kits/ce-declarations-of-conformity-xtp251.zip

Directives

2006/95/EC, *Low Voltage Directive (LVD)*

2004/108/EC, *Electromagnetic Compatibility (EMC) Directive*

Standards

EN standards are maintained by the European Committee for Electrotechnical Standardization (CENELEC). IEC standards are maintained by the International Electrotechnical Commission (IEC).

Electromagnetic Compatibility

EN 55022:2010, *Information Technology Equipment Radio Disturbance Characteristics – Limits and Methods of Measurement*

EN 55024:2010, *Information Technology Equipment Immunity Characteristics – Limits and Methods of Measurement*

This is a Class A product. In a domestic environment, this product can cause radio interference, in which case the user might be required to take adequate measures.

Safety

IEC 60950-1:2005, *Information technology equipment – Safety, Part 1: General requirements*

EN 60950-1:2006, *Information technology equipment – Safety, Part 1: General requirements*

Markings

This product complies with Directive 2002/96/EC on waste electrical and electronic equipment (WEEE). The affixed product label indicates that the user must not discard this electrical or electronic product in domestic household waste.

This product complies with Directive 2002/95/EC on the restriction of hazardous substances (RoHS) in electrical and electronic equipment.

This product complies with CE Directives 2006/95/EC, *Low Voltage Directive (LVD)* and 2004/108/EC, *Electromagnetic Compatibility (EMC) Directive*.