Window Comparator for Over- and Undervoltage Detection

Check for Samples: TPS3700

FEATURES

- **Wide Supply Voltage Range: 1.8 V to 18 V**
- **Adjustable Threshold: Down to 400 mV**
- **Open-Drain Outputs for Over- and Undervoltage Detection**
- **Low Quiescent Current: 5.5 µA (typ)**
- **High Threshold Accuracy:**
  - **1.0% Over Temperature**
  - **0.25% (typ)**
- **Internal Hysteresis: 5.5 mV (typ)**
- **Temperature Range: –40°C to +125°C**
- **Packages:**
  - **ThinSOT23-6**
  - **1,5-mm × 1,5-mm SON-6**

APPLICATIONS

- **Industrial Control Systems**
- **Automotive Systems**
- **Embedded Computing Modules**
- **DSP, Microcontroller, or Microprocessor Applications**
- **Notebook and Desktop Computers**
- **Portable- and Battery-Powered Products**
- **FPGA and ASIC Applications**

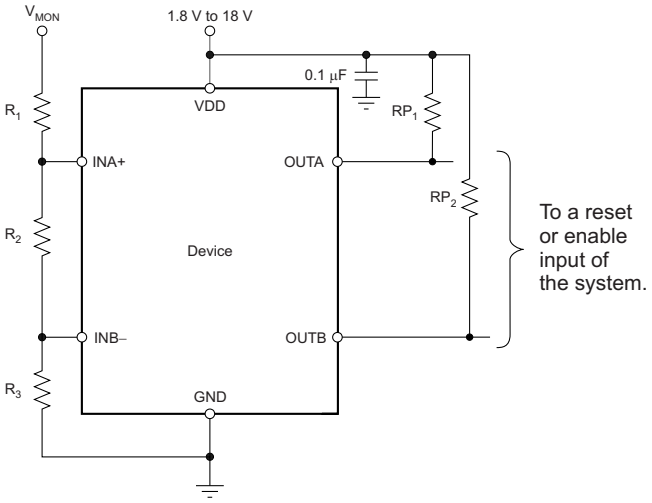


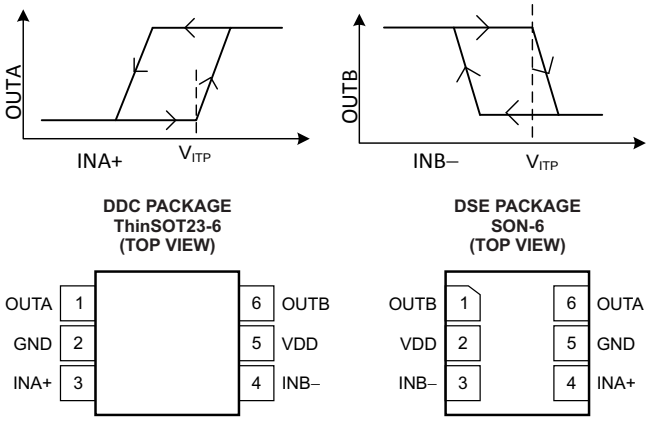
Figure 1. TPS3700 Typical Application

DESCRIPTION

The TPS3700 wide-supply voltage window comparator operates over a 1.8-V to 18-V range. The device has two high-accuracy comparators with an internal 400-mV reference and two open-drain outputs rated to 18 V for over- and undervoltage detection. The TPS3700 can be used as a window comparator or as two independent voltage monitors; the monitored voltage can be set with the use of external resistors.

OUTA is driven low when the voltage at INA+ drops below (V_{ITP} – V_{HYS}), and goes high when the voltage returns above the respective threshold (V_{ITP}). OUTB is driven low when the voltage at INB– rises above V_{ITP}, and goes high when the voltage drops below the respective threshold (V_{ITP} – V_{HYS}). Both comparators in the TPS3700 include built-in hysteresis for filtering to reject brief glitches, thereby ensuring stable output operation without false triggering.

The TPS3700 is available in a ThinSOT23-6 and a 1,5-mm × 1,5-mm SON-6 package and is specified over the junction temperature range of –40°C to +125°C.



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	DESCRIPTION
TPS3700**yyyz**	**yyy** is package designator **z** is package quantity

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range, unless otherwise noted.

		VALUE		UNIT
		MIN	MAX	
Voltage(2)	VDD	–0.3	+20	V
	V_{OUTA}, V_{OUTB}	–0.3	+20	V
	V_{INA+}, $V_{INB–}$	–0.3	+7	V
Current	Output pin current		40	mA
Temperature	Operating junction, T_J	–40	+125	°C
	Storage, T_{stg}	–65	+150	°C
Electrostatic discharge (ESD) rating(3)	Human body model (HBM)		2	kV
	Charge device model (CDM)		500	V

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods my affect device reliability.
(2) All voltages are with respect to network ground terminal.
(3) ESD testing is performed according to the respective JESD22 JEDEC standard.

THERMAL INFORMATION

THERMAL METRIC(1)		TPS3700		UNITS
		DDC (SOT23)	DSE (SON6)	
		6 PINS	6 PINS	
θ_{JA}	Junction-to-ambient thermal resistance	204.6	194.9	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	50.5	128.9	
θ_{JB}	Junction-to-board thermal resistance	54.3	153.8	
ψ_{JT}	Junction-to-top characterization parameter	0.8	11.9	
ψ_{JB}	Junction-to-board characterization parameter	52.8	157.4	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	N/A	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

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ELECTRICAL CHARACTERISTICS

Over the operating temperature range of T_J = –40°C to +125°C, and 1.8 V < V_{DD} < 18 V, unless otherwise noted. Typical values are at T_J = +25°C and V_{DD} = 5 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{DD}	Supply voltage range		1.8		18	V
$V_{(POR)}$	Power-on reset voltage(1)	V_{OL} (max) = 0.2 V, $I_{(OUT)}$ = 15 µA			0.8	V
V_{ITP}	Positive-going input threshold voltage	V_{DD} = 1.8 V	396	400	404	mV
		V_{DD} = 18 V	396	400	404	mV
V_{ITN}	Negative-going input threshold voltage	V_{DD} = 1.8 V	387	394.5	400	mV
		V_{DD} = 18 V	387	394.5	400	mV
V_{HYS}	Hysteresis voltage (HYS = V_{ITP} – V_{ITN})			5.5	12	mV
I_{IN}	Input current (at IN pin)	V_{DD} = 1.8 V and 18 V, V_{IN} = 6.5 V	–25	1	25	nA
		V_{DD} = 1.8 V and 18 V, V_{IN} = 0.1 V	–15	1	15	nA
V_{OL}	Low-level output voltage	V_{DD} = 1.3 V, I_{OUT} = 0.4 mA			250	mV
		V_{DD} = 1.8 V, I_{OUT} = 3 mA			250	mV
		V_{DD} = 5 V, I_{OUT} = 5 mA			250	mV
$I_{lkg(OD)}$	Open-drain output leakage current	V_{DD} = 1.8 V and 18 V, V_{OUT} = V_{DD}			300	nA
		V_{DD} = 1.8 V, V_{OUT} = 18 V			300	nA
$t_{pd(HL)}$	High-to-low propagation delay(2)	V_{DD} = 5 V, 10-mV input overdrive, R_L = 10 kΩ, V_{OH} = 0.9 × V_{DD}, V_{OL} = 400 mV		18		µs
$t_{pd(LH)}$	Low-to-high propagation delay(2)	V_{DD} = 5 V, 10-mV input overdrive, R_L = 10 kΩ, V_{OH} = 0.9 × V_{DD}, V_{OL} = 400 mV		29		µs
t_R	Output rise time	V_{DD} = 5 V, 10-mV input overdrive, R_L = 10 kΩ, V_O = (0.1 to 0.9) × V_{DD}		2.2		µs
t_F	Output fall time	V_{DD} = 5 V, 10-mV input overdrive, R_L = 10 kΩ, V_O = (0.1 to 0.9) × V_{DD}		0.22		µs
I_{DD}	Supply current	V_{DD} = 1.8 V, no load		5.5	11	µA
		V_{DD} = 5 V		6	13	µA
		V_{DD} = 12 V		6	13	µA
		V_{DD} = 18 V		7	13	µA
	Startup delay(3)			150		µs
UVLO	Undervoltage lockout(4)	V_{DD} falling	1.3		1.7	V

(1) The lowest supply voltage (V_{DD}) at which output is active; $t_{r(VDD)}$ > 15 µs/V. Below $V_{(POR)}$, the output cannot be determined.
(2) High-to-low and low-to-high refers to the transition at the input pins (INA+ and INB–).
(3) During power on, V_{DD} must exceed 1.8 V for at least 150 µs before the output is in a correct state.
(4) When V_{DD} falls below UVLO, OUTA is driven low and OUTB goes to high impedance. The outputs cannot be determined below $V_{(POR)}$.

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PARAMETRIC MEASUREMENT INFORMATION

TIMING DIAGRAM

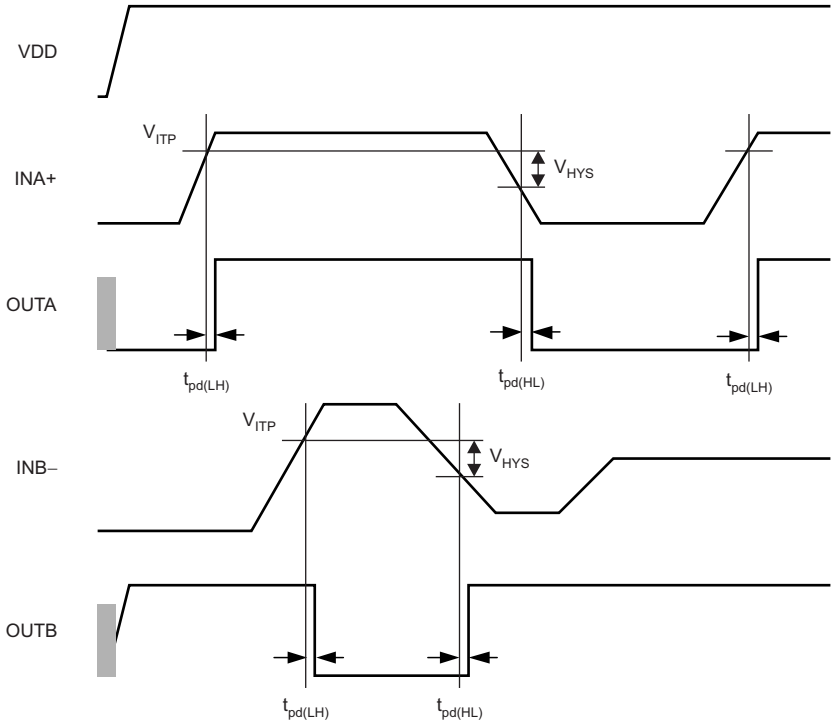

Figure 2. TPS3700 Timing Diagram

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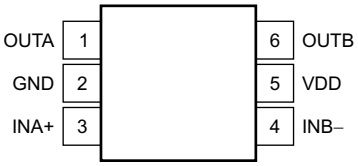
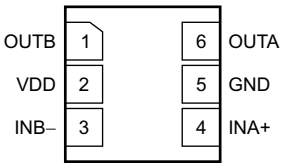
PIN CONFIGURATIONS

DDC PACKAGE
ThinSOT23-6
(TOP VIEW)



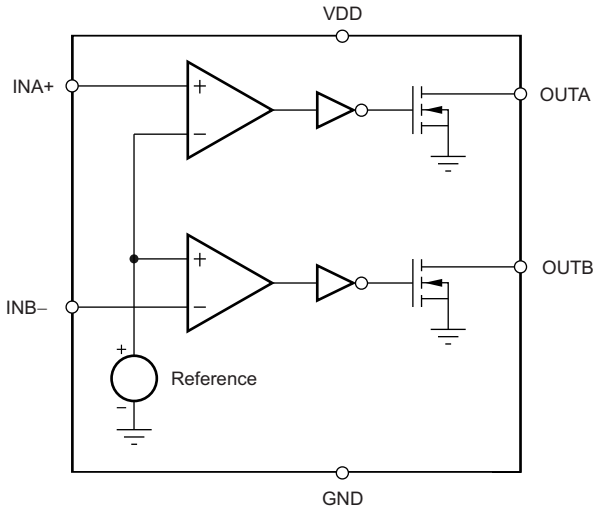
DSE PACKAGE
SON-6
(TOP VIEW)



PIN ASSIGNMENTS

PIN NAME	PIN NO.		DESCRIPTION
	DDC	DSE	
GND	2	5	Ground
INA+	3	4	This pin is connected to the voltage to be monitored with the use of an external resistor divider. When the voltage at this terminal drops below the threshold voltage ($V_{ITP} – V_{HYS}$), OUTA is driven low.
INB–	4	3	This pin is connected to the voltage to be monitored with the use of an external resistor divider. When the voltage at this terminal exceeds the threshold voltage (V_{ITP}), OUTB is driven low.
OUTA	1	6	INA+ comparator open-drain output. OUTA is driven low when the voltage at this comparator is below ($V_{ITP} – V_{HYS}$). The output goes high when the sense voltage returns above the respective threshold (V_{ITP}).
OUTB	6	1	INB– comparator open-drain output. OUTB is driven low when the voltage at this comparator exceeds V_{ITP}. The output goes high when the sense voltage returns below the respective threshold ($V_{ITP} – V_{HYS}$).
VDD	5	2	Supply voltage input. Connect a 1.8-V to 18-V supply to VDD to power the device. It is good analog design practice to place a 0.1-µF ceramic capacitor close to this pin.

BLOCK DIAGRAM



TYPICAL CHARACTERISTICS

At T_J = +25°C and V_{CC} = 5 V, unless otherwise noted.

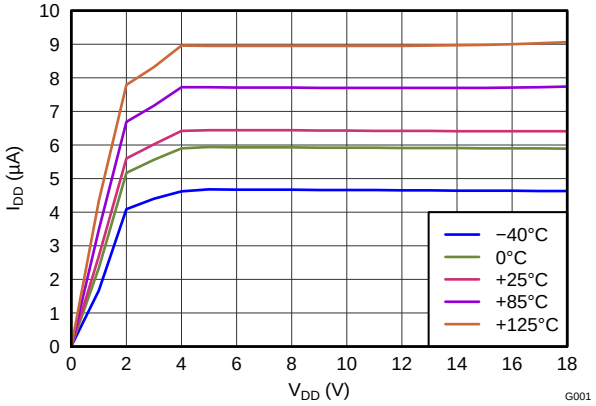


Figure 3.

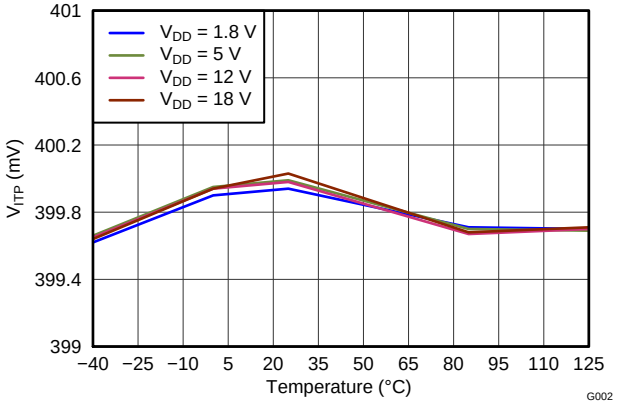


Figure 4.

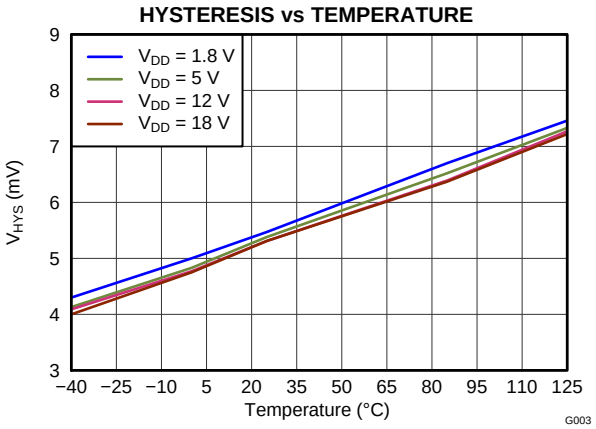


Figure 5.

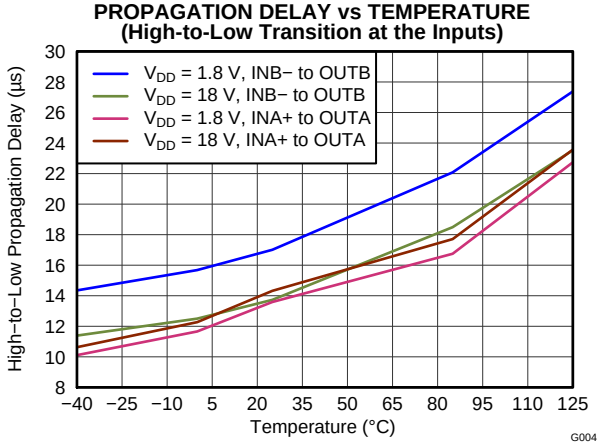


Figure 6.

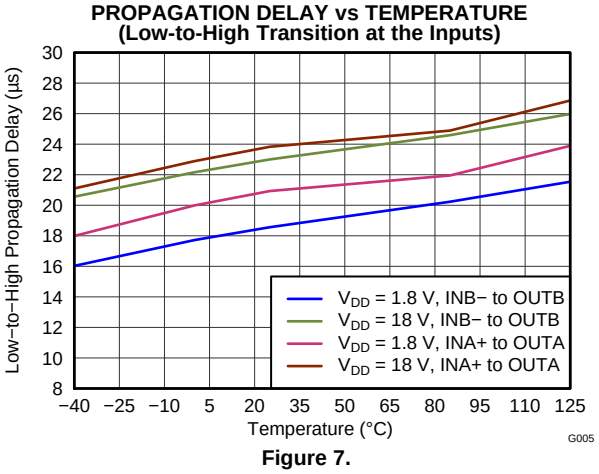


Figure 7.

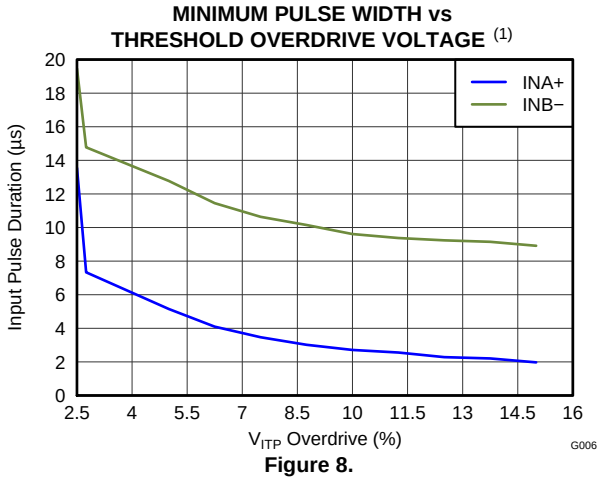


Figure 8.

(1) INA+ = negative spike below V_{ITN} and INB– = positive spike above V_{ITP}.

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TYPICAL CHARACTERISTICS (continued)

At T_J = +25°C and V_{CC} = 5 V, unless otherwise noted.

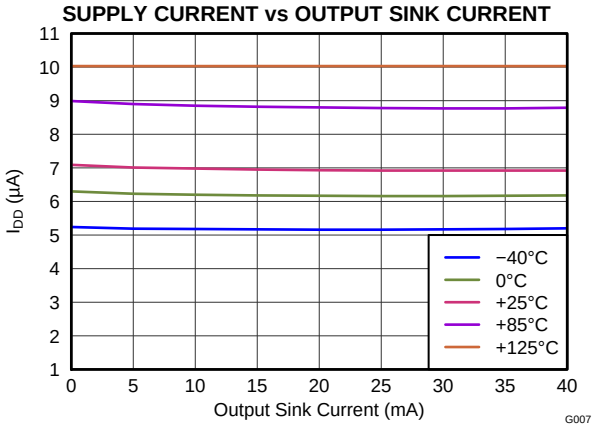

Figure 9.

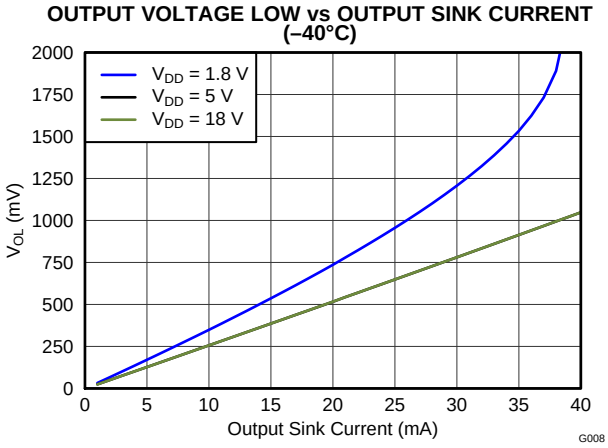

Figure 10.

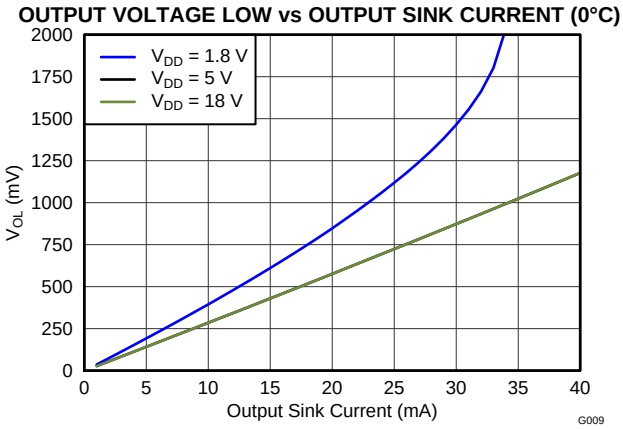

Figure 11.

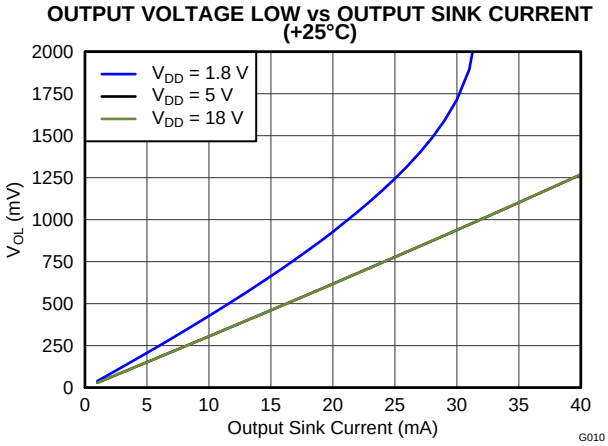

Figure 12.

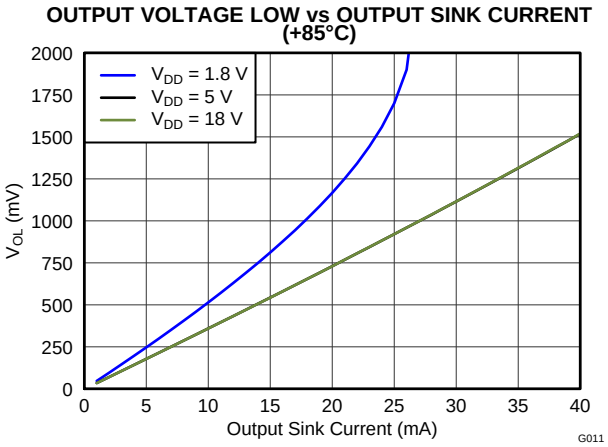

Figure 13.

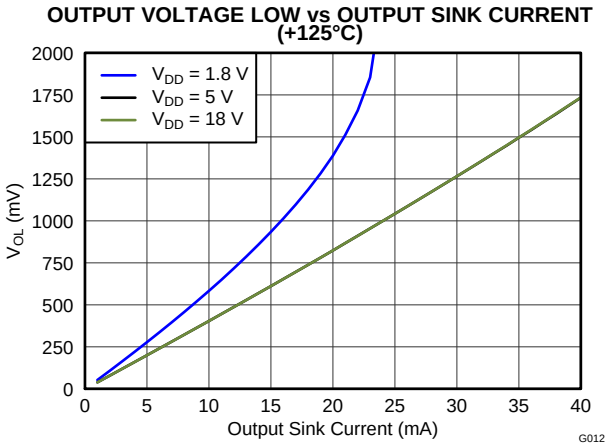

Figure 14.

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TYPICAL CHARACTERISTICS (continued)

At T_J = +25°C and V_{CC} = 5 V, unless otherwise noted.

STARTUP DELAY
(V_{DD} = 5 V, INA+ = 390 mV, INB– = 410 mV, Outputs Pulled Up to V_{DD})

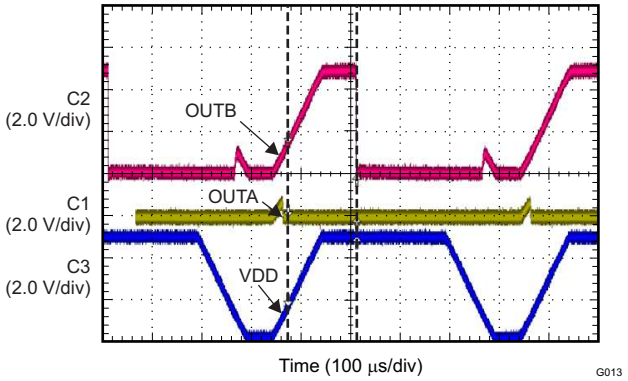

Figure 15.

STARTUP DELAY
(V_{DD} = 5 V, INA+ = 410 mV, INB– = 390 mV, Outputs Pulled Up to V_{DD})

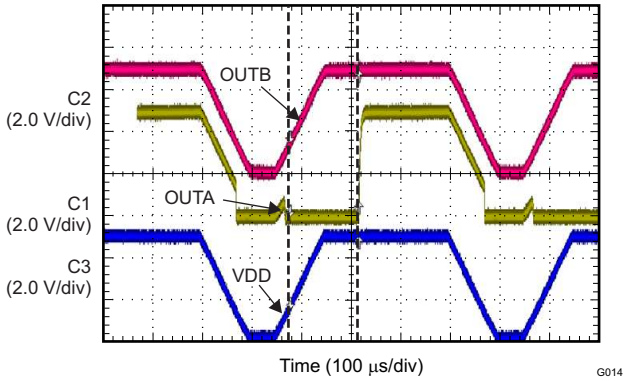

Figure 16.

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GENERAL DESCRIPTION

The TPS3700 combines two comparators for over- and undervoltage detection. The TPS3700 is a wide-supply voltage range (1.8 V to 18 V) device with a high-accuracy rising input threshold of 400 mV (1% over temperature) and built-in hysteresis. The outputs are also rated to 18 V and can sink up to 40 mA.

The TPS3700 is designed to assert the output signals, as shown in Table 1. Each input pin can be set to monitor any voltage above 0.4 V using an external resistor divider network. With the use of two input pins of different polarities, the TPS3700 forms a window comparator. Broad voltage thresholds can be supported that allow the device to be used in a wide array of applications.

Table 1. TPS3700 Truth Table

CONDITION	OUTPUT	STATUS
INA+ > V_{ITP}	OUTA high	Output A not asserted
INA+ < V_{ITN}	OUTA low	Output A asserted
INB– > V_{ITP}	OUTB low	Output B asserted
INB– < V_{ITN}	OUTB high	Output B not asserted

INPUTS (INA+, INB–)

The TPS3700 combines two comparators. Each comparator has one external input (inverting and noninverting); the other input is connected to the internal reference. The comparator rising threshold is designed and trimmed to be equal to the reference voltage (400 mV). Both comparators also have a built-in falling hysteresis that makes the device immune to supply rail noise and ensures stable operation.

The comparator inputs can swing from ground to 6.5 V, regardless of the device supply voltage used. Although not required in most cases, it is good analog design practice to place a 1-nF to 10-nF bypass capacitor at the comparator input for extremely noisy applications in order to reduce sensitivity to transients and layout parasitics.

For comparator A, the corresponding output (OUTA) is driven to logic low when the input INA+ voltage drops below (V_{ITP} – V_{HYS}). When the voltage exceeds V_{ITP}, the output (OUTA) goes to a high-impedance state; see Figure 2.

For comparator B, the corresponding output (OUTB) is driven to logic low when the voltage at input INB– exceeds V_{ITP}. When the voltage drops below V_{ITP} – V_{HYS} the output (OUTB) goes to a high-impedance state; see Figure 2. Together, these comparators form a window-detection function as discussed in the *Window Comparator* section.

OUTPUTS (OUTA, OUTB)

In a typical TPS3700 application, the outputs are connected to a reset or enable input of the processor [such as a digital signal processor (DSP), central processing unit (CPU), field-programmable gate array (FPGA), or application-specific integrated circuit (ASIC)] or the outputs are connected to the enable input of a voltage regulator [such as a dc-dc or low-dropout regulator (LDO)].

The TPS3700 provides two open-drain outputs (OUTA and OUTB); pull-up resistors must be used to hold these lines high when the output goes to high impedance (not asserted). By connecting pull-up resistors to the proper voltage rails, the outputs can be connected to other devices at correct interface voltage levels. The TPS3700 outputs can be pulled up to 18 V, independent of the device supply voltage. To ensure proper voltage levels, some thought should be given while choosing the pull-up resistor values. The pull-up resistor value is determined by V_{OL}, sink current capability, and output leakage current ($I_{lkg(OD)}$). These values are specified in the Electrical Characteristics table. By using wired-AND logic, OUTA and OUTB can be merged into one logic signal.

Table 1 and the *Inputs* section describe how the outputs are asserted or de-asserted. Refer to Figure 2 for a timing diagram that describes the relationship between threshold voltages and the respective output.

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WINDOW COMPARATOR

The inverting and noninverting configuration of the comparators forms a window-comparator detection circuit using a resistor divider network, as shown in Figure 17 and Figure 18. The input pins can monitor any system voltage above 400 mV with the use of a resistor divider network. INA+ and INB– monitor for undervoltage and overvoltage conditions, respectively.

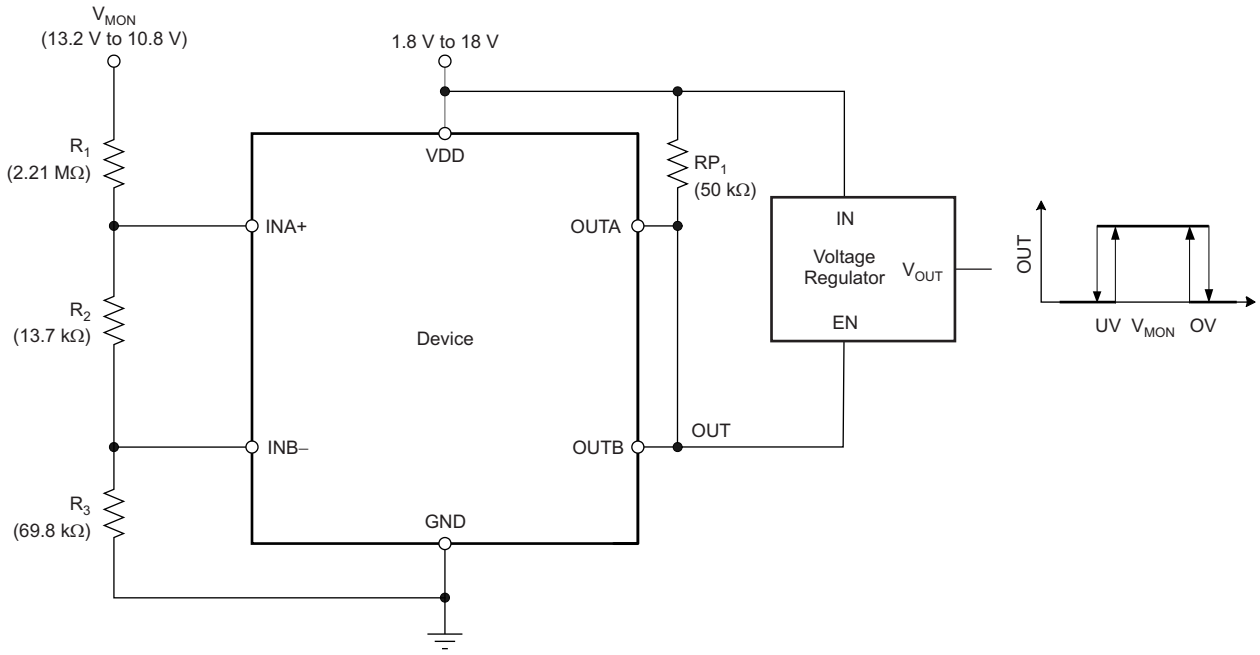

Figure 17. Window Comparator Block Diagram

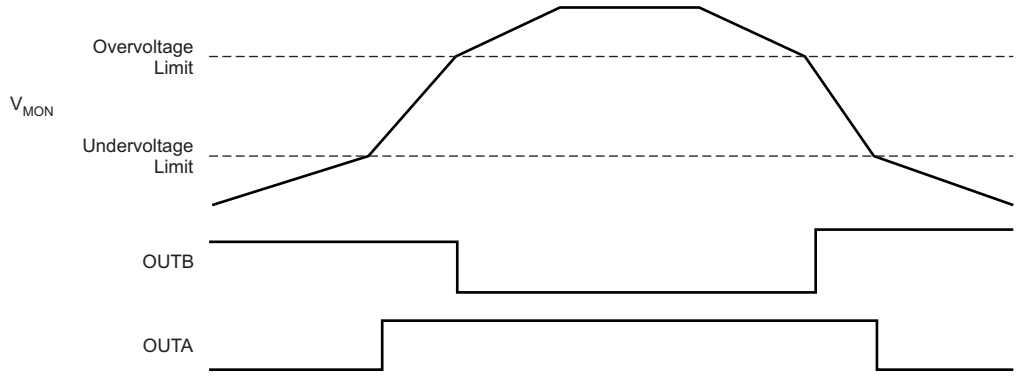

Figure 18. Window Comparator Timing Diagram

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The resistor divider values and target threshold voltage can be calculated by using Equation 1 through Equation 4:

$$R_{TOTAL} = R_1 + R_2 + R_3 \quad (1)$$

Choose R_{TOTAL} such that current through the divider is approximately 100x higher than the input current at the INA+ and INB– pins. The resistors can have high values to minimize current consumption as a result of low input bias current without adding significant error to the resistive divider. Refer to application note *Optimizing Resistor Dividers at a Comparator Input* (SLVA450) for details on sizing input resistors.

R_3 is determined by Equation 2:

$$R_3 = \frac{R_{TOTAL}}{V_{MON(OV)}} \times V_{ITP} \quad (2)$$

where:

$V_{MON(OV)}$ is the target voltage at which an overvoltage condition is detected

R_2 is determined by either Equation 3 or Equation 4:

$$R_2 = \left(\frac{R_{TOTAL}}{V_{MON}\,(\text{no UV})} \times V_{ITP} \right) - R_3 \quad (3)$$

where:

$V_{MON(no\ UV)}$ is the target voltage at which an undervoltage condition is removed as V_{MON} rises

$$R_2 = \left(\frac{R_{TOTAL}}{V_{MON(UV)}} \times (V_{ITP} - V_{HYS}) \right) - R_3 \quad (4)$$

where:

$V_{MON(UV)}$ is the target voltage at which an undervoltage condition is detected

For more application information on the TPS3700, refer to Figure 19 through Figure 22.

IMMUNITY TO INPUT PIN VOLTAGE TRANSIENTS

The TPS3700 is relatively immune to short voltage transient spikes on the input pins. Sensitivity to transients is dependent on both transient duration and amplitude; refer to the Typical Characteristics curve, *Minimum Pulse Width vs Threshold Overdrive Voltage* (Figure 8).

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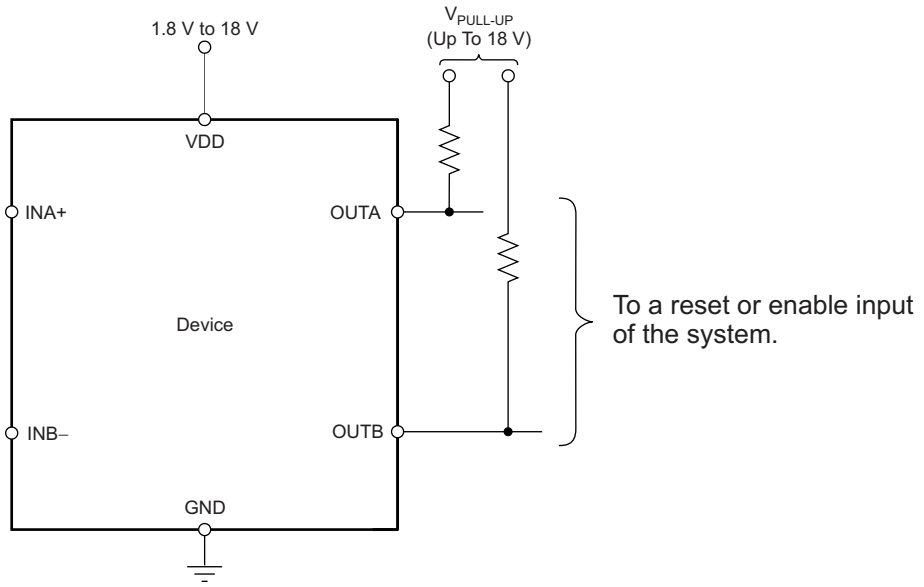

Figure 19. Interfacing to Voltages Other Than V_{DD}

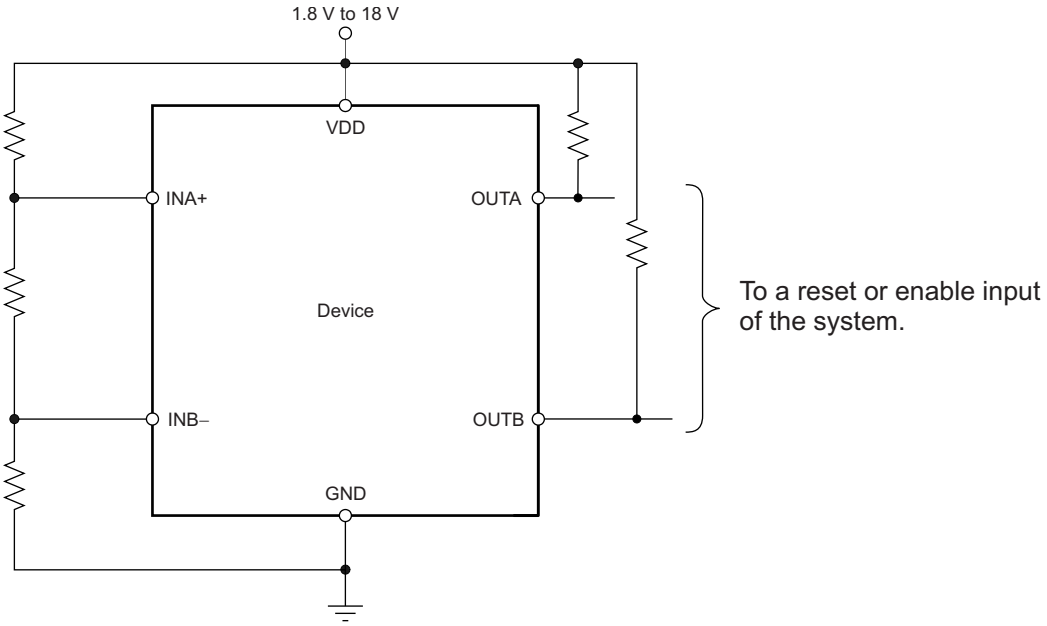

Figure 20. Monitoring the Same Voltage as V_{DD}

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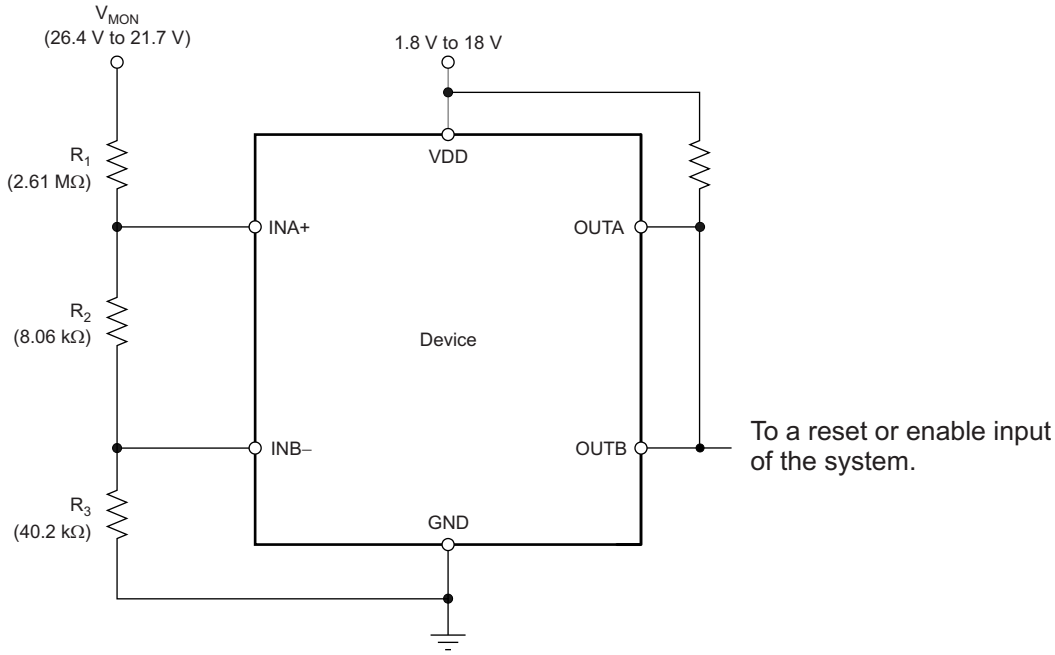
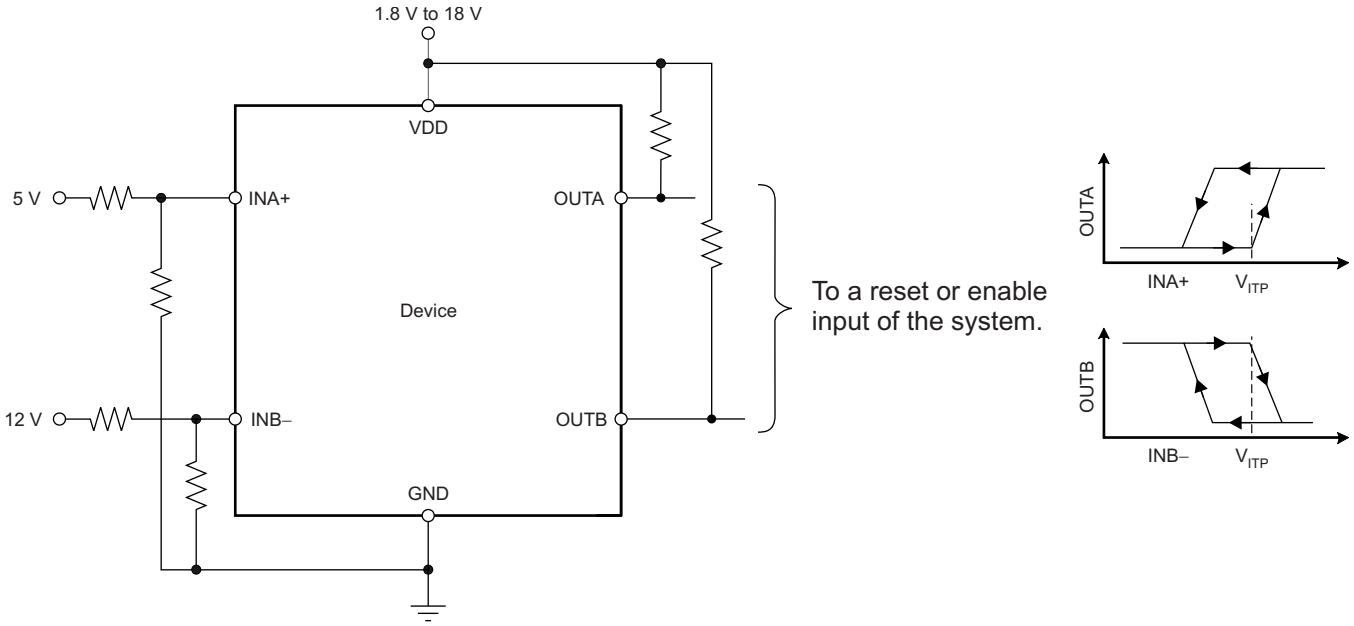


NOTE: The inputs can monitor a voltage higher than V_{DD} (max) with the use of an external resistor divider network.

Figure 21. Monitoring a Voltage Other Than V_{DD}



NOTE: In this case, OUTA is driven low when an undervoltage condition is detected at the 5-V rail and OUTB is driven low when an overvoltage condition is detected at the 12-V rail.

Figure 22. Monitoring Overvoltage for One Rail and Undervoltage for a Different Rail

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REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (April 2012) to Revision C **Page**

- Changed *Packages* Features bullet 1
- Added SON-6 package option to Description section 1
- Added DSE pin out graphic to front page 1
- Added DSE package to Thermal Information table 2
- Added DSE pin out graphic 5

Changes from Revision A (February 2012) to Revision B **Page**

- Moved to Production Data 1

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS3700DDCR	ACTIVE	SOT	DDC	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PXVQ	Samples
TPS3700DDCR2	ACTIVE	SOT	DDC	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PB4Q	Samples
TPS3700DDCT	ACTIVE	SOT	DDC	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PXVQ	Samples
TPS3700DSER	ACTIVE	WSON	DSE	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	BE	Samples
TPS3700DSET	ACTIVE	WSON	DSE	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	BE	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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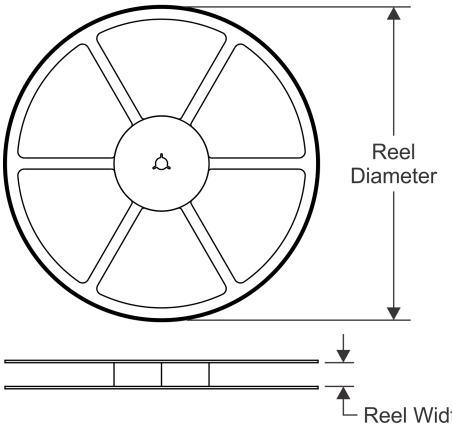
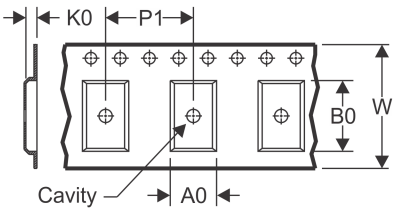
TAPE AND REEL INFORMATION

REEL DIMENSIONS

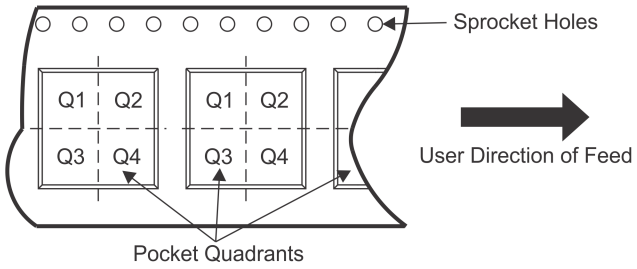


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

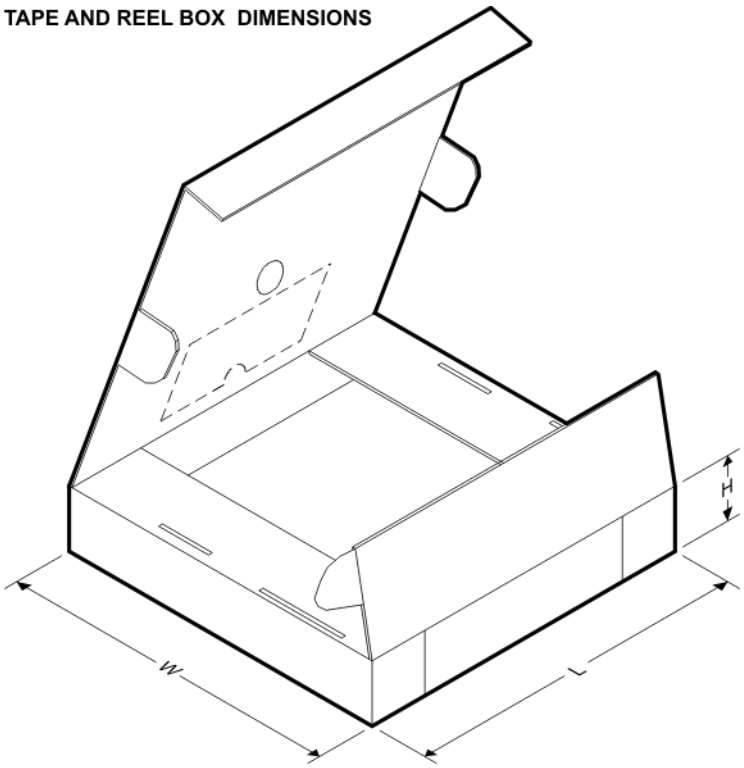
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS3700DDCR	SOT	DDC	6	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3700DDCR2	SOT	DDC	6	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q2
TPS3700DDCT	SOT	DDC	6	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3700DSER	WSON	DSE	6	3000	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2
TPS3700DSET	WSON	DSE	6	250	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2

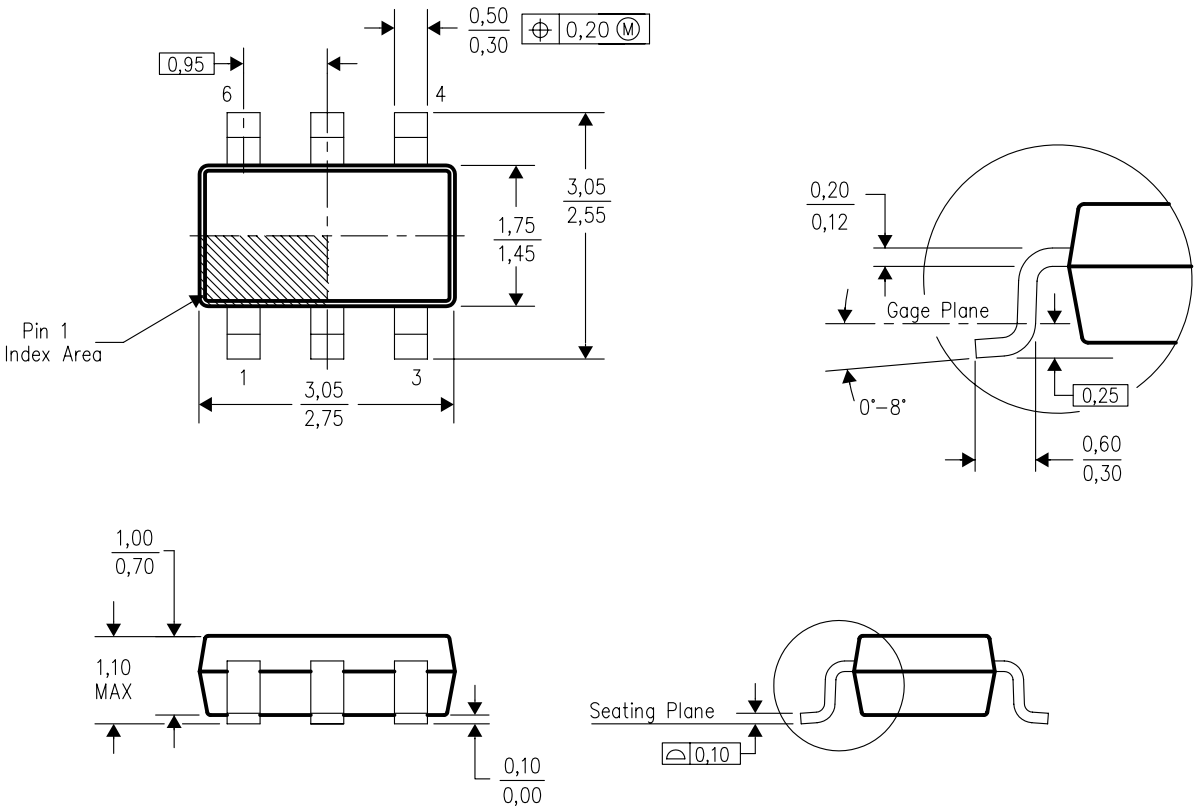
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS3700DDCR	SOT	DDC	6	3000	195.0	200.0	45.0
TPS3700DDCR2	SOT	DDC	6	3000	195.0	200.0	45.0
TPS3700DDCT	SOT	DDC	6	250	195.0	200.0	45.0
TPS3700DSER	WSON	DSE	6	3000	203.0	203.0	35.0
TPS3700DSET	WSON	DSE	6	250	203.0	203.0	35.0

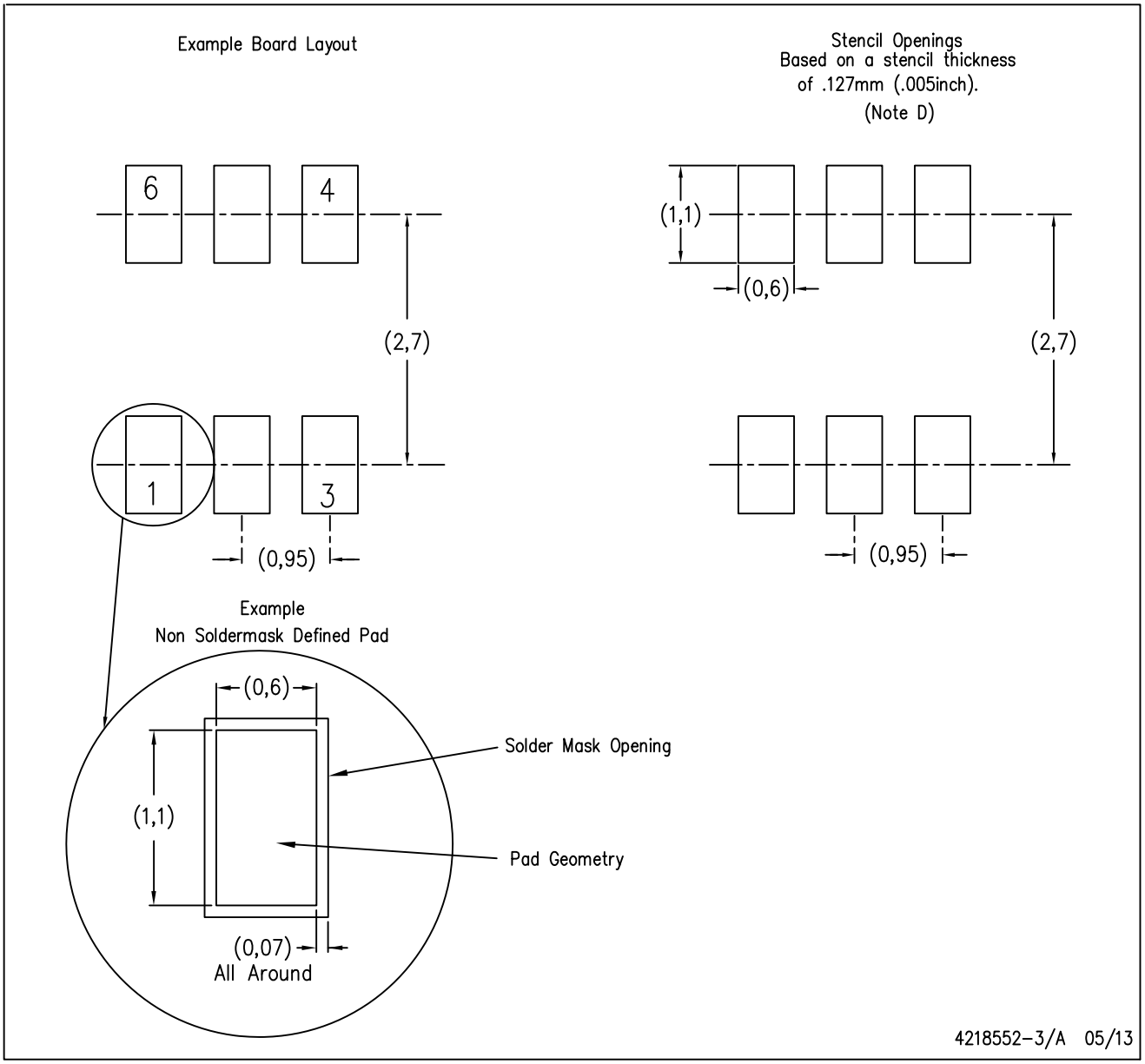
DDC (R–PDSO–G6) PLASTIC SMALL–OUTLINE



4204403–3/E 06/05

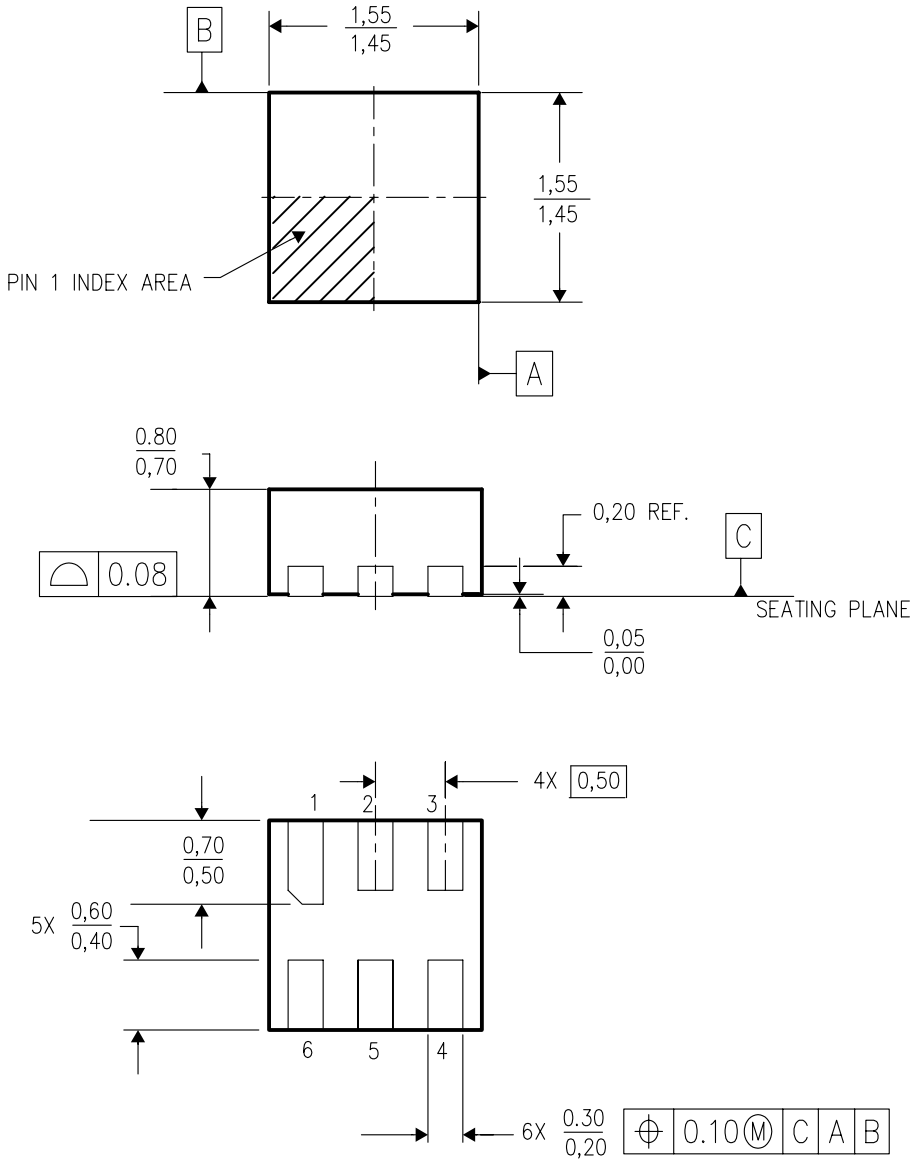
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO–193 variation AA (6 pin).

DDC (R–PDSO–G6) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

DSE (S–PDSO–N6) PLASTIC SMALL OUTLINE



4207810/A 03/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. This package is lead–free.

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