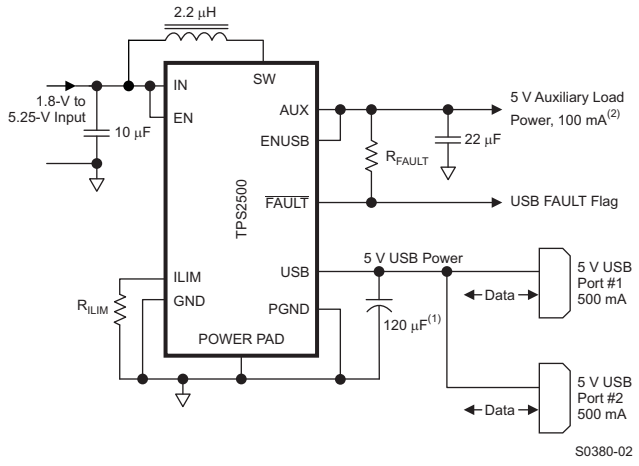
INTEGRATED USB POWER SWITCH WITH BOOST CONVERTER

Check for Samples: TPS2500, TPS2501

FEATURES

- **Integrated Synchronous Boost Converter and USB Current-Limit Power Switch**
- **Light-Load, High-Efficiency Eco-mode™ Control Scheme (TPS2500) or Constant Frequency (TPS2501)**
- **1.8-V to 5.25-V Input Voltage (2.2-V Minimum Start-Up Voltage)**
- **Adjustable USB Current Limit**
  - **130 mA to 1400 mA (Typical)**
- **Accurate 20% Current Limit at 1.4-A Setting**
- **Powers up to Two Standard USB Ports**
- **Auxiliary 5.1-V Output**
- **Fast Overcurrent-Response Time – 5 μs Typical**
- **Small 3-mm × 3-mm × 0.9-mm SON-10 Package**
- **15-kV / 8-kV System-Level ESD Capable**
- **UL Listed - File No. E169910**

TYPICAL APPLICATION CIRCUIT



(1) Requirement for USB applications only; downstream facing ports should be bypassed with 120 μF minimum per hub.

(2) Additional current can be supplied from AUX if <1 A is required for USB ports; total current should not exceed 1.1 A at V_{IN} = 3 V.

APPLICATIONS

- **Portable Applications Using Single Li+ Cell**
- **USB Hosts Without Native 5-V Supplies**

DESCRIPTION

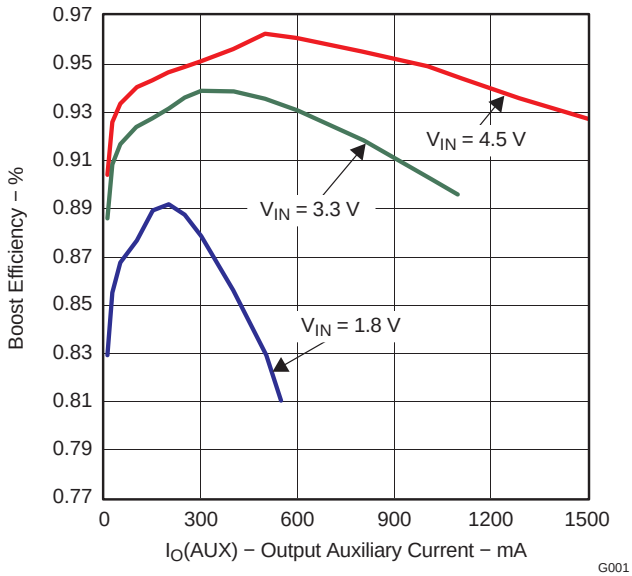
The TPS2500 and TPS2501 provide an integrated solution to meet USB 5-V power requirements from a 1.8-V to 5.25-V input supply. The features include a Hi-Speed USB compliant power output, output switch enable, current limit, and overcurrent fault reporting.

The 1.8-V to 5.25-V input can be supplied by sources including dc/dc regulated supplies (e.g., 3.3 V), or batteries such as single-cell Li+ or three-cell NiCd, NiMH, or alkaline.

The USB power-switch current limit is programmable via an external resistor from as low as 130 mA to as high as 1400 mA (typical). Two standard USB ports can be supported from a single TPS2500 or TPS2501 at the 1400-mA setting.

Additionally, the boost converter output is available as an auxiliary 5.1-V output to power additional loads. The total current supplied by the USB output and the auxiliary cannot exceed 1148 mA at V_{IN} = 3 V.

BOOST EFFICIENCY vs OUTPUT AUXILIARY CURRENT



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

DEVICE	TEMPERATURE(2)	PACKAGE	Eco-mode™ Control Scheme	MARKING
TPS2500	–40°C to 85°C	DRC (SON)	Enabled	CHO
TPS2501			Disabled	OBA

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.
(2) Maximum ambient temperature is a function of device junction temperature and system-level considerations, such as power dissipation and board layout. See *Dissipation Ratings* and *Recommended Operating Conditions* for specific information related to these devices.

ABSOLUTE MAXIMUM RATINGS (1)

over operating free-air temperature range (unless otherwise noted)

		VALUE	UNIT
	Input voltage range on SW(2), AUX, IN, USB, ENUSB, EN, $\overline{\text{FAULT}}$, ILIM	–0.3 to 7	V
	$\overline{\text{FAULT}}$ sink current	25	mA
	ILIM source current	1	mA
T_J	Junction temperature range	–40 to 150	°C
	ESD – HBM	2	kV
	ESD – CDM	500	V
	ESD – system level (contact/air)(3)	8/15	kV

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Leading edge voltage spikes on SW during normal switching operation may exceed 7 V and are within the intended operation of the device as long as the maximum voltage does not exceed 10 V for 25 ns. It is important to follow the recommended layout guidelines to minimize voltage overshoot. Do not force an external voltage source directly on SW.
(3) Surges per EN61000-4-2, 1999 applied between USB and output ground of the TPS2500EVM (HPA337) evaluation module (documentation available on the Web). These were the test levels, not the failure threshold.

DISSIPATION RATINGS(1)

PACKAGE	THERMAL RESISTANCE(2) θ_{JA}	THERMAL RESISTANCE θ_{JC}	$T_A \le 25°C$ POWER RATING
DRC	41.6°C/W	10.7°C/W	2403 mW

(1) The JEDEC high-K (2s2p) board used to derive this data was a 3-inch × 3-inch (7.62-mm × 7.62-mm), multilayer board with 1-ounce (0.035-mm) internal power and ground planes and 2-ounce (0.071-mm) copper traces on the top and bottom of the board.
(2) Mounting per the *PowerPAD™ Thermally Enhanced Package* application report (SLMA002).

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V_{IN}	Supply voltage at IN	1.8		5.25	V
V_{START}	Supply voltage at IN for start-up	2.2			V
	Enable voltage at EN, ENUSB	0		5.25	V
T_J	Operating junction temperature range	–40		125	°C

Table 1. RECOMMENDED EXTERNAL COMPONENTS

		MIN	NOM	MAX	UNIT
L	Inductor (nominal value)	2.2		4.7	µH
C_{IN}	Input capacitance on IN (ceramic capacitor, X5R, 10V, 0805)		10		µF
C_{AUX}	Boost output capacitance on AUX (ceramic capacitor, X5R, 10V, 1210)		22		µF
	Additional AUX capacitance			150	
R_{ILIM}	Current-limit set resistor from ILIM to GND (recommended 1% or better)	16.1		200	kΩ

ELECTRICAL CHARACTERISTICS — Shared Boost and USB Section

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
BIAS								
Quiescent current	V_{IN}	V_{IN} = 3.3 V, V_{AUX} = 5.2 V, V_{EN} = V_{IN}, V_{ENUSB} = V_{AUX}, I_{AUX} = I_{USB} = 0 A				13	20	µA
	V_{AUX}					380	480	
Shutdown current	V_{IN}	V_{IN} = 3.3 V, V_{EN} = V_{ENUSB} = 0 V, AUX and USB OPEN, –40°C ≤ T_J ≤ 85°C				4	8	µA
UVLO								
Undervoltage lockout threshold on IN for boost converter		V_{IN}	Rising		2.08		2.2	V
			After V_{AUX} in regulation	Falling	1.69		1.8	
				Hysteresis		0.4		
			Before V_{AUX} in regulation	Falling	1.93		2.05	
				Hysteresis		0.15		
Undervoltage lockout threshold on AUX for USB switch		V_{AUX}		Rising	4.18	4.3	4.45	V
				Falling	4.1	4.21	4.37	
				Hysteresis		0.09		
THERMAL SHUTDOWN								
Full thermal shutdown threshold					150			°C
Hysteresis						10		
USB-only thermal shutdown					130			
Hysteresis						10		

ELECTRICAL CHARACTERISTICS — Boost Section Only

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
APPLICATION SPECIFICATIONS						
V_{AUX}	AUX regulation voltage		4.95	5.1	5.25	V
OSCILLATOR						
freq	Switching frequency, normal mode	V_{IN} < V_{LFM}	925	1000	1075	kHz
	Switching frequency, low-frequency mode	V_{IN} > V_{LFM}	230	250	270	
V_{LFM}	Low-frequency mode input voltage threshold	V_{IN} rising	4.25	4.35	4.45	V
		Hysteresis		200		mV
V_{NFM}	No-frequency mode input voltage threshold (boost SYNC MOSFET always on)	V_{IN} rising	4.9	5.05	5.17	V
		Hysteresis		75		mV
	Maximum duty cycle			85		%
	Minimum controllable on-time			85		ns
Eco-mode CONTROL SCHEME, PULSED FREQUENCY OPERATION (TPS2500 ONLY)						
$IIND_{LOW}$	Demanded peak current to enter PFM mode	Peak inductor current, falling		420		mA
AUX_{LOW}	AUX-too-low comparator threshold	Resume switching due to AUX, falling		0.98 × V_{AUX}		V

ELECTRICAL CHARACTERISTICS — Boost Section Only (continued)

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OVERVOLTAGE PROTECTION						
V_{OVP}	AUX overvoltage shutdown	AUX rising		1.05 × V_{AUX}		V
POWER STAGE						
	Switch on resistance (SWN)			80	120	mΩ
I_{SW}	Peak switch current limit, cycle-by-cycle (SWN MOSFET)		3	4.5	6	A
I_{UPPER}				6.7		
	Switch on-resistance (SWP)			85	125	mΩ
	Switch on-resistance (SWP + USB)	$V_{IN} > V_{NFM}$		125	185	
START-UP						
I_{START}	Constant current		2.3	2.65	3	A
V_{EXIT}	Constant-current exit threshold (AUX voltage where converter starts switching), V_{IN} - V_{AUX}			700		mV
BOOST ENABLE (EN)						
	Enable threshold, boost converter		0.7		1	V
I_{EN}	Input current	V_{EN} = 0 V or 5.5 V	–0.5		0.5	µA

ELECTRICAL CHARACTERISTICS — USB Section Only

over recommended operating conditions (unless otherwise noted)

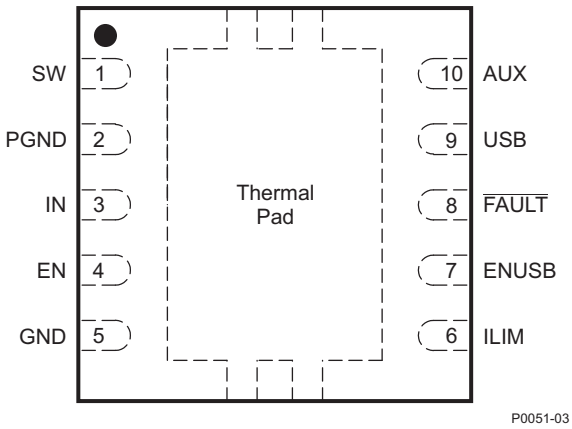
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
USB						
r_{USB}	USB switch resistance			50	80	mΩ
t_r	Rise time, output	V_{AUX} = 5.1 V, C_L = 100 µF, R_L = 10 Ω, R_{ILIM} = 20 kΩ		2	3	ms
t_f	Fall time, output			2.5	3.5	ms
USB ENABLE (ENUSB)						
	Enable threshold, USB switch		0.7		1.0	V
I_{ENUSB}	Input current	V_{ENUSB} = 0 V or 5.25 V	–0.5		0.5	µA
	Turnon time	C_L = 100 µF, R_L = 10 Ω, R_{ILIM} = 20 kΩ			5	ms
	Turnoff time				10	ms
$\overline{FAULT}$						
	Output low voltage	$I_{\overline{FAULT}}$ = 1 mA			150	mV
	Off-state current	$V_{\overline{FAULT}}$ = 5.25 V			1	µA
t_{DEG}	$\overline{FAULT}$ deglitch	$\overline{FAULT}$ assertion or deassertion due to overcurrent condition	6	8	10	ms
V_{TRIP}	AUX threshold for $\overline{FAULT}$ trip	AUX voltage falling	4.45	4.6	4.71	V
ILIM						
I_{OS}	Short-circuit output current, V_{IN} = 3.3 V	R_{ILIM} = 100 kΩ	190	285	380	mA
		R_{ILIM} = 40 kΩ	550	712	875	
		R_{ILIM} = 20 kΩ	1140	1420	1700	
t_{IOS}	Response time to short circuit	V_{AUX} = 5.1 V (see Figure 3)		5		µs

PIN DESCRIPTIONS

SIGNAL		TYPE(1)	DESCRIPTION
NAME	NO.		
AUX	10	O	Fixed 5.1-V boost converter output. Connect a low-ESR ceramic capacitor from AUX to PGND.
EN	4	I	Enable input for boost converter. Tie to IN to enable.
ENUSB	7	I	Enable input for the USB switch. Tie to IN or AUX to enable.
$\overline{\text{FAULT}}$	8	O	Active-low USB fault indicator (open-drain)
GND	5	P	Control/logic ground. Must be tied to PGND close to the IC externally.
ILIM	6	I	Program the nominal USB-switch current-limit threshold with a resistor to GND.
IN	3	I	Input supply voltage for boost converter
PGND	2	P	Source connection for the internal low-side boost-converter power switch. Connect to GND with a low-impedance connection to the input and output capacitors.
SW	1	P	Boost and rectifying switch input. This node is switched between PGND and AUX. Connect the boost inductor from IN to SW.
USB	9	O	Output of the USB power switch. Connect to the USB port.
Thermal pad	—	—	Must be soldered to achieve appropriate power dissipation. Connect to GND.

(1) I = input; O = output; P = power

DRC Package
(Top View)



AUX

AUX is the boost converter output and provides power to the USB switch and to any additional load connected to AUX. Internal feedback regulates AUX to 5.1 V. Connect a 22-μF ceramic capacitor from AUX to PGND to filter the boost converter output. See the *Component Recommendations* section for further details. Additional external load can be connected to AUX as long as the total current drawn by the USB switch and external load does not overload the boost converter. See the Determining the Maximum Allowable AUX and USB Current section for details.

EN

EN is a logic-level input that enables the boost converter. Pull EN above 1 V to enable the device and below 0.7 V to disable the device. EN also disables the USB switch, because the USB switch cannot be run when the boost converter is disabled.

ENUSB

ENUSB is a logic-level input that enables the USB switch. Pull ENUSB above 1 V to enable the USB switch and below 0.7 V to disable the USB switch. ENUSB only enables the USB switch. The boost converter is independent of ENUSB and continues to operate even when ENUSB disables the USB switch.

$\overline{\text{FAULT}}$

$\overline{\text{FAULT}}$ is an open-drain output that indicates when the USB switch is in an overcurrent or overtemperature condition. $\overline{\text{FAULT}}$ has a fixed internal deglitch of t_{DEG} to prevent false triggering from noise or transient conditions. $\overline{\text{FAULT}}$ asserts low if the USB switch remains in an overcurrent condition for longer than t_{DEG}. $\overline{\text{FAULT}}$ de-asserts when the overcurrent condition is removed after waiting for the same t_{DEG} period. Overtemperature conditions bypass the internal delay period and assert/de-assert the $\overline{\text{FAULT}}$ output immediately upon entering or leaving an overtemperature condition. $\overline{\text{FAULT}}$ is asserted low when V_{AUX} falls below V_{TRIP} (4.6 V, typical).

GND

Signal and logic circuits of the TPS2500 are referenced to GND. Connect GND to a quiet ground plane near the device. An optional 0.1-μF capacitor can be connected from V_{IN} to GND close the device to provide local decoupling. Connect GND and PGND to the thermal pad externally at a single location to provide a star-point ground. See the *Layout Recommendations* section for further details.

ILIM

Connect a resistor from ILIM to GND to program the current-limit threshold of the USB switch. Place this resistor as close to the device as possible to prevent noise from coupling into the internal circuitry. Do not drive ILIM with an external source. The current-limit threshold is proportional to the current through the R_{ILIM} resistor. See the *Programming the Current-Limit Threshold Resistor* section for details on selecting the current-limit resistor.

IN

IN is the input voltage supply for the boost converter. Connect a 10-μF ceramic capacitor (minimum) from IN to PGND. See the *Component Recommendations* section for further details on selecting the input capacitor.

PGND

PGND is the internal ground connection for the source of the low-side N-channel MOSFET in the boost converter. Connect PGND to an external plane near the ground connection of the input and output capacitors to minimize parasitic effects due to high switching currents of the boost converter. Connect PGND to GND and the thermal pad externally at a single location to provide a star-point ground. See the *Layout Recommendations* section for further details.

SW

SW is the internal boost converter connection of the low-side N-channel MOSFET drain and the high-side P-channel drain. Connect the boost inductor from IN to SW close to the device to minimize parasitic effects on the device operation.

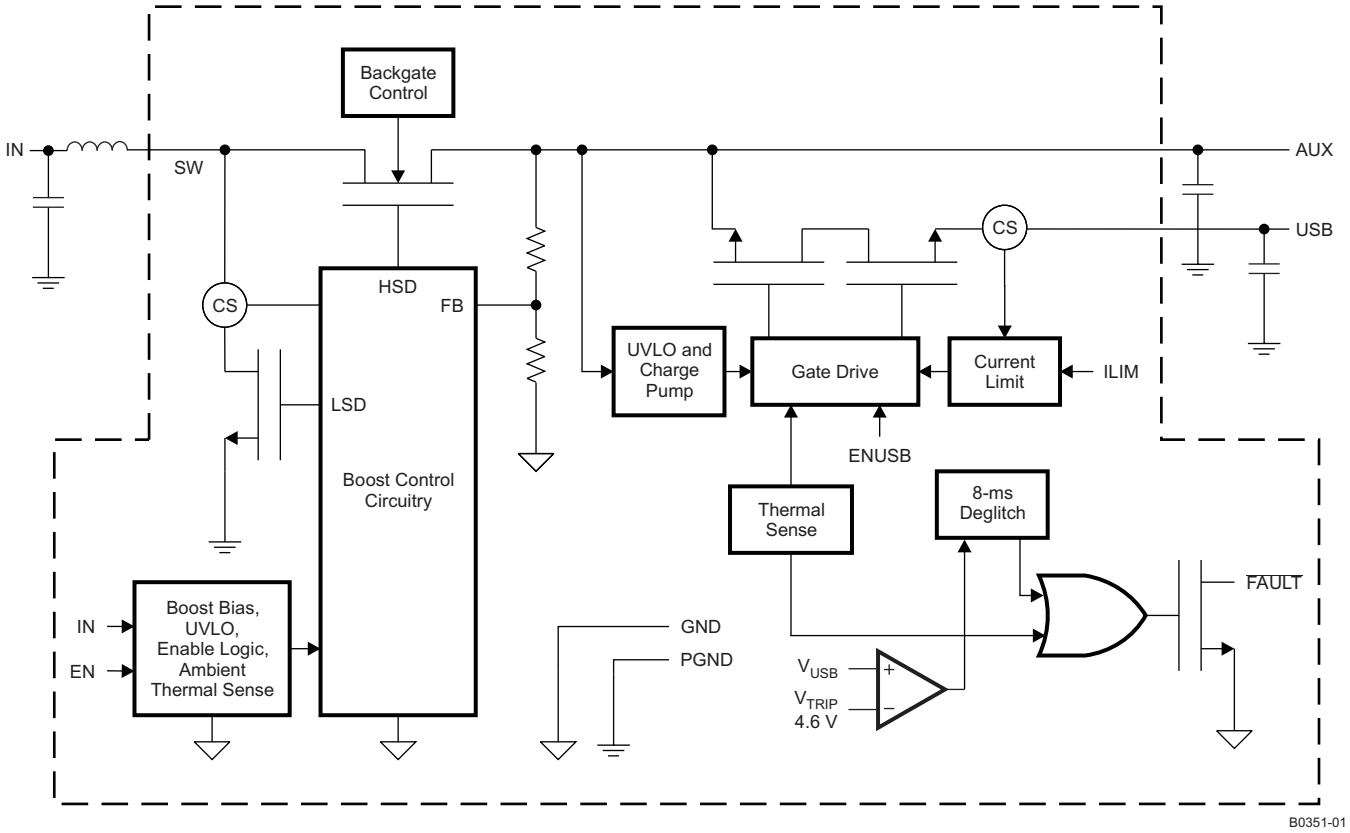
Thermal Pad

The thermal pad connection is used to heat-sink the device to the printed-circuit board (PCB). The thermal pad may not be connected externally to a potential other than ground because it is connected to GND internally. The thermal pad must be soldered to the PCB to remove sufficient thermal energy in order to stay within the recommended operating range of the device.

USB

USB is the output of the USB switch and should be connected to the USB connector to provide USB power. Although the device does not require it for operation, a bulk capacitor may be connected from USB to PGND to meet USB standard requirements. See the latest USB 2.0 specification for further details.

FUNCTIONAL BLOCK DIAGRAM



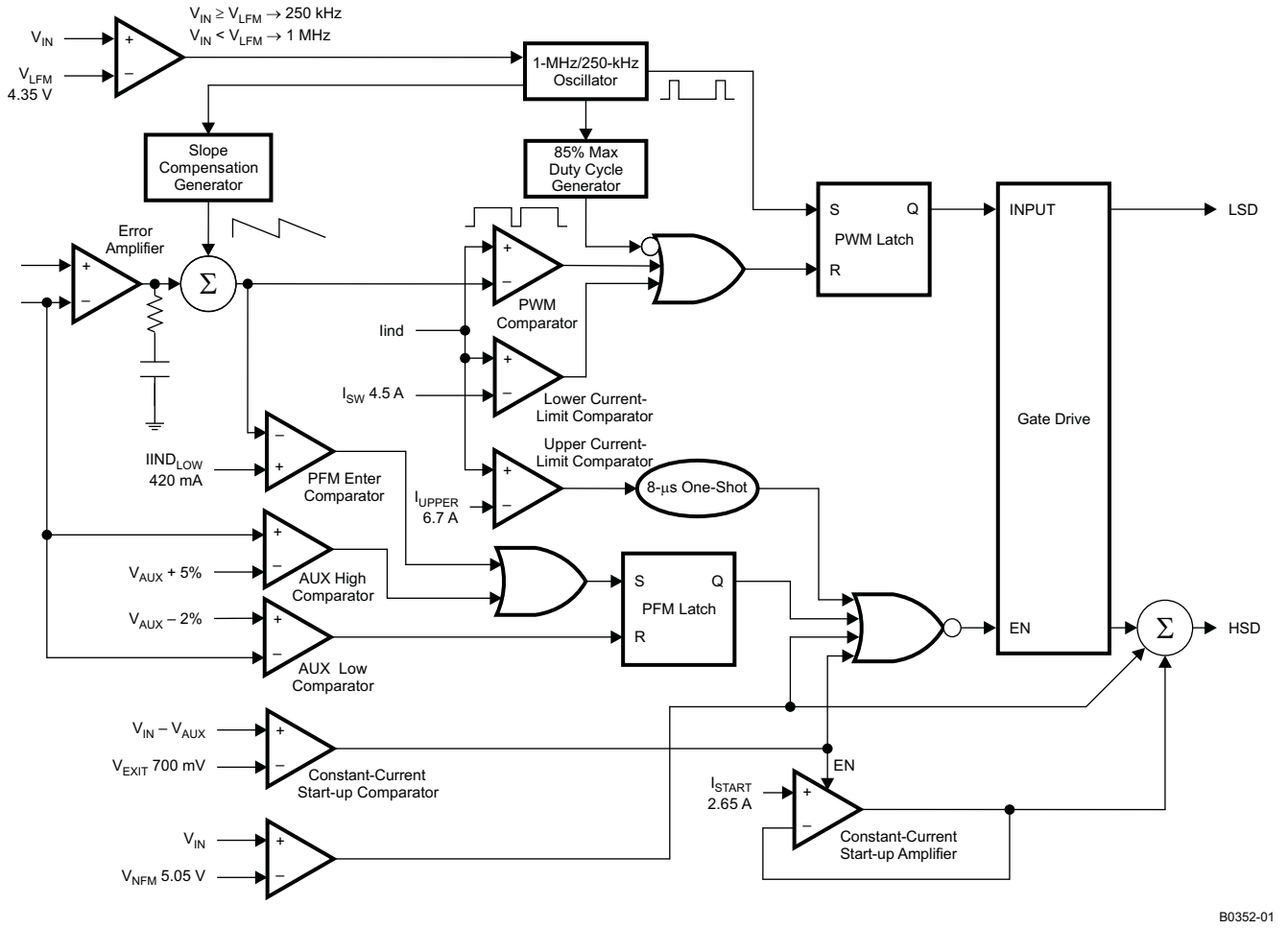
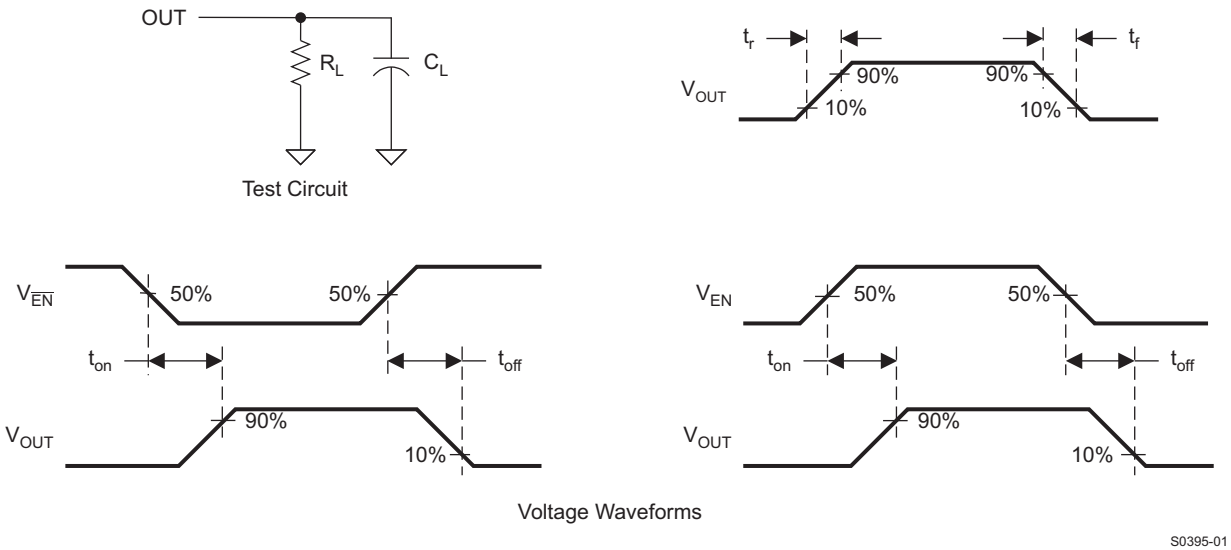


Figure 1. Detail of Boost Control Circuitry

PARAMETER MEASUREMENT INFORMATION



Voltage Waveforms

Figure 2. Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION (continued)

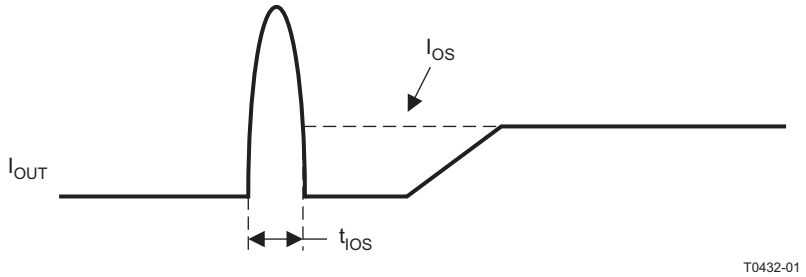


Figure 3. Response Time to Short-Circuit Waveform

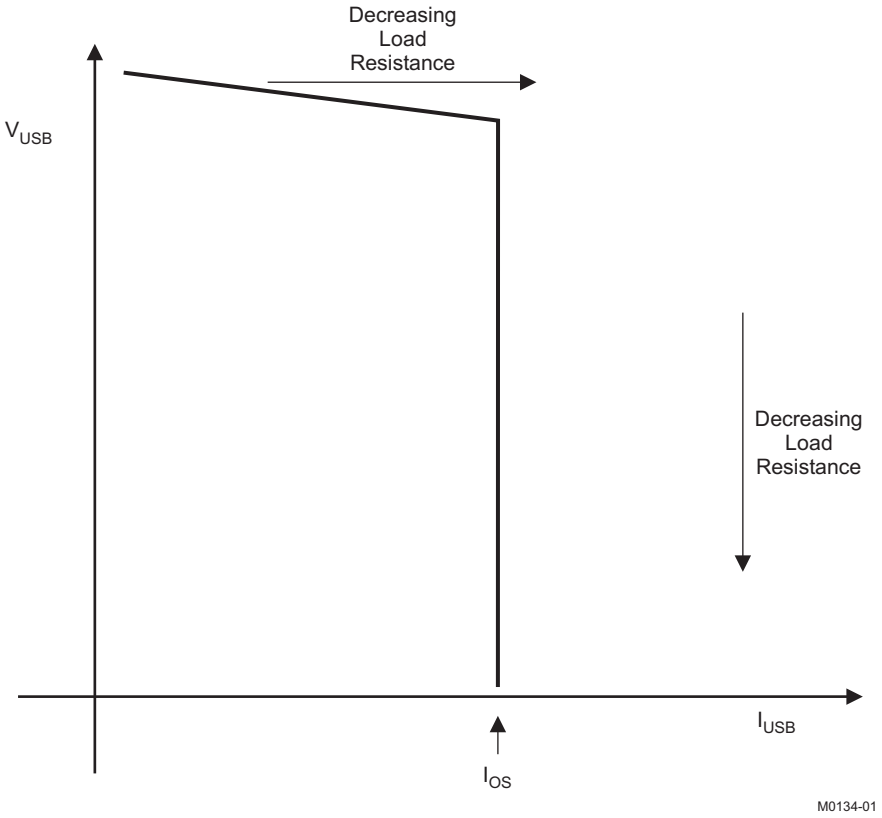


Figure 4. USB Output Voltage vs USB Load Current

TYPICAL CHARACTERISTICS

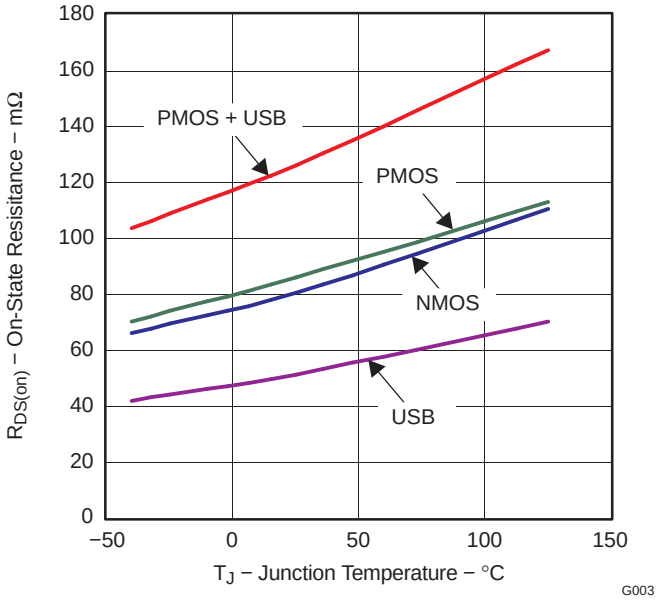


Figure 5. MOSFET On-State Resistance vs Junction Temperature

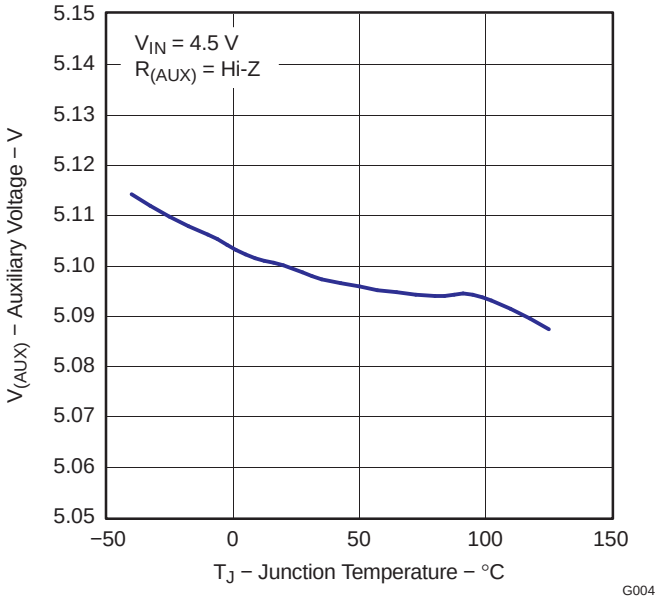


Figure 6. V_{AUX} vs Junction Temperature, I_{AUX} = I_{USB} = 0 A

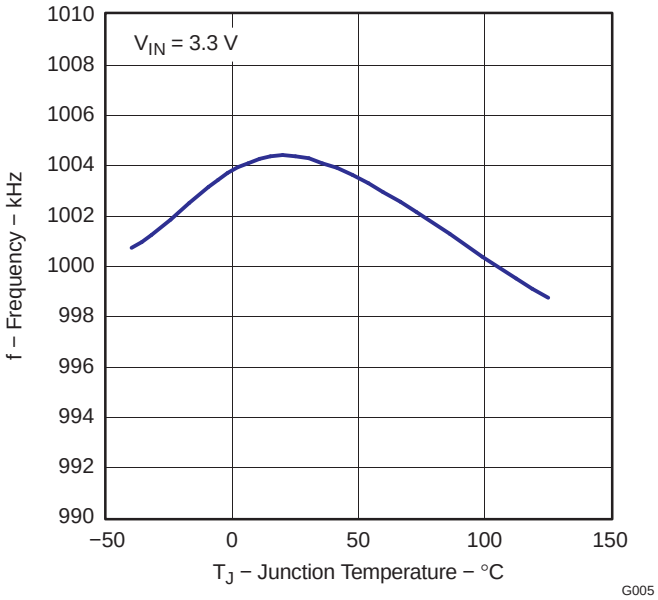


Figure 7. Converter Switching Frequency vs Junction Temperature, V_{IN} = 3.3 V

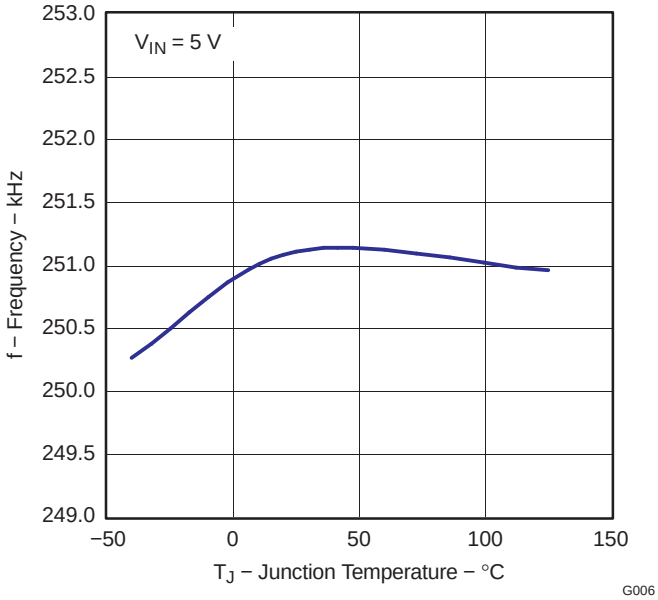


Figure 8. Converter Switching Frequency vs Junction Temperature, V_{IN} = 5 V

TYPICAL CHARACTERISTICS (continued)

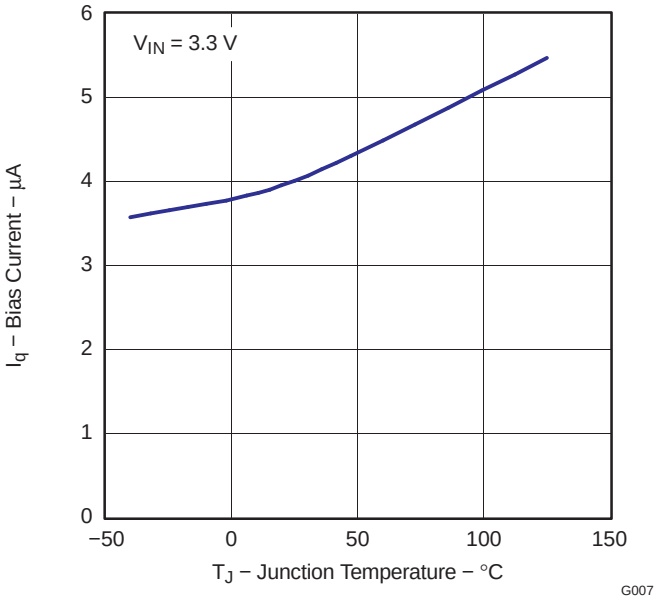


Figure 9. Bias Current vs Junction Temperature, V_{IN} = 3.3 V, V_{EN} = 0 V (Disabled)

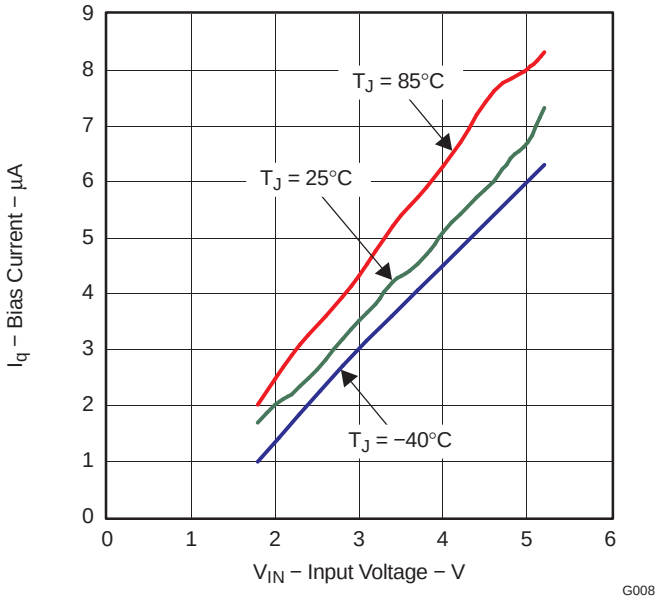


Figure 10. Bias Current vs Input Voltage, V_{EN} = 0 V (Disabled)

THEORY OF OPERATION

DESCRIPTION

This device targets applications for host-side USB devices where a 5-V power rail, required for USB operation, is unavailable. The TPS2500 integrates the functionality of a synchronous boost converter and a single USB switch into a monolithic integrated circuit so that lower-voltage rails can be used directly to provide USB power. An additional feature is that the auxiliary 5-V power rail is brought external to the device to power non-USB loads in addition to the integrated USB switch.

The boost converter is highly integrated, including the switching MOSFETs (low-side N-channel, high-side synchronous P-channel), gate-drive and analog-control circuitry, and control-loop compensation. Additional features include high-efficiency light-load operation, overload and short-circuit protection, and controlled monotonic soft start. The USB switch integrates all necessary functions, including back-to-back series N-channel MOSFETs, charge-pump gate driver, and analog control circuitry. The current-limit protection is user-adjustable by selecting the R_{ILIM} resistor from ILIM to GND.

The only external components required are the boost inductor, current-limit setting resistor, and input and output capacitors for the boost converter.

BOOST CONVERTER

Start-Up

Input power to the TPS2500 is provided from IN to GND. The device has an undervoltage lockout (UVLO) circuit that disables the device until the voltage on IN exceeds 2.15 V (typical). The TPS2500 goes through its normal start-up process and attempts to regulate the AUX voltage to 5.1 V (typical).

The boost converter has a two-step start-up sequence. Step one is a constant-current mode that regulates the current through the high-side P-channel MOSFET to I_{START} (2.65 A typical). I_{START} provides power to the load and charges the output capacitance on V_{AUX} until V_{AUX} reaches $V_{IN} – V_{EXIT}$. The converter begins to switch once V_{AUX} exceeds $V_{IN} – V_{EXIT}$. The initial duty cycle of the device is limited by a closed-loop soft start that ramps the reference voltage to the internal error amplifier to provide a controlled, monotonic start-up on V_{AUX}. The boost converter goes through this cycle any time the voltage on V_{AUX} drops below $V_{IN} – V_{EXIT}$ due to overload conditions or the boost converter re-enables after normal shutdown.

The USB switch is powered directly from V_{AUX} and turns on once the UVLO of the USB switch is met (4.3 V typical). The turnon is controlled internally to provide a monotonic start-up on V_{USB}.

Normal Operation

The boost converter runs at a 1-MHz fixed frequency and regulates the output voltage V_{AUX} using a pulse-width modulating (PWM) topology that adjusts the duty cycle of the low-side N-channel MOSFET on a cycle-by-cycle basis. The PWM latch is set at the beginning of each clock cycle and commands the gate driver to turn on the low-side MOSFET. The low-side MOSFET remains on until the PWM latch is reset.

Voltage regulation is controlled by a peak-current-mode control architecture. The voltage loop senses the voltage on V_{AUX} and provides negative feedback into an internal, transconductance-error amplifier with internal compensation and resistor divider. The output of the transconductance-error amplifier is summed with the output of the slope-compensation block and provides the error signal that is fed into the inverting input of the PWM comparator. Slope compensation is necessary to prevent subharmonic oscillations that may occur in peak-current-mode control architectures that exceed 50% duty cycle. The PWM ramp fed into the noninverting input of the PWM comparator is provided by sensing the inductor current through the low-side N-channel MOSFET. The PWM latch is reset when the PWM ramp intersects the error signal and terminates the pulse width for that clock period. The TPS2500 stops switching if the peak-demanded current signal from the error amplifier falls below the zero-duty-cycle threshold of the device.

Low-Frequency Mode

The TPS2500 enters low-frequency mode above $V_{IN} = V_{LFM}$ (4.35 V typical) by reducing the dc/dc converter frequency from 1 MHz (typical) to 250 kHz (typical). Current-mode control topologies require internal leading-edge blanking of the current-sense signal to prevent nuisance trips of the PWM control MOSFET. The consequence of leading-edge blanking is that the PWM controller has a minimum controllable on-time (85 ns typical) that results in a minimum controllable duty cycle. In a boost converter, the demanded duty cycle decreases as the input voltage increases. The boost converter pulse-skips if the demanded duty cycle is less than what the minimum controllable on-time allows, which is undesirable due to the excessive increase in switching ripple. When the TPS2500 enters low-frequency mode above $V_{IN} = V_{LFM}$, the minimum controllable duty cycle is increased because the minimum controllable on-time is a smaller percentage of the entire switching period. Low-frequency mode prevents pulse skipping at voltages larger than V_{LFM}. The TPS2500 resumes normal 1-MHz switching operation when V_{IN} decreases below V_{LFM}.

One effect of reducing the switching frequency is that the ripple current in the inductor and output AUX capacitors is increased. It is important to verify that the peak inductor current does not exceed the peak switch current limit I_{SW} (4.5 A typical) and that the increase in AUX ripple is acceptable during low-frequency mode.

No-Frequency Mode

The TPS2500 enters no-frequency mode above $V_{IN} = V_{NFM}$ (5.05 V typical) by disabling the oscillator and turning on the high-side synchronous PMOS 100% of the time. The input voltage is now directly connected to the AUX output through the inductor and high-side PMOS. Power dissipation in the device is reduced in no-frequency mode because there is no longer any switching loss and no RMS current flows through the low-side control NMOS, which results in higher system-level efficiency. The boost converter resumes switching when V_{IN} falls below V_{NFM}.

Eco-mode Light-Load Operation

The TPS2500 enters the Eco-mode control scheme at light loads to increase efficiency. The device reduces power dissipation while in the Eco-mode control scheme by disabling the gate drivers and power MOSFETs and entering a pulsed-frequency mode (PFM). PFM works by disabling the gate driver when the PFM latch is set. During this time period there is no switching, and the load current is provided solely by the output capacitor.

There are two comparators that determine when the device enters or leaves the Eco-mode control scheme. The first comparator is the PFM-enter comparator. The PFM-enter comparator monitors the peak demanded current in the inductor and allows the device to enter the Eco-mode control scheme when the inductor current falls below $IIND_{LOW}$ (420 mA typical). The second comparator is the AUX-low comparator. The AUX-low comparator monitors AUX and forces the converter out of the Eco-mode control scheme and resumes normal operation when the voltage on AUX falls below AUX_{LOW} (5 V typical). The Eco-mode control scheme is disabled during low-frequency mode when $V_{IN} > V_{LFM}$ (4.35 V typical).

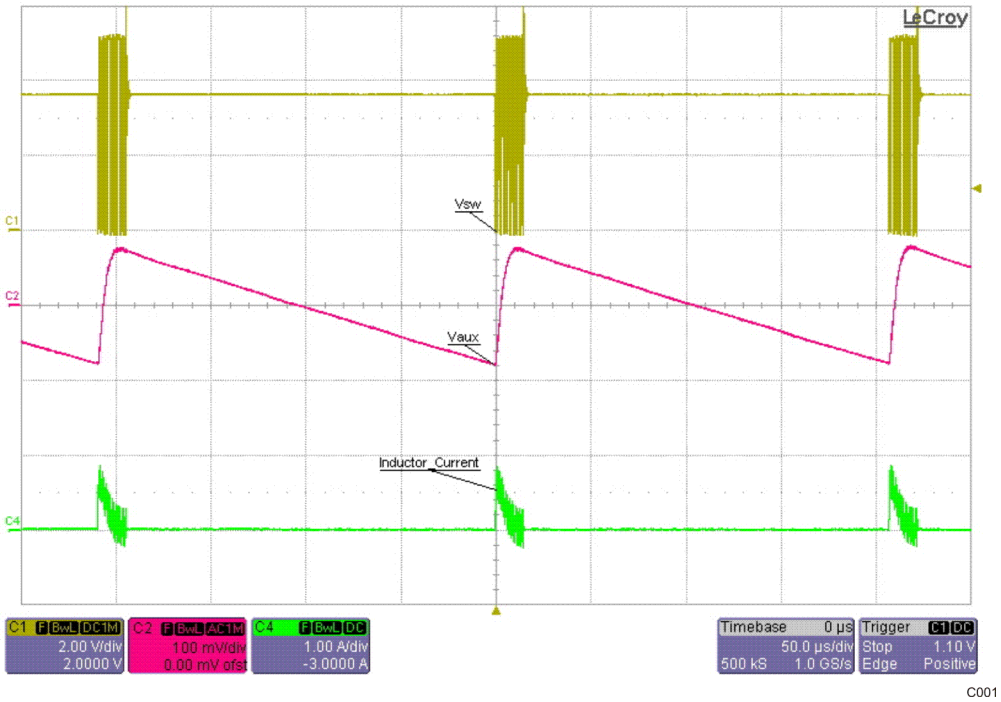


Figure 11. Eco-mode Control Scheme Operation, V_{IN} = 3.3 V, I_{AUX} = 10 mA

Overvoltage Protection

The TPS2500 provides overvoltage protection on V_{AUX} to protect downstream devices. Overvoltage protection is provided by disabling the gate drivers and power MOSFETs when an overvoltage condition is detected. The TPS2500 uses a single AUX-high comparator to monitor the AUX voltage by sensing the voltage on the internal feedback node fed into the error amplifier. The AUX-high comparator disables the gate driver whenever the voltage on AUX exceeds the regulation point by 5% (typical). The gate driver remains disabled until the AUX voltage falls below the 5% high OVP threshold. The overvoltage protection feature is disabled when $V_{IN} > V_{NFM}$ (5.05 V typical) to prevent unwanted shutdown.

Overload Conditions

The TPS2500 boost converter uses multiple overcurrent protection features to limit current in the event of an overload or short-circuit condition. The first feature is the lower current-limit comparator that works on a cycle-by-cycle basis. This comparator turns off the low-side MOSFET by resetting the PWM latch whenever the current through the low-side MOSFET exceeds 4.5 A (typical). The low-side MOSFET remains off until the next switching cycle. The second feature is the upper current-limit comparator that disables switching for eight switching cycles whenever the current in the low-side MOSFET exceeds 6.7 A (typical). After eight switching cycles, the boost converter resumes normal operation. The third feature is the constant-current start-up I_{START} comparator that disables switching and regulates the current through the high-side MOSFET whenever the voltage on V_{AUX} drops below the input voltage by V_{EXIT} (700 mV typ). This feature protects the boost converter in the event of an output short circuit on V_{AUX}. I_{START} also current-limit protects the synchronous MOSFET in no-frequency mode when $V_{IN} > V_{NFM}$ (5.05 V typical). The converter goes through normal start-up operation once the short-circuit condition is removed. A fourth feature is the 85% (typical) maximum-duty-cycle clamp that prevents excessive current from building in the inductor.

Determining the Maximum Allowable AUX and USB Current

The maximum output current of the boost converter out of AUX depends on several system-level factors including input voltage, inductor value, switching frequency, and ambient temperature. The limiting factor for the TPS2500 is the peak inductor current, which cannot exceed I_{SW} (3 A minimum). The cycle-by-cycle current-limit turns off the low-side NMOS as a protection mechanism whenever the inductor current exceeds I_{SW}. The graph in Figure 12 can be used as a guideline for determining the maximum total current at different input voltages. The

typical plot assumes nominal conditions—2.2 μH inductor, 1-MHz/250-kHz switching frequency, nominal MOSFET on-resistances. The conservative plot assumes more pessimistic conditions—1.7 μH inductor, 925-kHz/230-kHz switching frequency, and maximum MOSFET on-resistances. The graph accounts for the frequency change from 1-MHz to 250-kHz when V_{IN} > V_{LFM} (4.35 V typical) and for the no-frequency mode when V_{IN} > V_{NFM} (5.05 V typical), which explains the discontinuities of the graph.

Table 2. Maximum Total DC/DC Current (I_{AUX} + I_{USB}) at Common Input Voltages

Input Voltage (V)	Maximum Total Output Current (I_{AUX} + I_{USB})	
	Conservative (mA)	Typical (mA)
1.8	599	757
2.5	916	1113
2.7	1008	1216
3	1148	1374
3.3	1308	1536
3.6	1445	1704
4.35	1241	1730
4.5	1364	1858
4.75	1593	2093
5.05	2300	2300
5.25	2300	2300

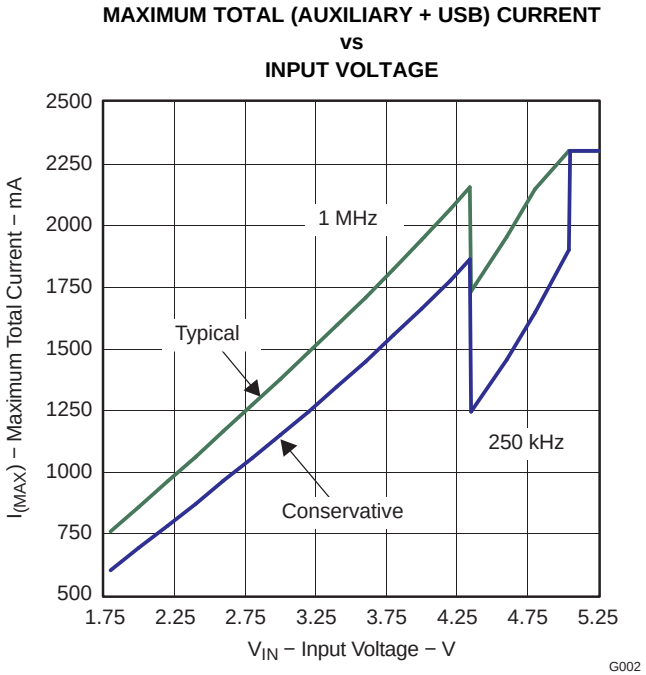


Figure 12. Maximum Total DC/DC Current vs. Input Voltage

POWER SWITCH

Overview

The TPS2500 integrates a current-limited, power-distribution switch using an N-channel MOSFET for applications where short circuits or heavy capacitive loads are encountered. The current-limit threshold is user-programmable between 130 mA and 1.4 A (typical) by selecting an external resistor. The device incorporates an internal charge pump and gate-drive circuitry necessary to fully enhance the N-channel MOSFET. The internal gate driver controls the MOSFET turnon to limit large current and voltage surges by providing built-in soft-start functionality.

The power switch has an independent undervoltage lockout (UVLO) circuit that disables the power switch until the voltage on AUX reaches 4.3 V (typical). Built-in hysteresis prevents unwanted on/off cycling due to input voltage drop on AUX from current surges on the output of the power switch. The power switch has an independent logic-level enable control (ENUSB) that gates power-switch turnon and bias for the charge pump, driver, and miscellaneous control circuitry. A logic-high input on ENUSB enables the driver, control circuits, and power switch. The enable input is compatible with CMOS, TTL, LVTTL, 2.5-V, and 1.8-V logic levels.

Overcurrent Conditions

The TPS2500 power switch responds to overcurrent conditions by limiting its output current to the I_{OS} levels shown in Figure 4. The device maintains a constant output current and reduces the output voltage accordingly during an overcurrent condition. Two possible overload conditions can occur.

The first condition is when a short circuit or partial short circuit is present on the output of the switch prior to device turnon and the device is powered up or enabled. The output voltage is held near zero potential with respect to ground, and the TPS2500 ramps the output current to I_{OS}. The TPS2500 power switch limits the current to I_{OS} until the overload condition is removed or the device begins to cycle thermally.

The second condition is when a short circuit, partial short circuit, or transient overload occurs while the device is already enabled and powered on. The device responds to the overcurrent condition within time t_{IOS} (see Figure 3). The current-sense amplifier is overdriven during this time and momentarily disables the power switch. The current-sense amplifier recovers and limits the output current to I_{OS}. The power switch thermally cycles if an overload condition is present long enough to activate thermal limiting in any of the foregoing cases. The power switch turns off when the junction temperature exceeds 130°C while in current-limit. The power switch remains off until the junction temperature cools 10°C and then restarts. The TPS2500 power switch cycles on/off until the overload is removed. The boost converter is independent of the power-switch thermal sense and continues to operate as long as the temperature of the boost converter remains less than 150°C and does not trigger the boost-converter thermal sense.

$\overline{\text{FAULT}}$ Response

The $\overline{\text{FAULT}}$ open-drain output is asserted low during an overcurrent condition that causes V_{USB} to fall below V_{TRIP} (4.6 V typical) or causes the junction temperature to exceed the shutdown threshold (130°C). The TPS2500 asserts the $\overline{\text{FAULT}}$ signal until the fault condition is removed and the power switch resumes normal operation. The $\overline{\text{FAULT}}$ signal is independent of the boost converter. The $\overline{\text{FAULT}}$ signal uses an internal delay *deglitch* circuit (8-ms typical) to delay asserting the $\overline{\text{FAULT}}$ signal during an overcurrent condition. The power switch must remain in an overcurrent condition for the entire deglitch period or the deglitch timer is restarted. This ensures that $\overline{\text{FAULT}}$ is not accidentally asserted due to normal operation such as starting into a heavy capacitive load. The deglitch circuitry delays entering and leaving fault conditions. Overtemperature conditions are not deglitched and assert the $\overline{\text{FAULT}}$ signal immediately.

Power Switch Undervoltage Lockout

The undervoltage lockout (UVLO) circuit disables the TPS2500 power switch until the input voltage on AUX reaches the power switch UVLO turn-on threshold of 4.3 V (typical). Built-in hysteresis prevents unwanted on/off cycling due to input-voltage drop from large current surges.

Power Switch Enable

The logic enable controls the power switch, bias for the charge pump, driver, and other circuits to reduce the supply current of the power switch. The power-switch supply current is reduced to less than 4 μA (typical) when a logic-low input is present on ENUSB. A logic-high input on ENUSB enables the driver, control circuits, and power switch. The enable input is compatible with both TTL and CMOS logic levels.

Programming the Current-Limit Threshold Resistor R_{ILIM}

The overcurrent threshold is user programmable via an external resistor. The TPS2500 uses an internal regulation loop to provide a regulated voltage on the ILIM pin. The current-limit threshold is proportional to the current sourced out of ILIM. The recommended 1% resistor range for R_{ILIM} is 16.1 kΩ ≤ R_{ILIM} ≤ 200 kΩ to ensure stability of the internal regulation loop. Many applications require that the minimum current limit is above a certain current level or that the maximum current limit is below a certain current level, so it is important to consider the tolerance of the overcurrent threshold when selecting a value for R_{ILIM}. The following equations and Figure 13 can be used to calculate the resulting overcurrent threshold for a given external resistor value ®$_{ILIM}$). Figure 13 includes current-limit tolerance due to variations caused by temperature and process. However, the equations do not account for tolerance due to external resistor variation, so it is important to account for this tolerance when selecting R_{ILIM}. The traces routing the R_{ILIM} resistor to the TPS2500 should be as short as possible to reduce parasitic effects on the current-limit accuracy.

R_{ILIM} can be selected to provide a current-limit threshold that occurs 1) above a minimum load current or 2) below a maximum load current.

To design above a minimum current-limit threshold, find the intersection of R_{ILIM} and the maximum desired load current on the $I_{OS(min)}$ curve and choose a value of R_{ILIM} below this value. Programming the current limit above a minimum threshold is important to ensure start up into full load or heavy capacitive loads. The resulting maximum current-limit threshold is the intersection of the selected value of R_{ILIM} and the $I_{OS(max)}$ curve.

To design below a maximum current-limit threshold, find the intersection of R_{ILIM} and the maximum desired load current on the $I_{OS(max)}$ curve and choose a value of R_{ILIM} above this value. Programming the current limit below a maximum threshold is important to avoid current-limiting upstream power supplies, causing the input voltage bus to droop. The resulting minimum current-limit threshold is the intersection of the selected value of R_{ILIM} and the $I_{OS(min)}$ curve.

Current-limit threshold equations (I_{OS}):

$$I_{OS(max)}\ (mA) = \frac{27{,}570\ V}{R_{ILIM}^{0.93}\ k\Omega}$$

$$I_{OS(typ)}\ (mA) = \frac{28{,}235\ V}{R_{ILIM}^{0.998}\ k\Omega}$$

$$I_{OS(min)}\ (mA) = \frac{32{,}114\ V}{R_{ILIM}^{1.114}\ k\Omega}$$

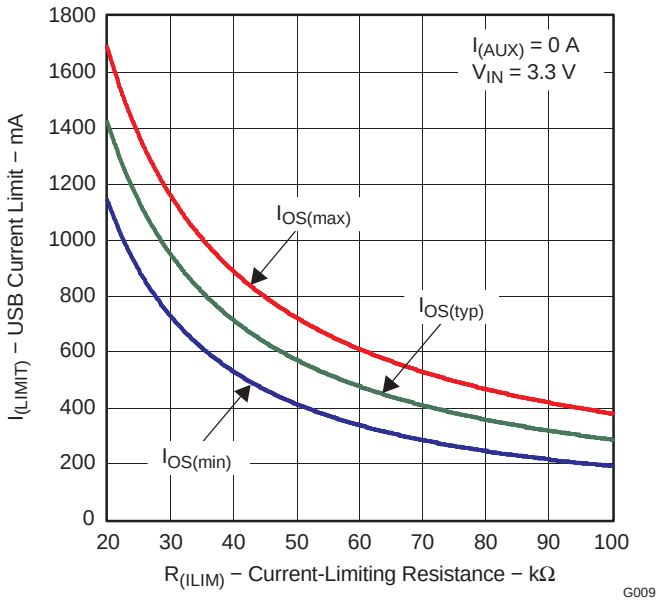


Figure 13. USB Current-Limit Threshold vs R_{ILIM} Over Temperature and Process, V_{IN} = 3.3 V, I_{AUX} = 0 A

In addition to current-limit shifts due to process and temperature, the operating conditions of the boost converter also affect the current-limit threshold of the USB switch. Figure 13 accounts for process and temperature shifts at V_{IN} = 3.3 V and I_{AUX} = 0 A. The following figures show current-limit shift trends over V_{IN} and I_{AUX} (where I_{AUX} is the auxiliary 5-V load current provided to any non-USB loads). These curves can be used to calculate the USB current-limit threshold shift for a given application where the input voltage V_{IN} range and auxiliary current I_{AUX} vary.

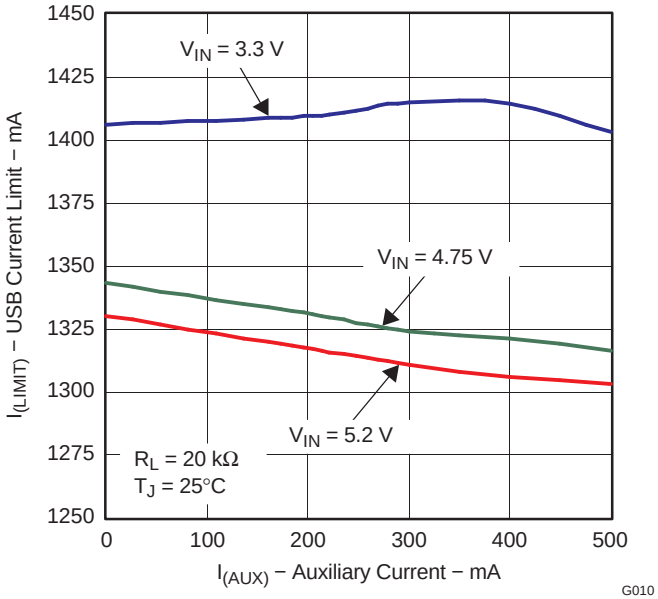


Figure 14. USB Current-Limit Threshold vs I_{AUX}, R_{ILIM} = 20 kΩ, T_A = 25 °C

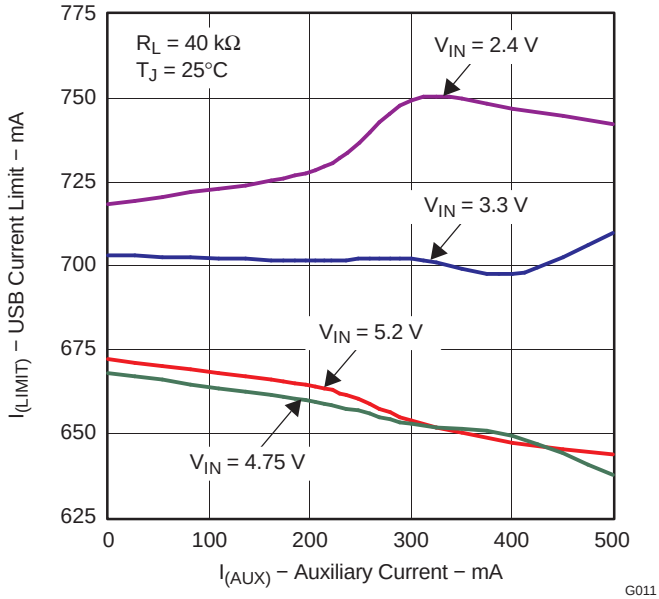


Figure 15. USB Current-Limit Threshold vs I_{AUX}, R_{ILIM} = 40 kΩ, T_A = 25 °C

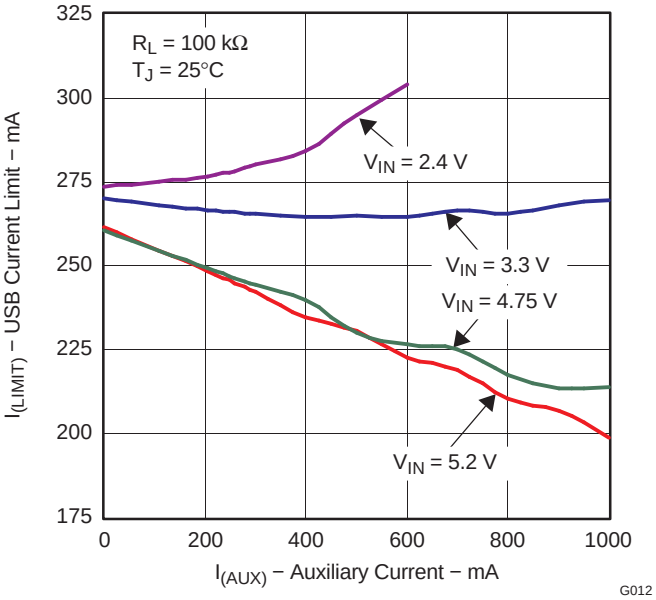


Figure 16. USB Current-Limit Threshold vs I_{AUX}, R_{ILIM} = 100 kΩ, T_A = 25 °C

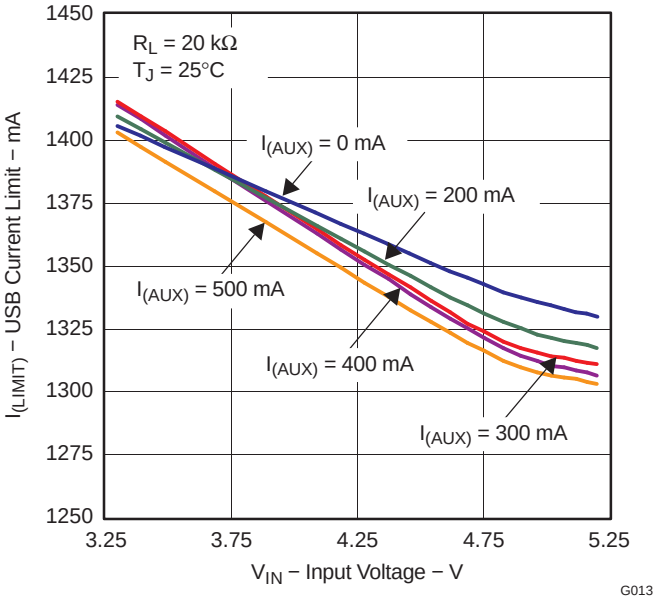


Figure 17. USB Current-Limit Threshold vs V_{IN}, R_{ILIM} = 20 kΩ, T_A = 25 °C

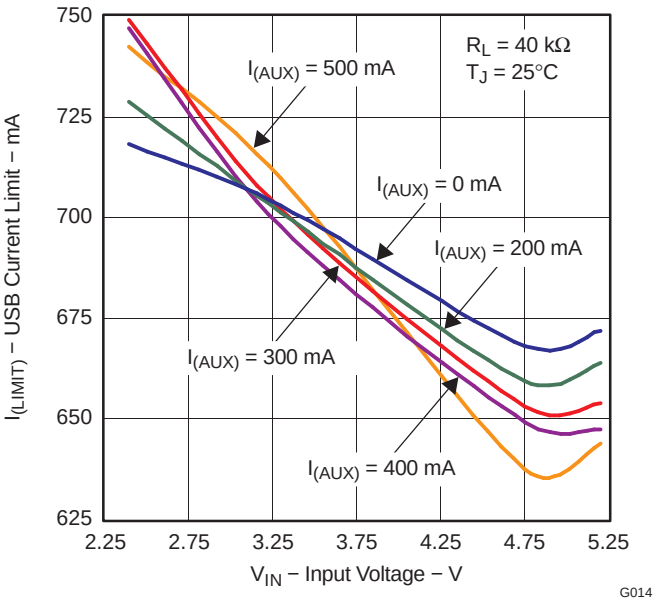


Figure 18. USB Current-Limit Threshold vs V_{IN}, R_{ILIM} = 40 kΩ, T_A = 25 °C

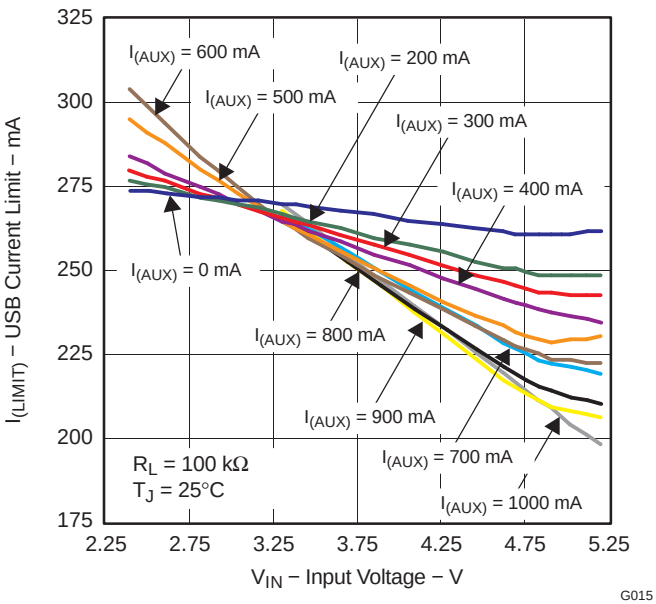


Figure 19. USB Current-Limit Threshold vs V_{IN}, R_{ILIM} = 100 kΩ, T_A = 25 °C

Accounting for Resistor Tolerance in the USB Switch Current-Limit Accuracy

The previous sections described the selection of R_{ILIM}, given certain application requirements and the importance of understanding the current-limit threshold tolerance. The analysis focused only on the TPS2500 performance and assumed an exact resistor value. However, resistors sold in quantity are not exact and are bounded by an upper and lower tolerance centered around a nominal resistance. The additional R_{ILIM} resistance tolerance directly affects the current-limit threshold accuracy at a system level. Table 3 shows a process that accounts for

worst-case resistor tolerance assuming 1% resistor values. Step 1 follows the selection process outlined in the application examples above. Step 2 determines the upper and lower resistance bounds of the selected resistor. Step 3 uses the upper and lower resistor bounds in the I_{OS} equations to calculate the threshold limits. It is important to use tighter tolerance resistors, e.g. 0.5% or 0.1%, when precision current limiting is desired. Also, it is important to note that this table assumes V_{IN} = 3.3 V and I_{AUX} = 0 A, so Figure 14 through Figure 19 should be consulted to approximate how I_{OS} shifts with V_{IN} and I_{AUX}. See the Programming the Current-Limit Threshold Resistor section for additional details.

Table 3. Common R_{ILIM} Resistor Selections, V_{IN} = 3.3 V, I_{AUX} = 0 A

Desired Nominal Current Limit (mA)	Ideal Resistor (kΩ)	Closest 1% Resistor (kΩ)	Resistor Tolerance		Actual Limits		
			1% low (kΩ)	1% high (kΩ)	$I_{OS(min)}$ (mA)	$I_{OS(nom)}$ (mA)	$I_{OS(max)}$ (mA)
300	94.98	95.30	94.35	96.25	198.2	299.0	401.7
400	71.19	71.50	70.79	72.22	273.0	398.3	524.8
500	56.93	57.60	57.02	58.18	347.4	494.2	641.7
600	47.42	47.50	47.03	47.98	430.6	599.0	767.7
700	40.64	40.20	39.80	40.60	518.5	707.6	896.5
800	35.55	35.70	35.34	36.06	591.8	796.6	1001.2
900	31.59	31.60	31.28	31.92	678.0	899.7	1121.5
1000	28.42	28.70	28.41	28.99	754.7	990.4	1226.5
1100	25.84	26.10	25.84	26.36	839.0	1088.9	1339.7
1200	23.68	23.70	23.46	23.94	934.1	1199.0	1465.5
1300	21.85	22.10	21.88	22.32	1009.8	1285.5	1563.9
1400	20.29	20.50	20.30	20.71	1098.0	1385.7	1677.1

Thermal Sense

The TPS2500 self-protects using two independent thermal sensing circuits that monitor the operating temperatures of the boost converter and power switch independently and disable operation if the temperature exceeds recommended operating conditions. The boost converter and power switch each have an ambient thermal sensor that disables operation if the measured junction temperature in that part of the circuit exceeds 150°C. The boost converter continues to operate even if the power switch is disabled due to an overtemperature condition.

Component Recommendations

The main functions of the TPS2500 are integrated and meet recommended operating conditions with a wide range of external components. The following sections give guidelines and trade-offs for external component selection. The recommended values given are conservative and intended over the full range of recommended operating conditions.

Boost Inductor

Connect the boost inductor from IN to SW. The inductance controls the ripple current through the inductor. A 2.2-μH inductor is recommended, and the minimum and maximum inductor values are constrained by the integrated features of the TPS2500. The minimum inductance is limited by the peak inductor-current value. The ripple current in the inductor is inversely proportional to the inductance value, so the output voltage may fall out of regulation if the peak inductor current exceeds the cycle-by-cycle current-limit comparator (3 A minimum). Using a nominal 2.2-μH inductor allows full recommended current operation even if the inductance is 20% low (1.76 μH) due to component variation. The maximum inductance value is limited by the internal compensation of the boost-converter control loop. A maximum 4.7-μH (typical) inductor value is recommended to maintain adequate phase margin over the full range of recommended operating conditions.

The following chart shows the efficiency vs AUX current of two different inductors at V_{IN} = 3.3 V to demonstrate how efficiency is impacted by different inductors.

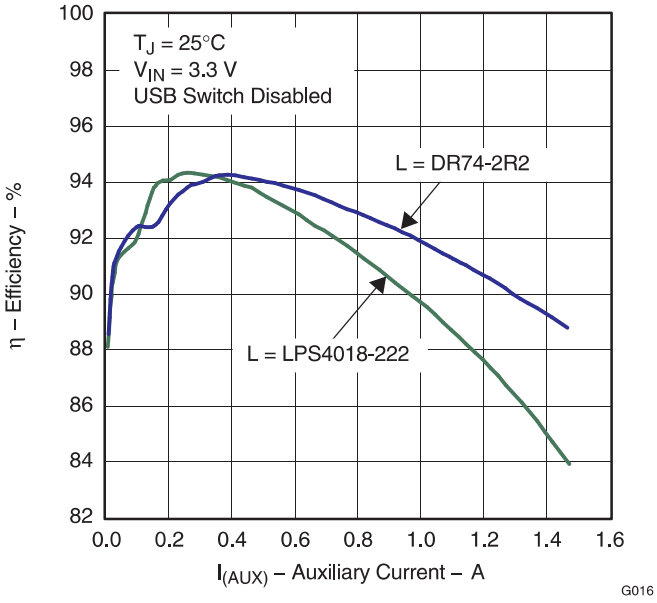


Figure 20. Efficiency vs AUX Current

IN Capacitance

Connect the input capacitance from IN to the reference ground plane. (See the *Layout Recommendations* section for connecting PGND and GND to the ground plane.) Input capacitance reduces the ac voltage ripple on the input rail by providing a low-impedance path for the switching current of the boost converter. The TPS2500 does not have a minimum or maximum input capacitance requirement for operation, but a 10-μF, X7R or X5R ceramic capacitor is recommended for most applications for reasonable input-voltage ripple performance. There are several scenarios where it is recommended to use additional input capacitance:

- The output impedance of the upstream power supply is high, or the power supply is located far from the TPS2500.
- The TPS2500 is tested in a lab environment with long, inductive cables connected to the input, and transient voltage spikes could exceed the absolute maximum voltage rating of the device.
- The device is operating in Eco-mode control scheme near V_{IN} = 1.8 V, where insufficient input capacitance may cause the input ripple voltage to fall below the minimum 1.75-V (typical) UVLO circuit, causing device turnoff.

Additionally, it is good engineering practice to use an additional 0.1-μF ceramic decoupling capacitor close to the IC to prevent unwanted high-frequency noise from coupling into the device.

AUX Capacitance

Connect the boost-converter output capacitance from AUX to the reference ground plane. The AUX capacitance controls the ripple voltage on the AUX rail and provides a low-impedance path for the switching and transient-load currents of the boost converter. It also sets the location of the output pole in the control loop of the boost converter. There are limitations to the minimum and maximum capacitance on AUX. The recommended minimum capacitance on AUX is a 22-μF, X5R or X7R ceramic capacitor. A 10-V rated ceramic capacitor is recommended to minimize the capacitance derating loss due to dc bias applied to the capacitor. The low ESR of the ceramic capacitor minimizes ripple voltage and power dissipation from the large, pulsating currents of the boost converter and provides adequate phase margin across all recommended operating conditions.

In some applications, it is desirable to add additional AUX capacitance. Additional AUX capacitance reduces transient undershoot/overshoot voltages due to load steps and reduces AUX ripple in the Eco-mode control scheme. Adding AUX capacitance changes the control loop, resulting in reduced phase margin, so it is recommended that no more than 220 μF of additional capacitance be added in parallel to the 22-μF ceramic capacitor. The combined output capacitance on AUX and USB should not exceed 500 μF.

USB Capacitance

Connect the USB capacitance from USB to the reference ground plane. The USB capacitance is on the output of the power switch and provides energy for transient load steps. The TPS2500 does not require any USB capacitance for operation. Additional capacitance can be added on USB, but it is recommended to not exceed 220 μF to maintain adequate phase margin for the boost converter control loop. The combined output capacitance on AUX and USB should not exceed 500 μF. USB applications require a minimum of 120 μF on downstream-facing ports.

ILIM and $\overline{\text{FAULT}}$ Resistors

Connect the ILIM resistor from ILIM to the reference ground plane. The ILIM resistor programs the current-limit threshold of the USB power switch (see the *Programming the Current-Limit Threshold Resistor* section). The ILIM pin is the output of an internal linear regulator that provides a fixed 400-mV output. The recommended nominal resistor value using 1% resistors on ILIM is 16.1 kΩ ≤ R_{ILIM} ≤ 200 kΩ. This range should be adjusted accordingly if 1% resistors are not used. Do not overdrive ILIM with an external voltage or connect directly to GND. Connect the ILIM resistor as close to the TPS2500 as possible to minimize the effects of parasitics on device operation. Do not add external capacitance on the ILIM pin. The ILIM pin should not be left floating.

Connect the $\overline{\text{FAULT}}$ resistor from the $\overline{\text{FAULT}}$ pin to an external voltage source such as V_{AUX} or V_{IN}. The $\overline{\text{FAULT}}$ pin is an open-drain output capable of sinking a maximum current of 10 mA continuously. The $\overline{\text{FAULT}}$ resistor should be sized large enough to limit current to under 10 mA continuously. Do not tie $\overline{\text{FAULT}}$ directly to an external voltage source. The maximum recommended voltage on $\overline{\text{FAULT}}$ is 6.5 V. The $\overline{\text{FAULT}}$ pin can be left floating if not used.

Power Dissipation

Power dissipation is an important consideration in any power device with integrated MOSFETs. Although there are internal thermal sensors that disable the device in the event of an overtemperature condition, it is still good design practice to calculate the maximum junction temperature and to maintain the maximum junction temperature under the recommended maximum of 125 °C. There are many ways to approximate the junction temperature of the device. One method is to calculate the junction temperature rise by multiplying the power dissipation of the device by the thermal resistance of the device package. The absolute junction temperature is approximated by the addition of the ambient temperature plus the calculated junction temperature rise: $T_J = T_A + (P_{DISS} \times \theta_{JA}) \leq 125°C$

where T_A and T_J are in °C, θ_{JA} is in °C/W, and P_{DISS} is in W.

The maximum ambient temperature is often an application-specific requirement, such as 85°C maximum. The thermal resistance is mainly a function of the device package but is impacted by system-level considerations such as layout, heatsinking from the surrounding copper pours, the number of board layers, copper thickness, airflow, and surrounding power-dissipating devices (e.g., the power inductor). External equipment such as a thermal camera can help assess the overall thermal performance of a design. The thermal resistance value of 41.6 °C/W from the *Dissipation Ratings* table can be used as an initial estimate. The power dissipation of the device is the sum of the power dissipation in the boost converter plus the power dissipation in the USB power switch. This can be approximated by:

$$P_{DISS} = V_{AUX} \times (I_{AUX} + I_{USB}) \left(\frac{1}{\eta} - 1 \right) + I_{USB}^2 \times r_{USB}$$

where P_{DISS} is in W, V_{AUX} is in V, I_{AUX} and I_{USB} are in A, η is the efficiency of the boost converter, and r_{USB} is in Ω. I_{AUX} is the additional current powering auxiliary loads and does not include any current powering the USB load. Efficiency can be approximated from the efficiency graphs in the *Application Curves* section. This approach may be slightly pessimistic because it does not separate any power losses in the inductor from overall converter efficiency.

Layout Recommendations

Layout is an important design step due to the high switching frequency of the boost converter. Careful attention must be applied to the PCB layout to ensure proper function of the device and to obtain the specified performance. Potential issues resulting from poor layout techniques include wider line and load regulation tolerances, EMI noise issues, stability problems, and USB current-limit shifts. It is critical to provide a low-impedance ground path that minimizes parasitic inductance. Wide and short traces should be used in the high-current paths, and components should be placed as close to the device as possible.

Grounding is an important part of the layout. The device has a PGND and a GND pin. The GND pin is the quiet analog ground of the device and should have its own separate ground pour; connect the quiet signals to GND including the R_{ILIM} resistor and any input decoupling capacitors to the GND pour. It is important that the R_{ILIM} resistor be tied to a quiet ground to avoid unwanted shifts in the current-limit threshold. The PGND pin is the high-current power-stage ground; the ground pours of the output (AUX) and bulk input capacitors should be tied to PGND. PGND and GND should to be tied together in one location at the IC thermal pad, creating a star-point ground.

The output filter of the boost converter is also critical for layout. The inductor and AUX capacitors should be placed to minimize the area of current loop through AUX–PGND–SW.

The layout for the TPS2500EVM evaluation board (HPA337) is shown in Figure 21 and should be followed as closely as possible for best performance. The key components are inside the white silkscreen box.

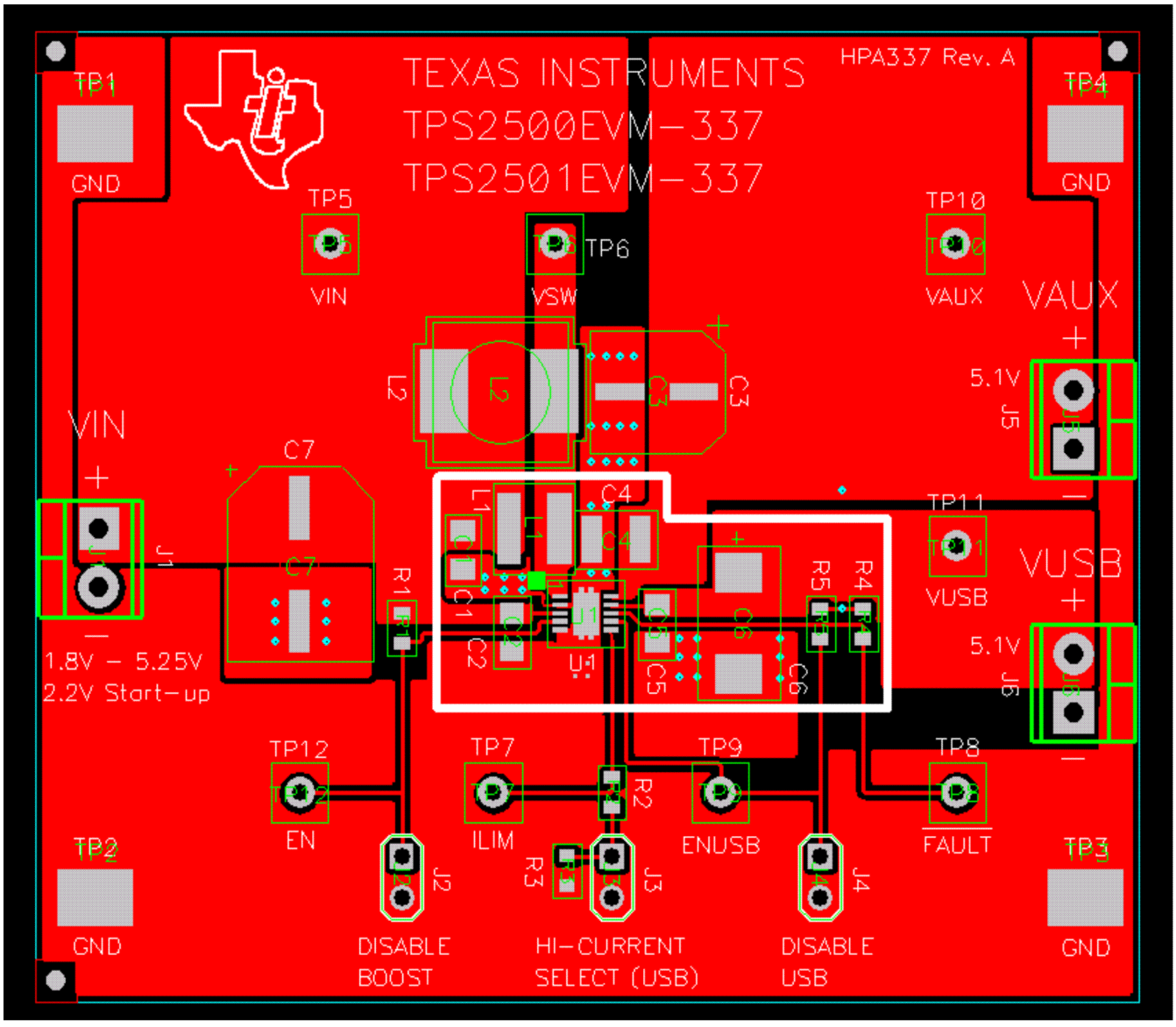


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Figure 21. Recommended Layout, TPS2500EVM (HPA337) Evaluation Board

APPLICATION INFORMATION

Step-by-Step Design Procedure

The following design procedure provides an example for selecting component values for the TPS2500.

The following design parameters are needed as inputs to the design process.

- Input voltage range
- Output voltage on AUX
- Input ripple voltage
- Output ripple voltage on AUX
- Output current rating of AUX rail
- Output current rating of USB rail
- Nominal efficiency target
- Operating frequency

A power inductor, input and output filter capacitors, and current-limit threshold resistor are the only external components required to complete the TPS2500 boost-converter design. The input ripple voltage, AUX ripple voltage, and total output current affect the selection of these components.

This design example assumes the following input specifications.

PARAMETER	EXAMPLE VALUE
Input voltage range (V_{IN})	2.7 V to 4.2 V
AUX voltage (V_{AUX})	5.1 V (internally fixed)
Input ripple voltage (ΔV_{IN})	15 mV
AUX ripple voltage (ΔV_{AUX})	50 mV
AUX current (I_{AUX})	0.5 A
USB current (I_{USB})	0.5 A
Total current ($I_{TOTAL} = I_{AUX} + I_{USB}$)	1 A
Efficiency target, nominal	90%
Switching frequency (f)	1 MHz

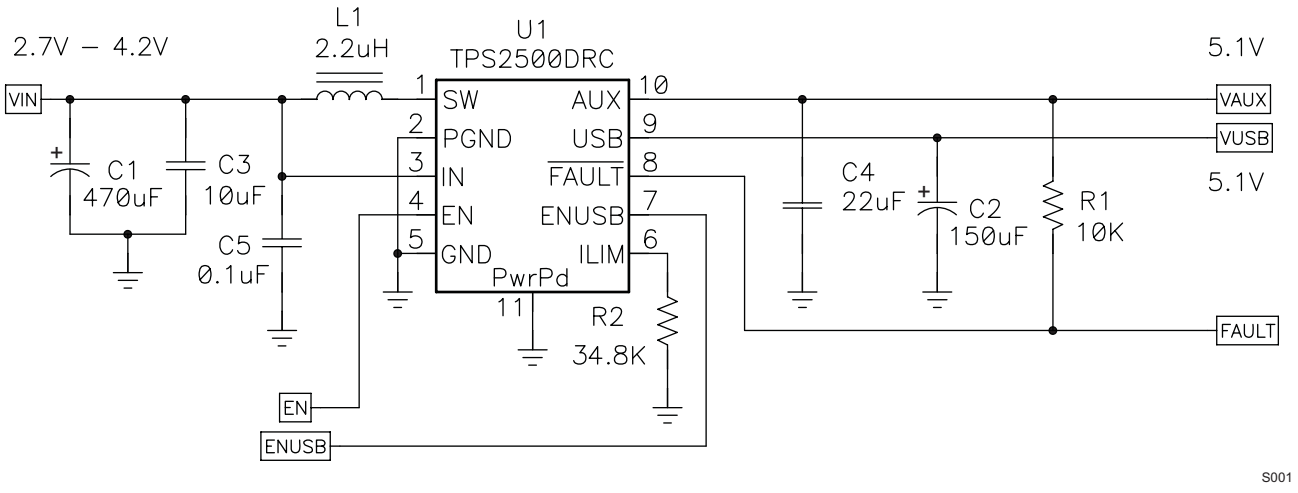


Figure 22. Reference Schematic

Switching Frequency

The switching frequency of the TPS2500 is internally fixed at 1 MHz.

AUX Voltage

The AUX voltage of the TPS2500 is internally fixed at 5.1 V.

Determine Maximum Total Current (I_{AUX} + I_{USB})

Using Figure 12, the maximum total current at V_{IN} = 2.7 V is 1 A using the conservative line. The design requirements are met for this application.

Power Inductor

The inductor ripple current, Δi, should be at least 20% of the average inductor current to avoid erratic operation of the peak-current-mode PWM controller. Assume an inductor ripple current, Δi, which is 30% of the average inductor current and a power-converter efficiency, η, of 90%. Using the minimum input voltage, the average inductor current at V_{IN} = 2.7 V is:

$$I_{IN} = \frac{V_{AUX} \times I_{TOTAL}}{V_{IN} \times \eta} = \frac{5.1\,V \times 1\,A}{2.7\,V \times 0.9} = 2.1\,A$$

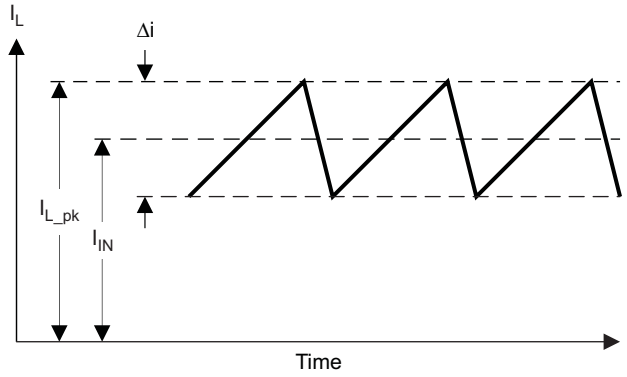


Figure 23. Waveform of Current in Boost Inductor

The corresponding inductor ripple current is:

$$\Delta i = 0.3 \times I_{IN} = 0.3 \times 2.1\ A = 630\ mA$$

Verify that the peak inductor current is less than the 3-A peak switch current:

$$I_{L\_pk} = I_{IN} + \frac{\Delta i}{2} = 2.42\ A < 3\ A$$

The following equation estimates the duty cycle of the low-side PWM MOSFET:

$$D = \frac{t_{on}}{t_{on} + t_{off}} = \left[\frac{V_{AUX} - V_{IN} + I_{IN} \times (R_{SYNC} + R_L)}{V_{AUX} + I_{IN} \times (R_{SYNC} - R_{PWM})} \right]$$

$$= \left[\frac{5.1\,V - 2.7\,V + 2.1\,A \times (0.1\,\Omega + 0.07\,\Omega)}{5.1\,V + 2.1\,A \times (0.1\,\Omega - 0.1\,\Omega)} \right] = 0.54$$

where R_{PWM} is the low-side control MOSFET on-resistance, R_{SYNC} is the high-side synchronous MOSFET on-resistance, and R_L is an estimate of the inductor dc resistance.

The following equation calculates the recommended inductance for this design.

$$L = \frac{V_{IN} \times D}{f \times \Delta i} = \frac{2.7\,V \times 0.54}{1 \times 10^6\,Hz \times 0.63\,A} = 2.31\,\mu H$$

The peak inductor current is:

$$I_{L\_pk} = I_{IN} + \frac{\Delta i}{2} = 2.42\ A$$

The rms inductor current is:

$$I_{L\_RMS} = \sqrt{I_{IN}^2 + \left(\frac{\Delta i}{2 \cdot \sqrt{3}}\right)^2} = \sqrt{(2.1\ A)^2 + \left(\frac{0.63\ A}{2 \cdot \sqrt{3}}\right)^2} = 2.11\ A$$

Select a Coilcraft LPS4018-222ML inductor. This 2.2-µH inductor has a saturation current rating of 2.7 A and an rms current rating of 2.3 A. See the *Component Recommendations* section for specific additional information.

Output AUX Capacitor Selection

The AUX output capacitor, C_{AUX}, discharges during the PWM MOSFET on-time, resulting in an output ripple voltage of ΔV_{AUX}. ΔV_{AUX} is largest at maximum load current.

$$C_{AUX} = \frac{D \times I_{TOTAL}}{f \times \Delta V_{AUX}}$$

$$C_{o\_min} = \frac{0.54 \times 1\ A}{1 \times 10^6\ Hz \times 50\ mV} = 10.8\ \mu F$$

Ceramic capacitors exhibit a dc bias effect, whereby the capacitance falls with increasing bias voltage. The effect is worse for capacitors in smaller case sizes and lower voltage ratings. X5R and X7R capacitors exhibit less dc bias effect than Y5V and Z5U capacitors.

Select a TDK C3225X5R1A226M 22-µF, 10-V X5R ceramic capacitor to allow for a 50% drop in capacitance due to the dc bias effect. See the *Component Recommendations* section for specific additional information.

Output USB Capacitor Selection

The USB output capacitor provides energy during a load step on the USB output. The TPS2500 does not require a USB output capacitor, but many USB applications require that downstream-facing ports be bypassed with a minimum of 120-µF, low-ESR capacitance.

Select a Panasonic EEVFK1A151P 150-µF, 10-V capacitor.

Input Capacitor Selection

The ripple current through the input filter capacitor is equal to the ripple current through the inductor. If the ESL and ESR of the input filter capacitor are ignored, then the required input filter capacitance is:

$$C_{IN} = \frac{\Delta i}{8 \times f \times \Delta V_{IN}} = \frac{630\ mA}{8 \times 1 \times 10^6\ Hz \times 15\ mV} = 5.25\ \mu F$$

Select a TDK C2012X5R1A106K 10-µF, 10-V, X5R, size 805 ceramic capacitor. The capacitance drops 20% at 3.3-V bias, resulting in an effective capacitance of 8 µF.

An additional 0.1-µF ceramic capacitor should be placed locally from IN to GND to prevent noise from coupling into the device if the input capacitor cannot be located physically near to the device.

In applications where long, inductive cables connect the input power supply to the device, additional bulk input capacitance may be necessary to minimize voltage overshoot. See the *Component Recommendations* section for specific additional information.

Current-Limit Threshold Resistor R_{ILIM}

The current-limit threshold I_{OS} of the power switch is externally adjustable by selecting the R_{ILIM} resistor. To eliminate the possibility of false tripping, R_{ILIM} should be selected so that the minimum tolerance of the current-limit threshold is greater than the maximum specified USB load, I_{USB}. For design margin, an additional 10% (50 mA) buffer is added above the maximum continuous load current and minimum current-limit threshold, which sets the minimum desired current-limit threshold at 550 mA.

It is also important to account for I_{OS} shifts due to variation in V_{IN} and I_{AUX}, so by referencing the curves in the *Programming the Current-Limit Threshold Resistor* section (Figure 19, specifically) it can be seen that I_{OS} will shift down by ~50 mA from the V_{IN} = 3.3 V, I_{AUX} = 0 A reference point at our maximum operating conditions of V_{IN} = 4.2 V, I_{AUX} = 500 mA. Select R_{ILIM} so that the minimum current-limit threshold equals 600 mA to ensure a minimum I_{USB} current-limit threshold of 550 mA.

$$R_{ILIM} = \left(\frac{32{,}114}{IOS_{min}}\right)^{\frac{1}{1.114}} = \left(\frac{32{,}114}{600\ mA}\right)^{\frac{1}{1.114}} = 35.62\ k\Omega$$

Choose the next-smaller 1% resistor, which is 34.8 kΩ.

ADDITIONAL DESIGN EXAMPLE

Specific Application Examples

The Table 4 outlines several specific applications and component recommendations for the given electrical specifications.

Table 4. Component Recommendations

Application Example			Electrical Specifications					Component Values				
Description	# of USB Ports	AUX Load (mA)	V_{IN} min (V)	V_{IN} max (V)	I_{AUX} max (mA)	I_{USB} max (mA)	I_{TOTAL} (mA)	Inductor (μH)	C_{IN} (μF)(1)	C_{AUX} (μF)(1)	C_{USB} (μF)(2)	R_{ILIM} (kΩ)
Single-cell lithium ion battery or 3.3-V bus	1	100	2.7	4.2	100	550	650	3.3	10	22	150	30.9
Single-cell lithium ion battery or 3.3-V bus	2	0	2.7	4.2	0	1100	1100	2.2	10	22	150	18.2
Two-cell NiMH battery	1	0	1.8	2.4	0	550	550	2.2	10	22	150	35.7
Single-cell lithium ion battery ORed with 5-V bus	2	0	2.7	5.25	0	1100	1100	2.2	10	22	150	18.2
Single-cell lithium ion battery ORed with 5-V bus	1	200	2.7	5.25	200	550	750	3.3	10	22	150	26.1

(1) Use low-ESR, X5R or X7R ceramic capacitors.
(2) Not required for operation, only required to meet USB 2.0 standard

APPLICATION CURVES

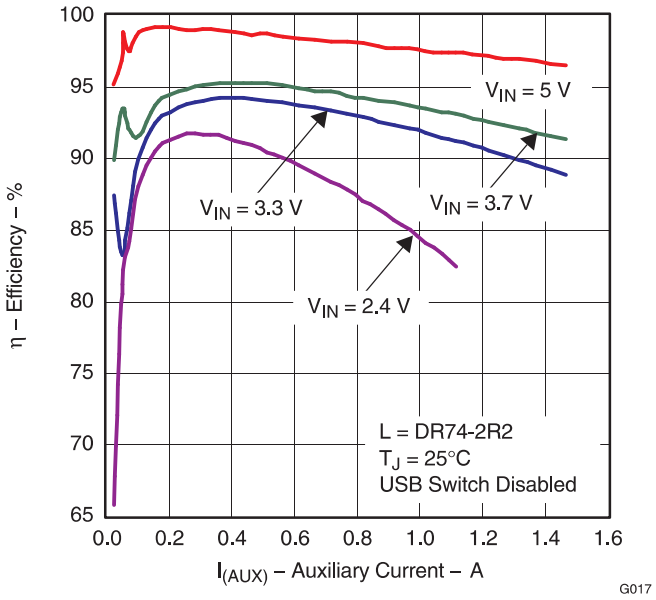


Figure 24. Efficiency vs I_{AUX}, TPS2500 (Eco-mode Control Scheme)

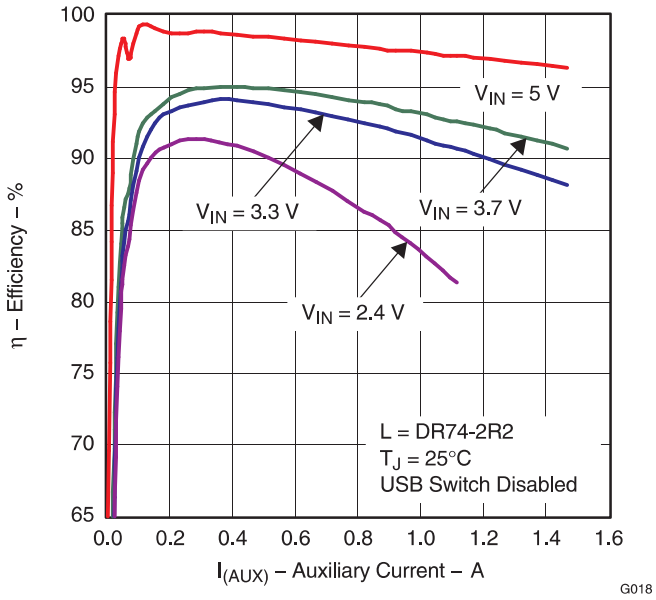


Figure 25. Efficiency vs I_{AUX}, TPS2501 (Forced PWM Mode)

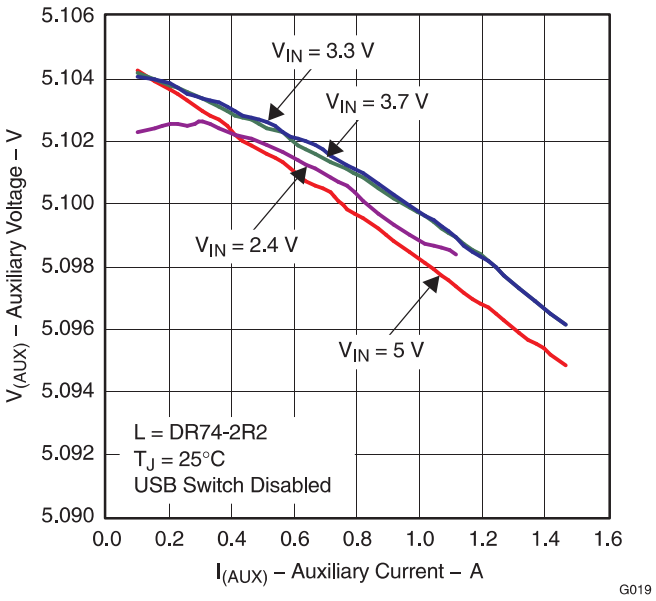


Figure 26. Load Regulation, TPS2500 (Eco-mode Control Scheme)

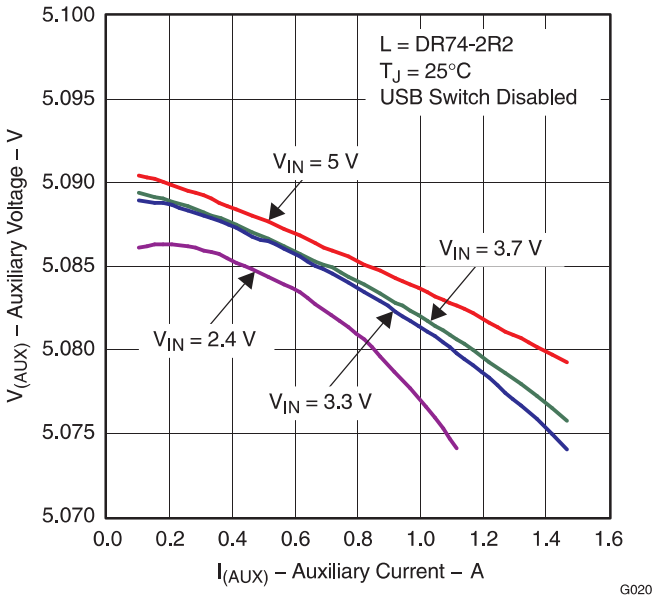


Figure 27. Load Regulation, TPS2501 (Forced PWM Mode)

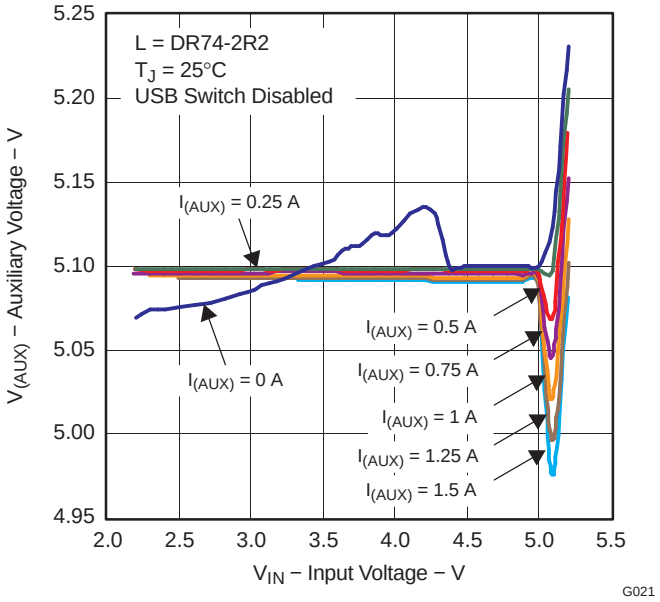


Figure 28. Line Regulation, TPS2500 (Eco-mode Control Scheme)

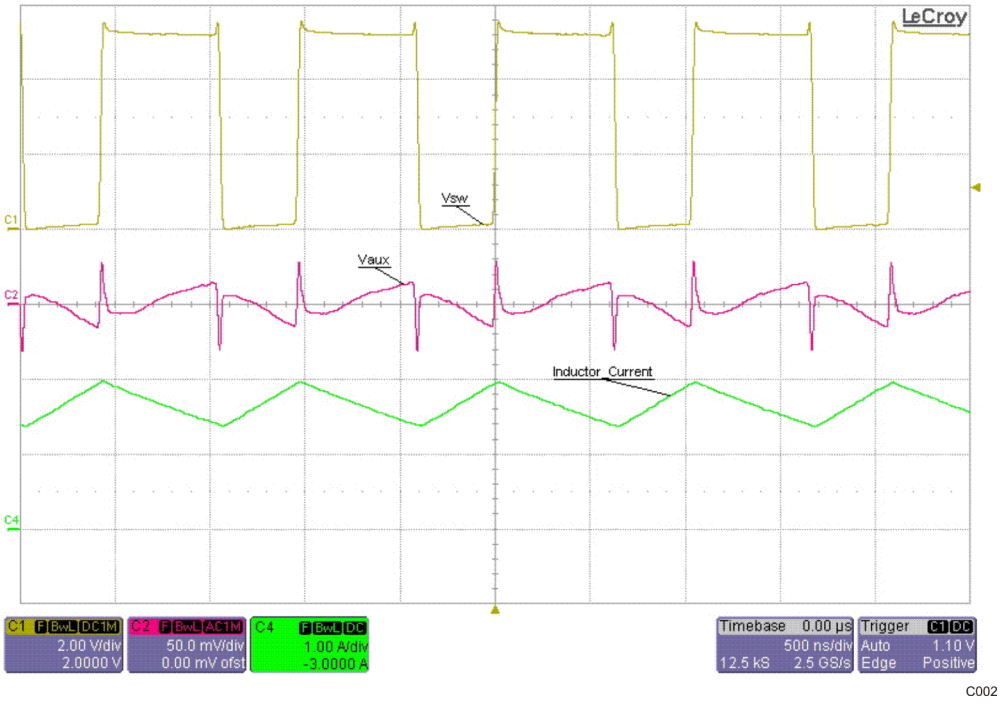


Figure 29. V_{AUX} Ripple, V_{IN} = 3.3 V, I_{AUX} = 1 A

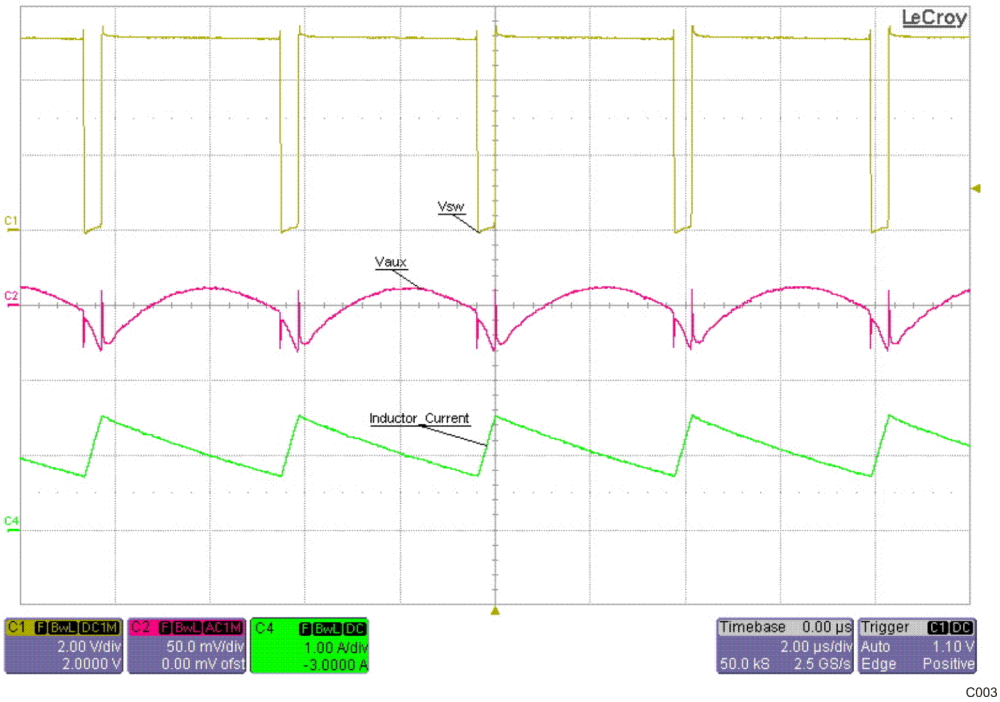


Figure 30. V_{AUX} Ripple, V_{IN} = 4.75 V, I_{AUX} = 1 A

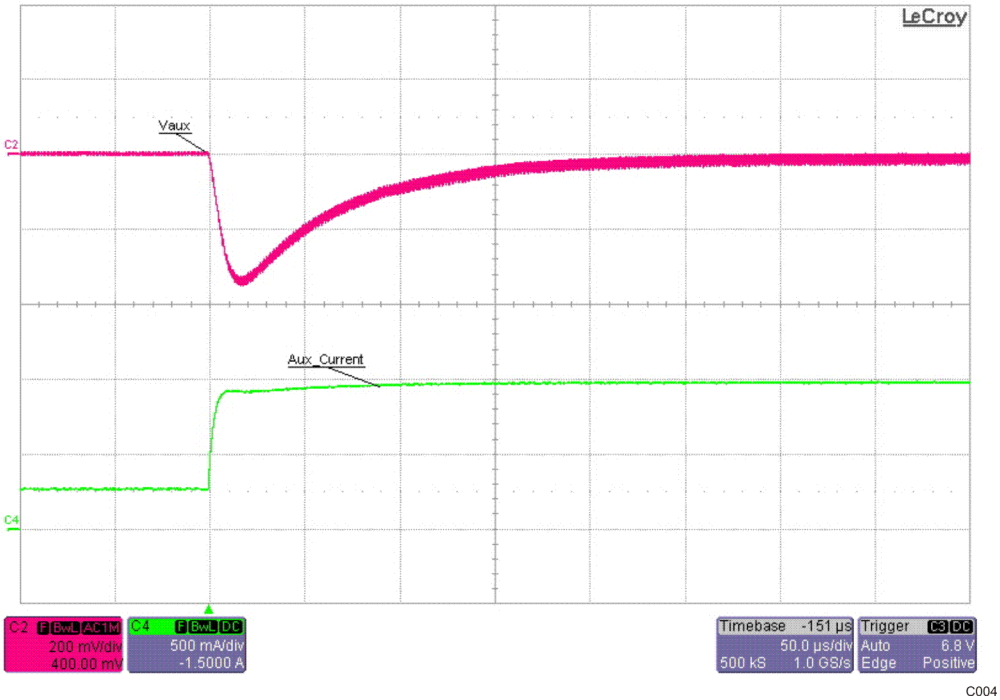


Figure 31. Load Transient, V_{IN} = 3.3 V, I_{AUX} = 0.25 A to 1 A

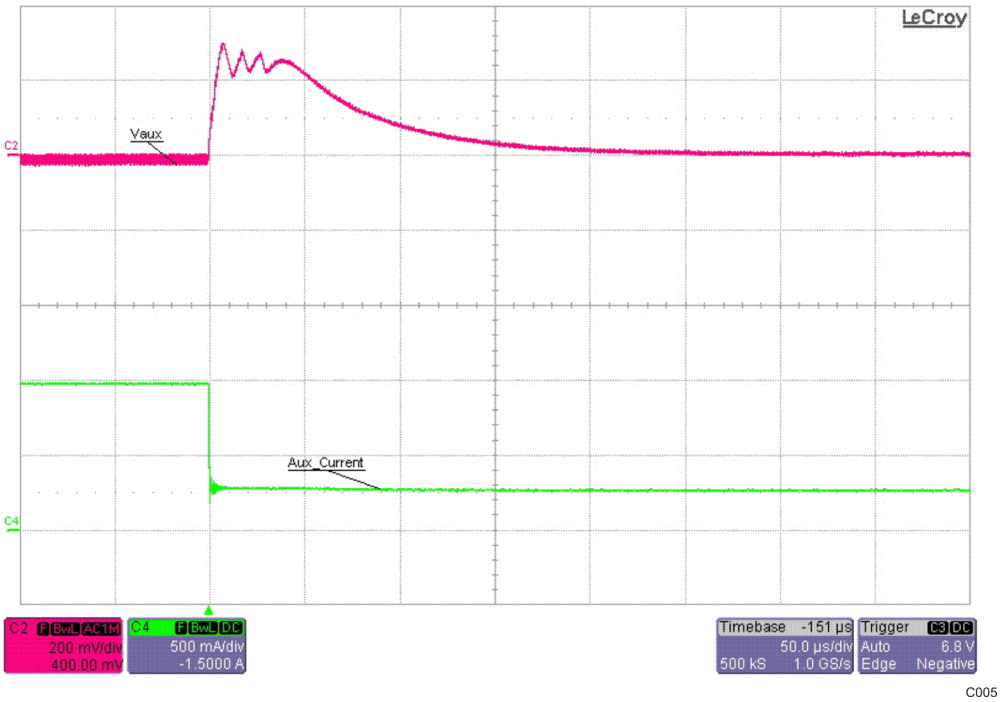


Figure 32. Load Transient, V_{IN} = 3.3 V, I_{AUX} = 1 A to 0.25 A

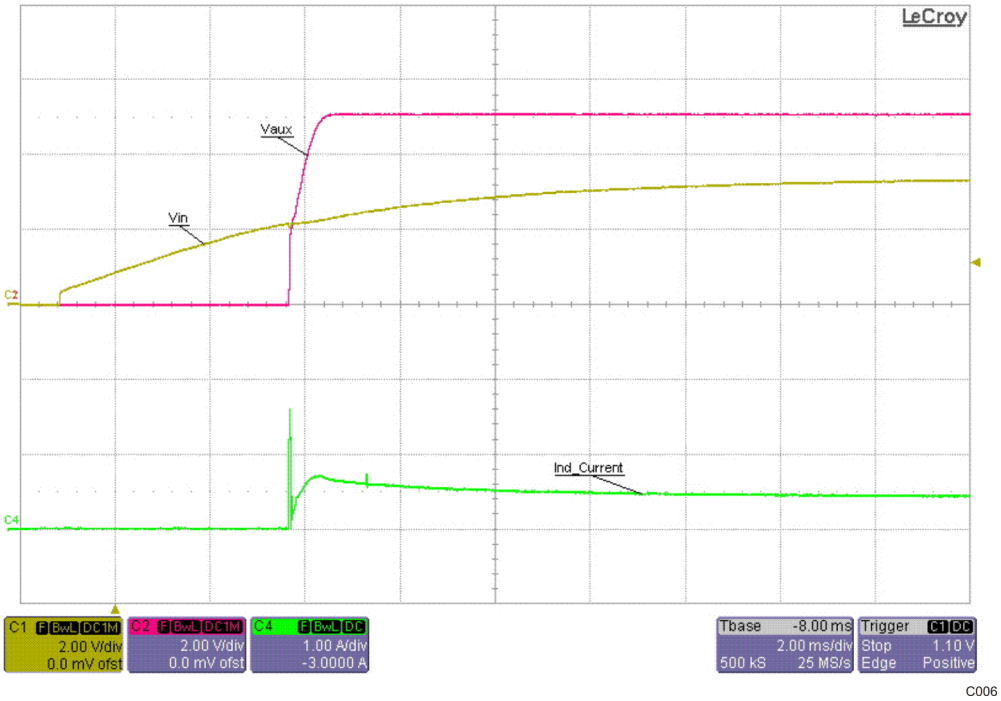


Figure 33. Start-Up, V_{IN} = 3.3 V, I_{AUX} = 0.5 A, USB Switch Disabled

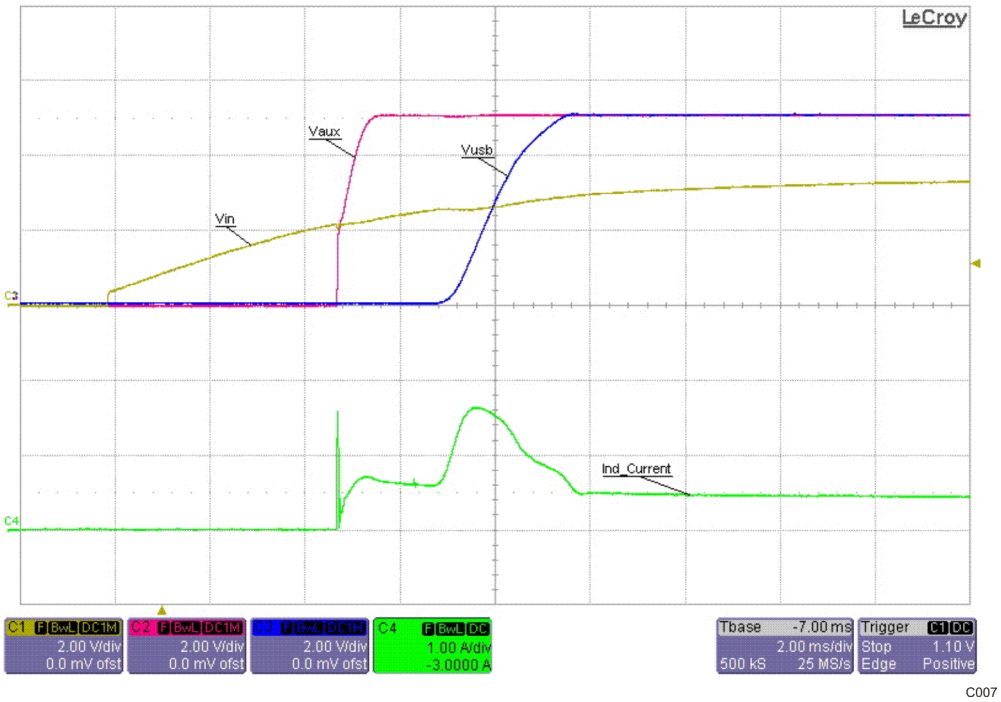


Figure 34. Start-Up, V_{IN} = 3.3 V, I_{AUX} = 0.5 A, USB Switch Enabled

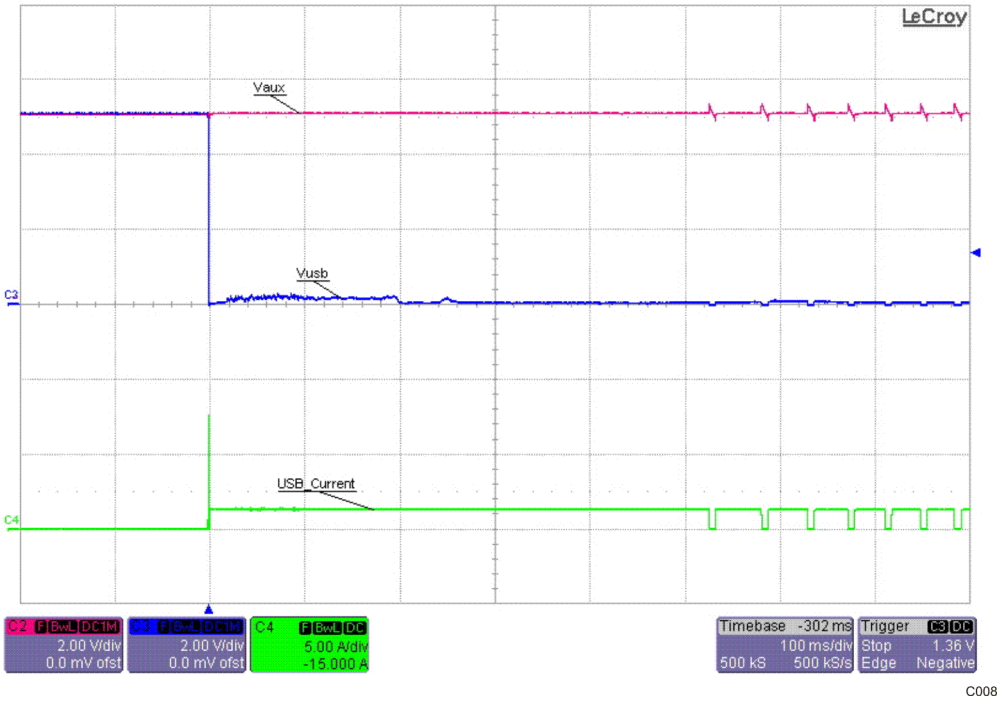


Figure 35. V_{IN} = 3.3 V, Short Applied to V_{USB}

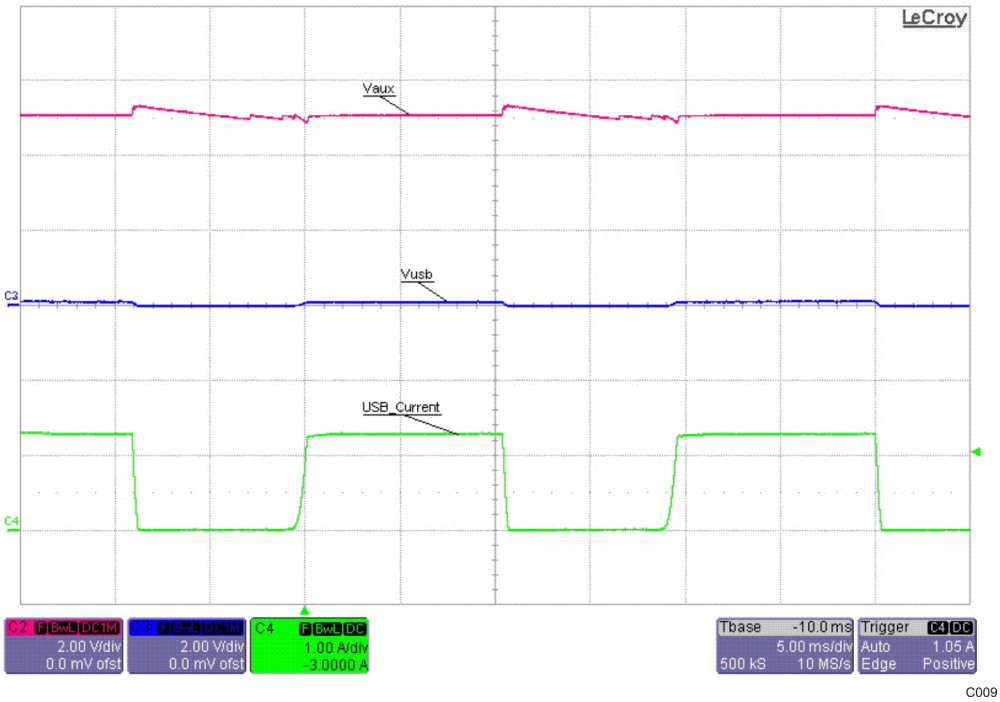


Figure 36. V_{IN} = 3.3 V, USB Switch Thermal Cycle Due to Short on V_{USB}

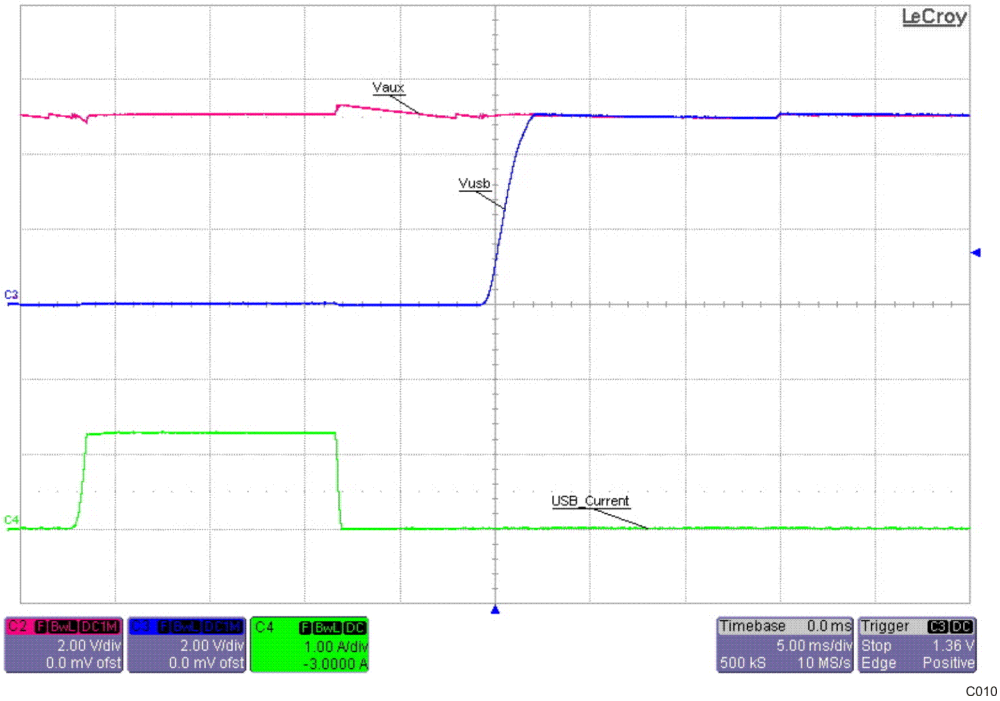


Figure 37. V_{IN} = 3.3 V, Short Removed From V_{USB}

REVISION HISTORY

Changes from Original (October 2008) to Revision A **Page**

- Changed From: Advanced Information To: Production Data 1

Changes from Revision A (August 2009) to Revision B **Page**

- Added SW note to absolute maximum ratings table 2
- Changed from diabled to disabled 12
- Changed Auxiliary Current - mA to Auxiliary Current - A in Figures 20, 24, 25, 26, 27 19

Changes from Revision B (April 2010) to Revision C **Page**

- Deleted Feature Minimal External Components Required 1
- Added Feature UL Listed - File No. E169910 1

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TPS2500DRCR	ACTIVE	SON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	(CHO ~ CHOU)	Samples
TPS2500DRCT	ACTIVE	SON	DRC	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	(CHO ~ CHOU)	Samples
TPS2501DRCR	ACTIVE	SON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OBA	Samples
TPS2501DRCT	ACTIVE	SON	DRC	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OBA	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

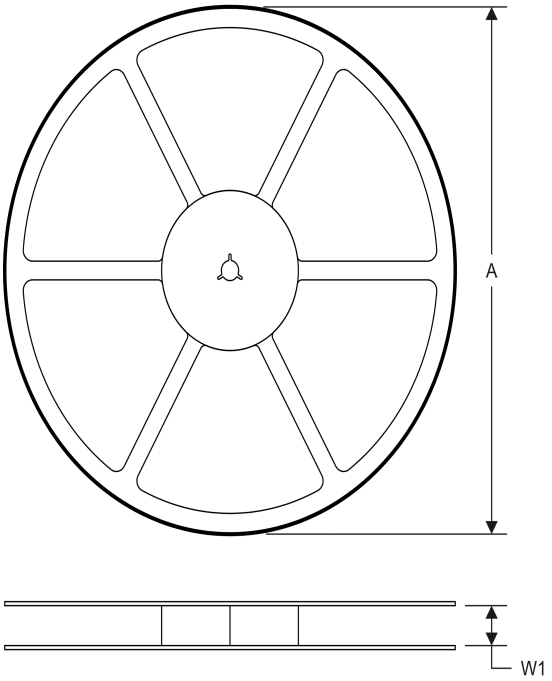
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

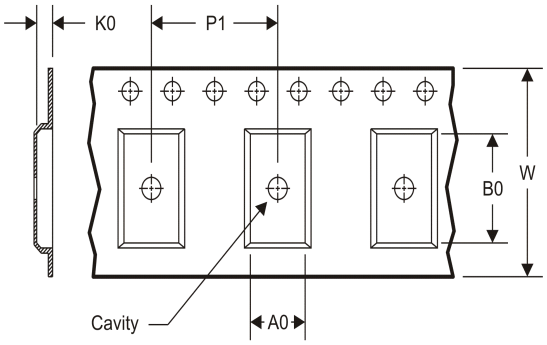
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



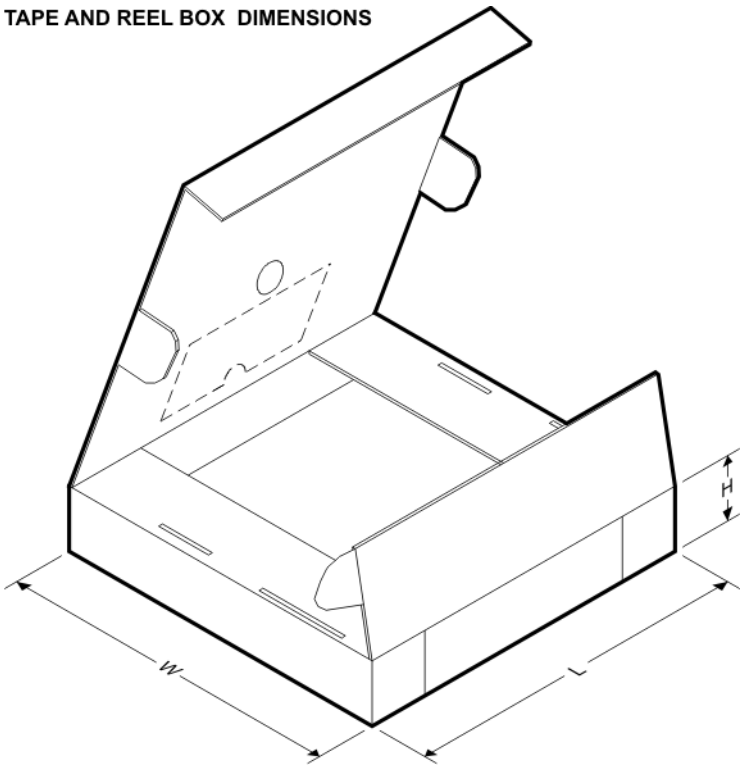
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS2500DRCR	SON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS2500DRCT	SON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS2501DRCR	SON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS2501DRCT	SON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

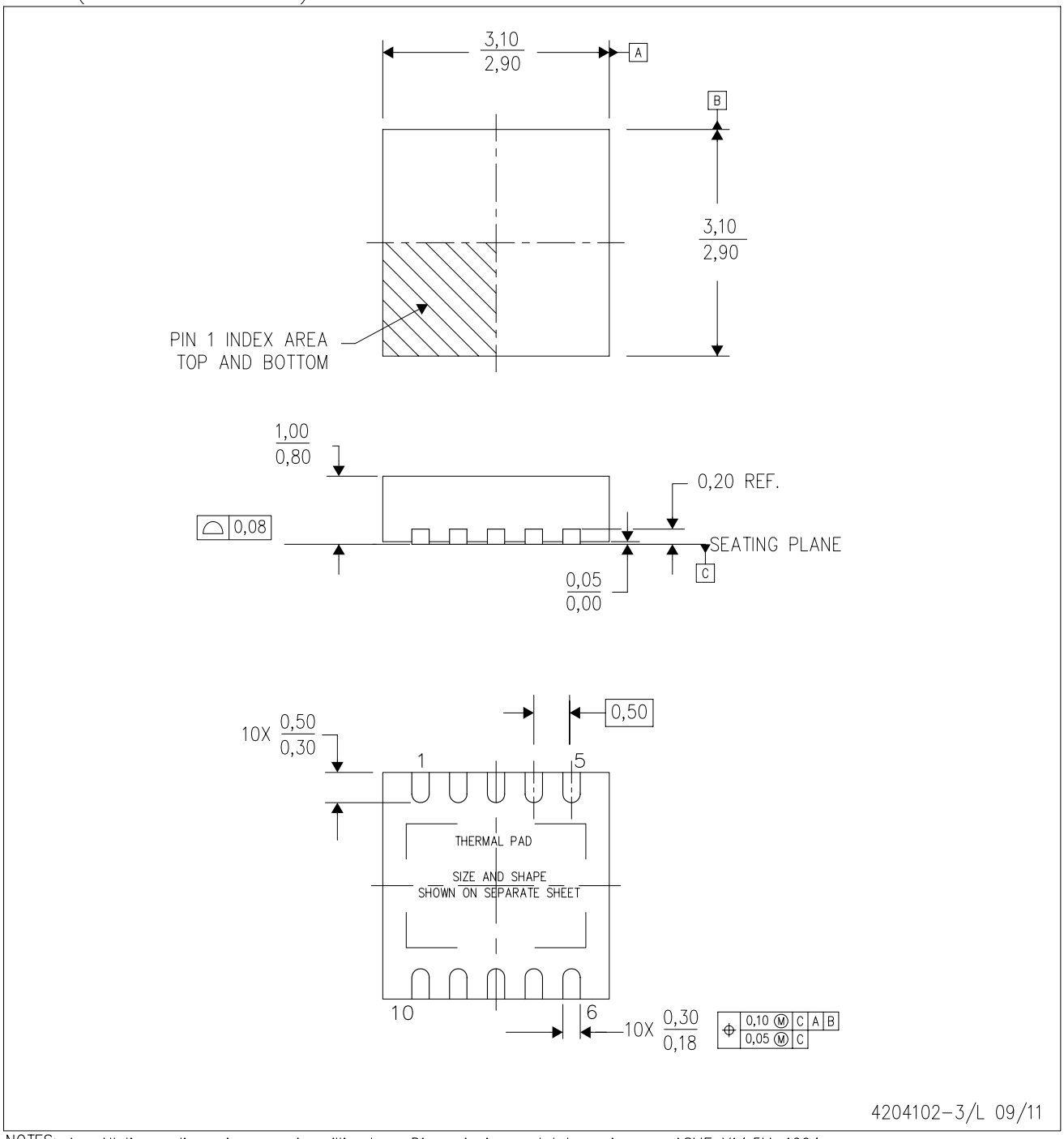
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS2500DRCR	SON	DRC	10	3000	367.0	367.0	35.0
TPS2500DRCT	SON	DRC	10	250	210.0	185.0	35.0
TPS2501DRCR	SON	DRC	10	3000	367.0	367.0	35.0
TPS2501DRCT	SON	DRC	10	250	210.0	185.0	35.0

DRC (S–PVSON–N10) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance, if present.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions, if present

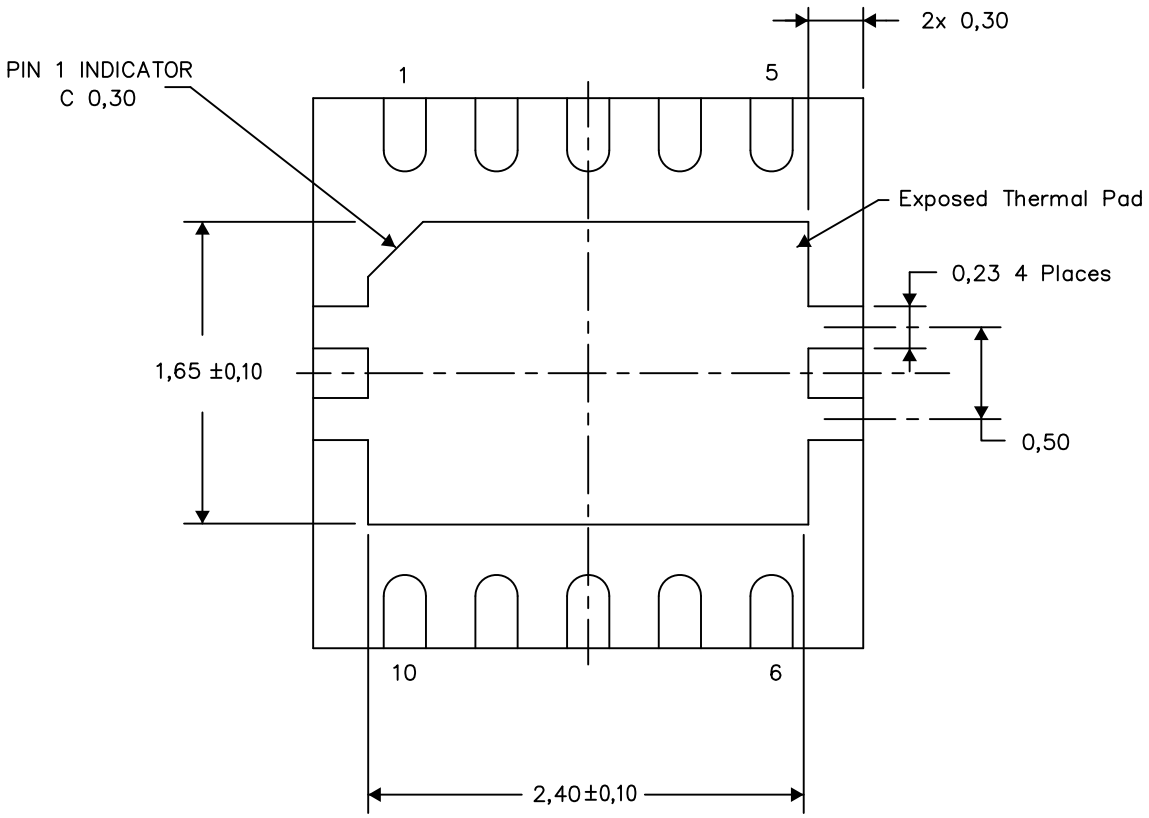
DRC (S–PVSON–N10) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



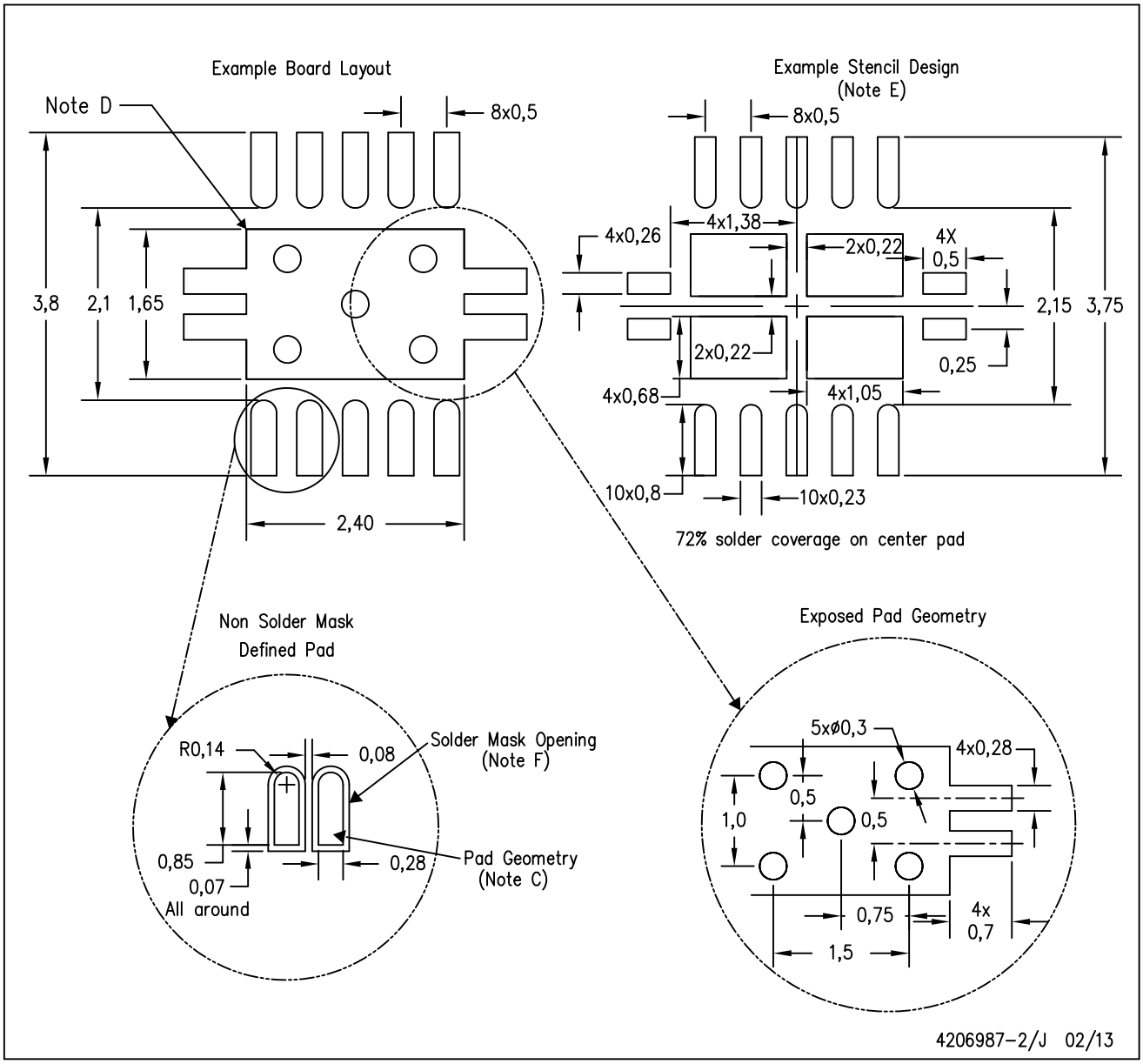
Bottom View

Exposed Thermal Pad Dimensions

4206565–3/R 03/13

NOTE: A. All linear dimensions are in millimeters

DRC (S–PVSON–N10) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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