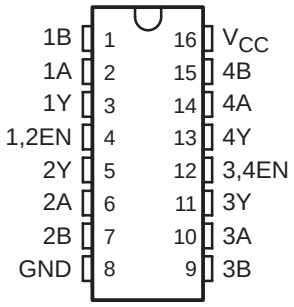
- **Designed for TIA/EIA-485, TIA/EIA-422, and ISO 8482 Applications**
- **Signaling Rate[1] Exceeding 50 Mbps**
- **Fail-Safe in Bus Short-Circuit, Open-Circuit, and Idle-Bus Conditions**
- **ESD Protection on Bus Inputs 6 kV**
- **Common-Mode Bus Input Range −7 V to 12 V**
- **Propagation Delay Times <16 ns**
- **Low Standby Power Consumption <20 μA**
- **Pin-Compatible Upgrade for MC3486, DS96F175, LTC489, and SN75175**

SN65LBC175A (Marked as 65LBC175A)
SN75LBC175A (Marked as 75LBC175A)
D or N PACKAGE
(TOP VIEW)

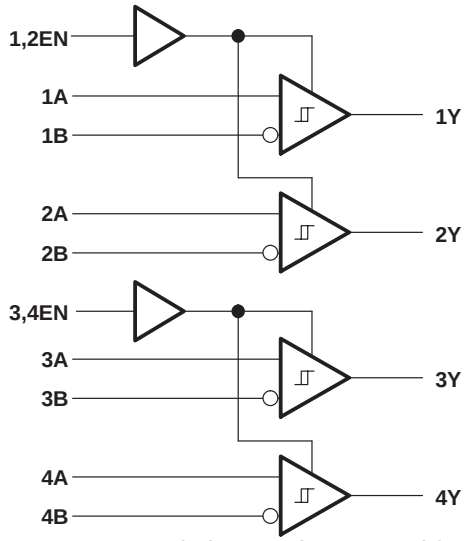


description

The SN65LBC175A and SN75LBC175A are quadruple differential line receivers with 3-state outputs, designed for TIA/EIA-485 (RS-485), TIA/EIA-422 (RS-422), and ISO 8482 (Euro RS-485) applications.

These devices are optimized for balanced multipoint bus communication at data rates up to and exceeding 50 million bits per second. The transmission media may be twisted-pair cables, printed-circuit board traces, or backplanes. The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media and the noise coupling to the environment.

logic diagram



Each receiver operates over a wide range of positive and negative common-mode input voltages, and features ESD protection to 6 kV, making it suitable for high-speed multipoint data transmission applications in harsh environments. These devices are designed using LinBiCMOS™, facilitating low power consumption and inherent robustness.

Two EN inputs provide pair-wise enable control, or these can be tied together externally to enable all four drivers with the same signal.

The SN75LBC175A is characterized for operation over the temperature range of 0°C to 70°C. The SN65LBC175A is characterized over the temperature range from −40°C to 85°C.

LinBiCMOS is a trademark of Texas Instruments.

[1]The signaling rate of a line is the number of voltage transitions that are made per second expressed in the units bps (bits per second).

FUNCTION TABLE
(each receiver)

DIFFERENTIAL INPUTS A – B (V_{ID})	ENABLE EN	OUTPUT Y
$V_{ID} \le -0.2$ V	H	L
-0.2 V $< V_{ID} < -0.01$ V	H	?
-0.01 V $\le V_{ID}$	H	H
X	L	Z
X	OPEN	Z
Short circuit	H	H
Open circuit	H	H

H = high level, L = low level, X = irrelevant, Z = high impedance (off), ? = indeterminate

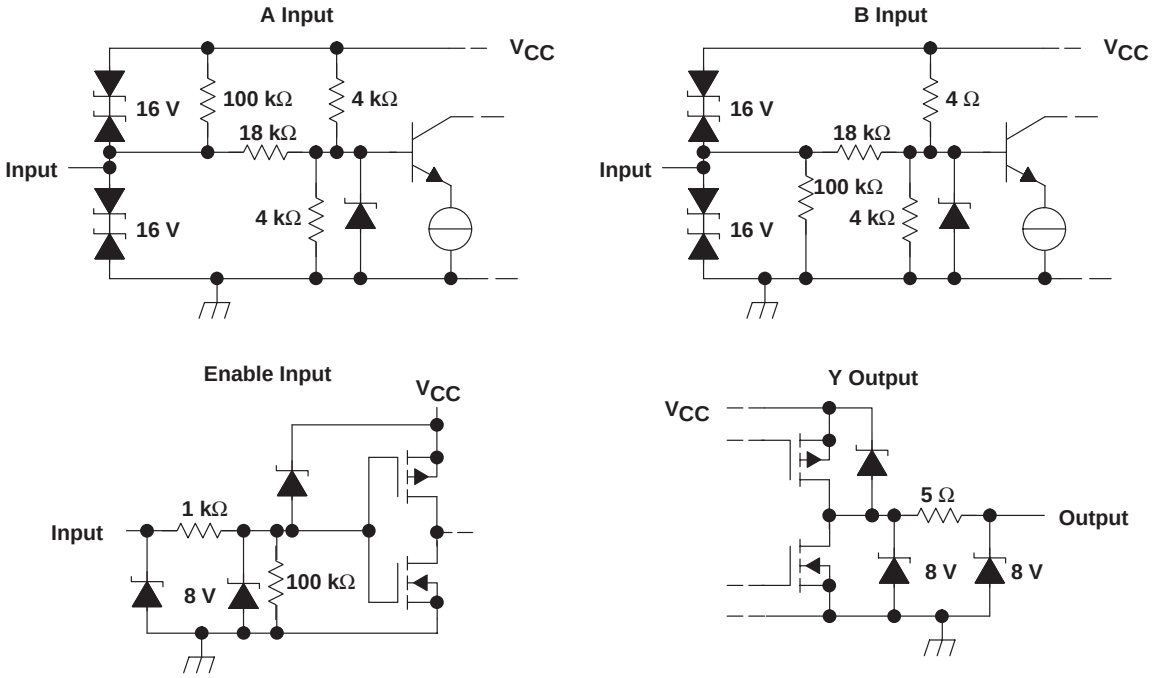
AVAILABLE OPTIONS

T_A	PACKAGE	
	PLASTIC SMALL OUTLINE† (JEDEC MS-012)	PLASTIC DUAL-IN-LINE (JEDEC MS-001)
0°C to 70°C	SN75LBC175AD	SN75LBC175AN
−40°C to 85°C	SN65LBC175AD	SN65LBC175AN

† Add an R suffix for taped and reeled

† For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

equivalent input and output schematic diagrams



absolute maximum ratings† over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V_{CC} (see Note 1) . . . . . −0.3 V to 6 V
Voltage range at any bus input (steady state), A and B . . . . . −10 V to 15 V
Voltage range at any bus input (transient pulse through 100 Ω, see Figure 5) . . . . . −30 V to 30 V
Voltage input range at 1,2EN and 3,4EN, V_I . . . . . −0.5 V to V_{CC} + 0.5 V
Receiver output current, I_O . . . . . ±10 mA
Electrostatic discharge:
Human body model (see Note 2): A and B to GND . . . . . 6 kV
All pins . . . . . 5 kV
Charged-device model (see Note 3): All pins . . . . . 2 kV
Continuous power dissipation . . . . . See Power Dissipation Rating Table

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential I/O bus voltages, are with respect to GND, and are steady-state (unless otherwise specified).
2. Tested in accordance with JEDEC Standard 22, Test Method A114-A.
3. Tested in accordance with JEDEC Standard 22, Test Method C101.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR† ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	1080 mW	8.7 mW/°C	690 mW	560 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW

† This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Voltage at any bus terminal	A, B	−7		12	V
High-level input voltage, V_{IH}	EN	2		V_{CC}	V
Low-level input voltage, V_{IL}	EN	0		0.8	V
Output current	Y	−8		8	mA
Operating free-air temperature, T_A	SN75LBC175A	0		70	°C
	SN65LBC175A	−40		85	°C

electrical characteristics over recommended operating conditions

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IT+}	Positive-going differential input voltage threshold		−7 V ≤ V_{CM} ≤ 12 V (V_{CM} = (V_A + V_B) / 2)			−80	−10	mV
V_{IT-}	Negative-going differential input voltage threshold				−200	−120		
V_{HYS}	Hysteresis voltage (V_{IT+} − V_{IT-})					−40		mV
V_{IK}	Input clamp voltage		I_I = −18 mA		−1.5	−0.8		V
V_{OH}	High-level output voltage		V_{ID} = 200 mV, I_{OH} = −8 mA	See Figure 1	2.7	4.8		V
V_{OL}	Low-level output voltage		V_{ID} = −200 mV, I_{OL} = 8 mA			0.2	0.4	
I_{OZ}	High-impedance-state output current		V_O = 0 V to V_{CC}		−1		1	µA
I_I	Line input current		Other input at 0 V, V_{CC} = 0 V or 5 V	V_I = 12 V			0.9	mA
				V_I = −7 V	−0.7			
I_{IH}	High-level input current	Enable inputs					100	µA
I_{IL}	Low-level input current				−100			µA
R_I	Input resistance		A, B		12			kΩ
I_{CC}	Supply current		V_{ID} = 5 V	1,2EN, 3,4EN at 0 V			20	mA
			No load	1,2EN, 3,4EN at V_{CC}		11	16	mA

† All typical values are at V_{CC} = 5 V and 25°C.

switching characteristics over recommended operating conditions

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_r	Output rise time	V_{ID} = −3 V to 3 V, See Figure 2		2	4	ns
t_f	Output fall time			2	4	ns
t_{PLH}	Propagation delay time, low-to-high level output		9	12	16	ns
t_{PHL}	Propagation delay time, high-to-low level output		9	12	16	ns
t_{PZH}	Propagation delay time, high-impedance to high-level output	See Figure 3		27	38	ns
t_{PHZ}	Propagation delay time, high-level to high-impedance output			7	16	ns
t_{PZL}	Propagation delay time, high-impedance to low level output	See Figure 4		29	38	ns
t_{PLZ}	Propagation delay time, low-level to high-impedance output			12	16	ns
$t_{sk(p)}$	Pulse skew (| (t_{PLH} − t_{PHL}) |)			0.2	1	ns
$t_{sk(o)}$	Output skew (see Note 4)				2	ns
$t_{sk(pp)}$	Part-to-part skew (see Note 5)				2	ns

† All typical values are at V_{CC} = 5 V and 25°C.

NOTES: 4. Outputs skew ($t_{sk(o)}$) is the magnitude of the time delay difference between the outputs of a single device with all of the inputs connected together.

5. Part-to-part skew ($t_{sk(pp)}$) is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same input signals, the same supply voltages, at the same temperature, and have identical packages and test circuits.

PARAMETER MEASUREMENT INFORMATION

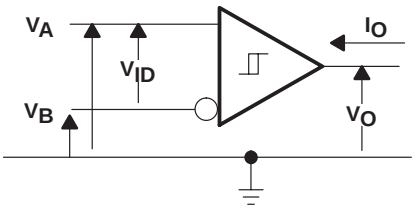
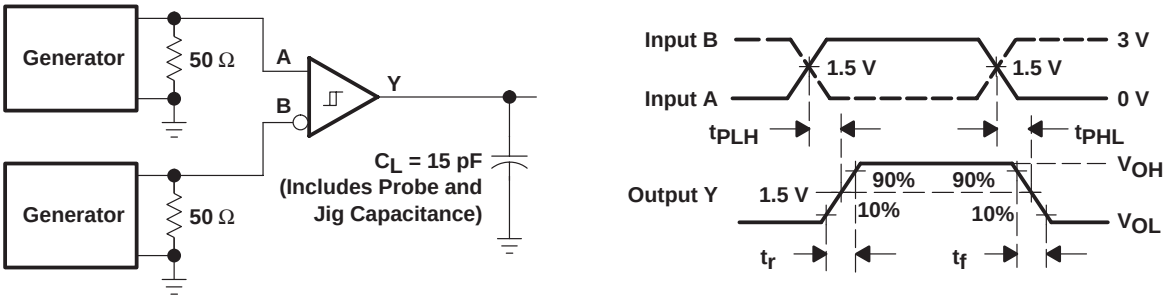
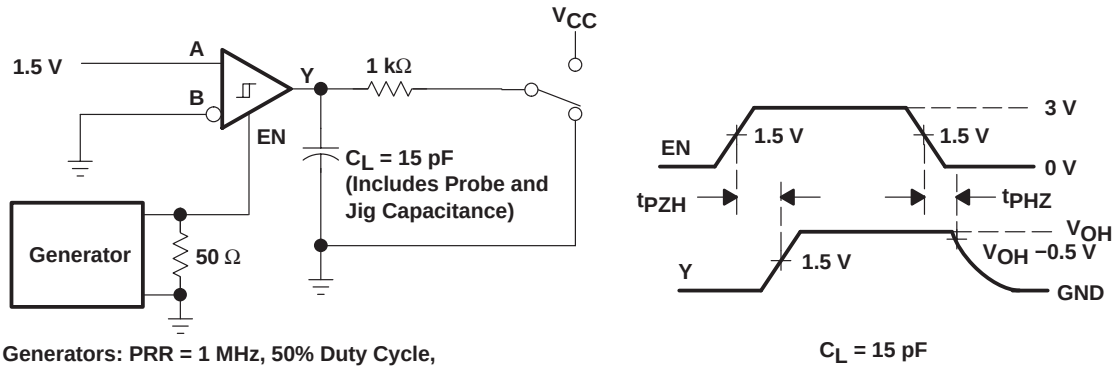


Figure 1. Voltage and Current Definitions



Generators: PRR = 1 MHz, 50% Duty Cycle,
t_r <6 ns, Z_O = 50 Ω

Figure 2. Switching Test Circuit and Waveforms

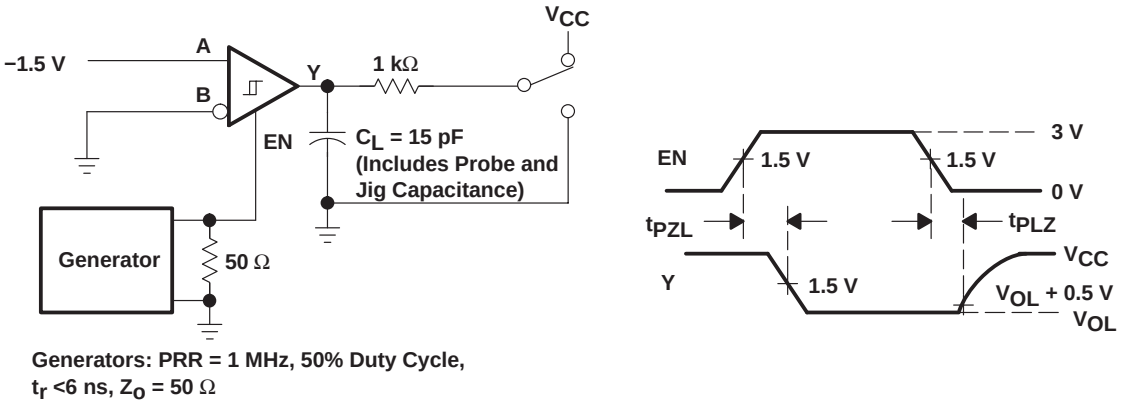


Generators: PRR = 1 MHz, 50% Duty Cycle,
t_r <6 ns, Z_O = 50 Ω

C_L = 15 pF

Figure 3. Test Circuit Waveforms, t_{PZH} and t_{PHZ}

PARAMETER MEASUREMENT INFORMATION



Generators: PRR = 1 MHz, 50% Duty Cycle,
t_r <6 ns, Z_O = 50 Ω

Figure 4. Test Circuit Waveforms, t_{PZL} and t_{PLZ}

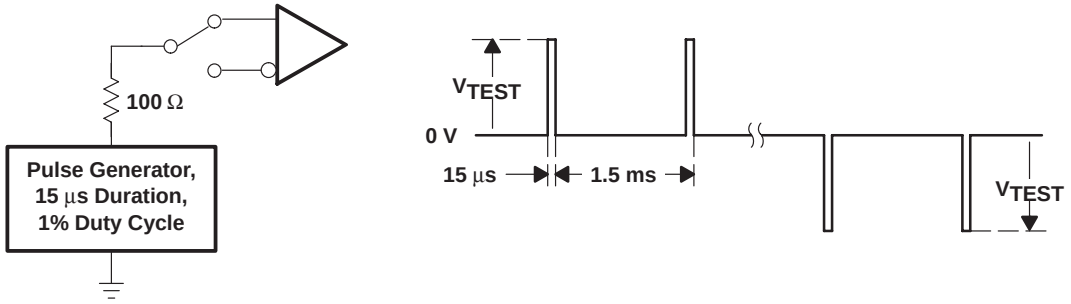


Figure 5. Test Circuit and Waveform, Transient Over-Voltage Test

TYPICAL CHARACTERISTICS

BUS INPUT CURRENT vs BUS INPUT VOLTAGE

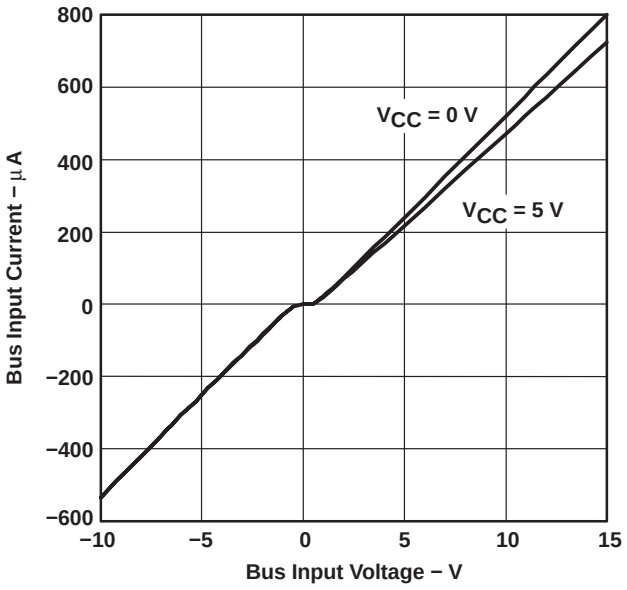


Figure 6

OUTPUT VOLTAGE vs DIFFERENTIAL INPUT VOLTAGE

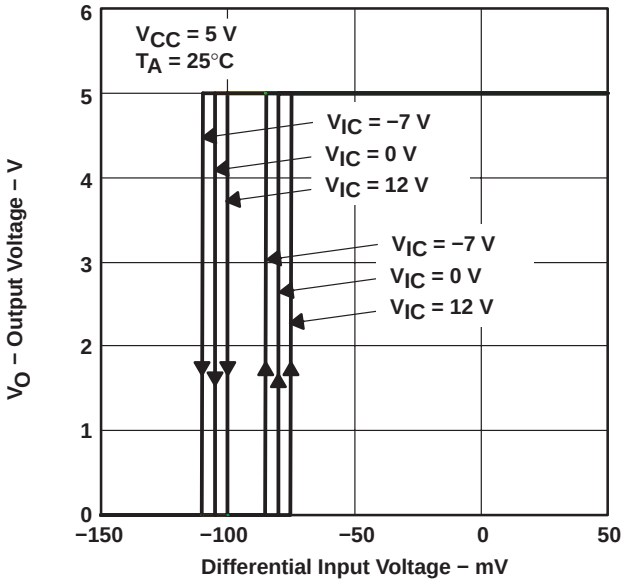


Figure 7

SUPPLY CURRENT vs SIGNALING RATE (ALL FOUR CHANNELS)

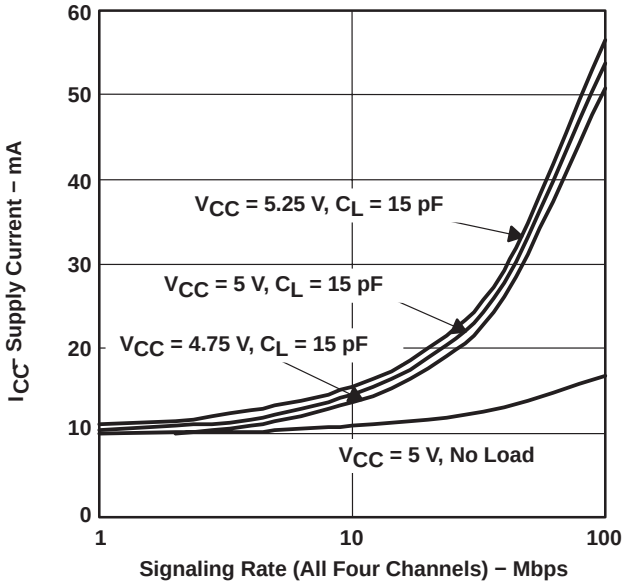


Figure 8

PROPAGATION DELAY TIME vs FREE-AIR TEMPERATURE

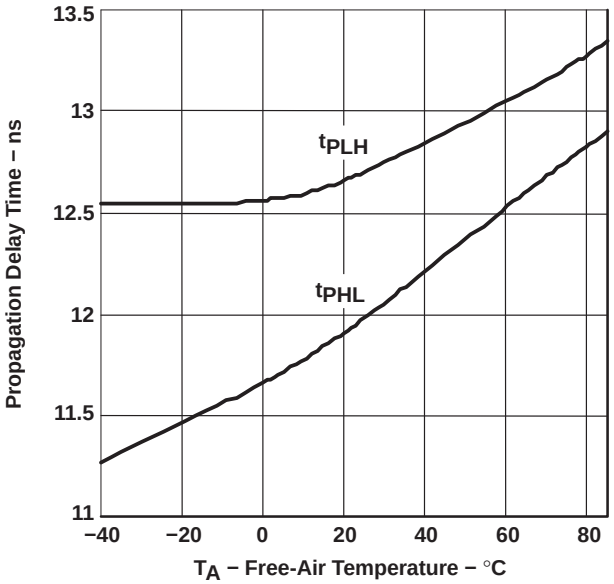


Figure 9

TYPICAL CHARACTERISTICS

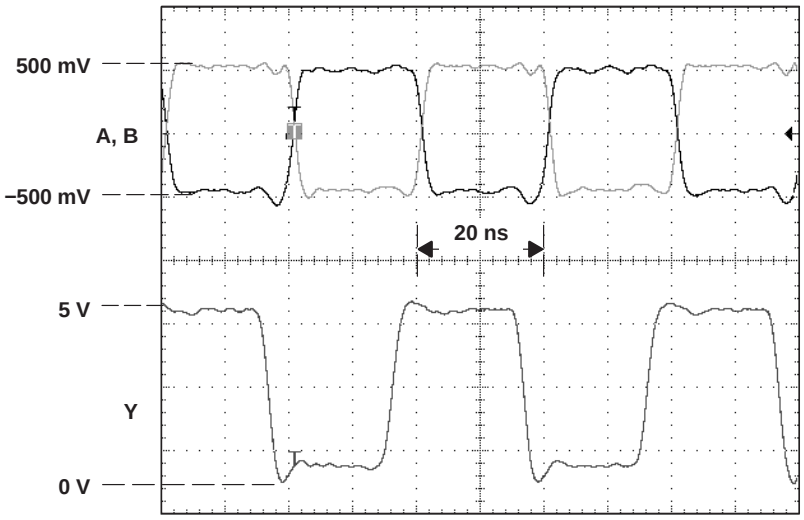


Figure 10. Receiver Inputs and Outputs, 50 Mbps Signaling Rate

APPLICATION INFORMATION

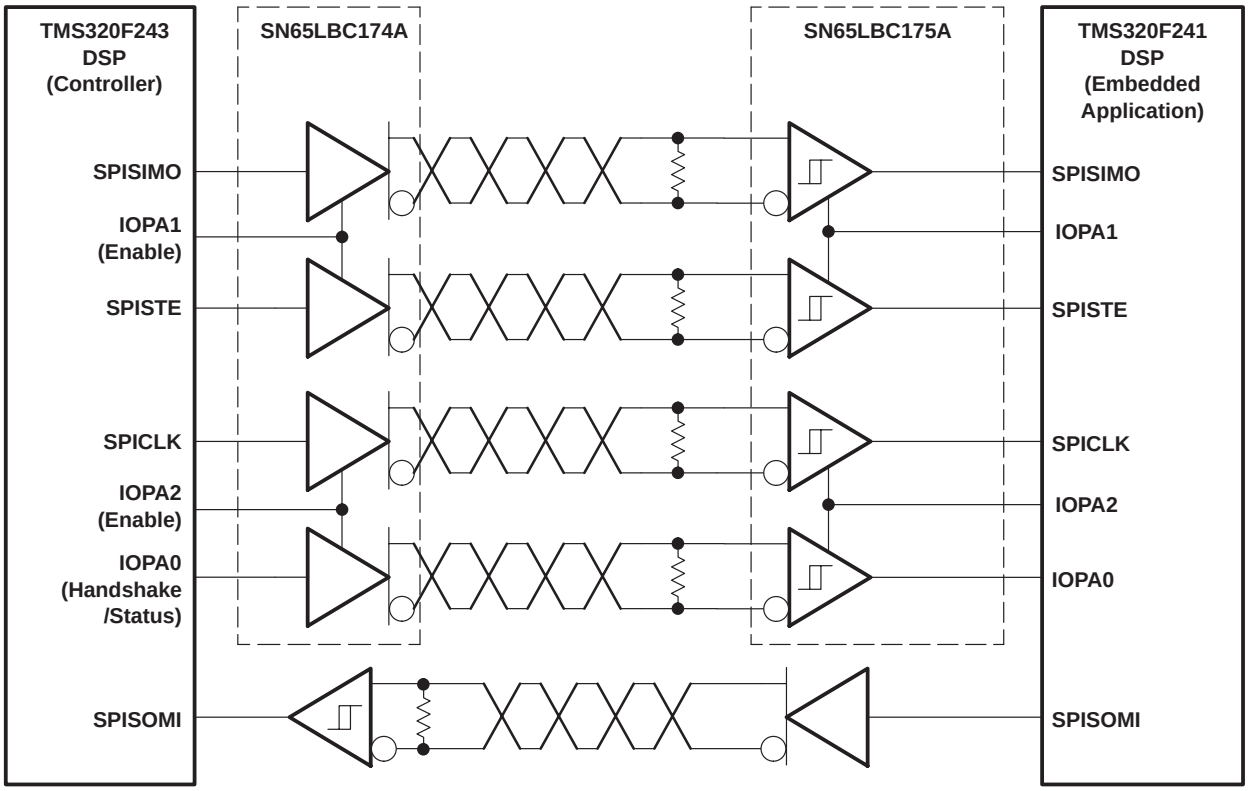


Figure 11. Typical Application Circuit, DSP-to-DSP Link via Serial Peripheral Interface

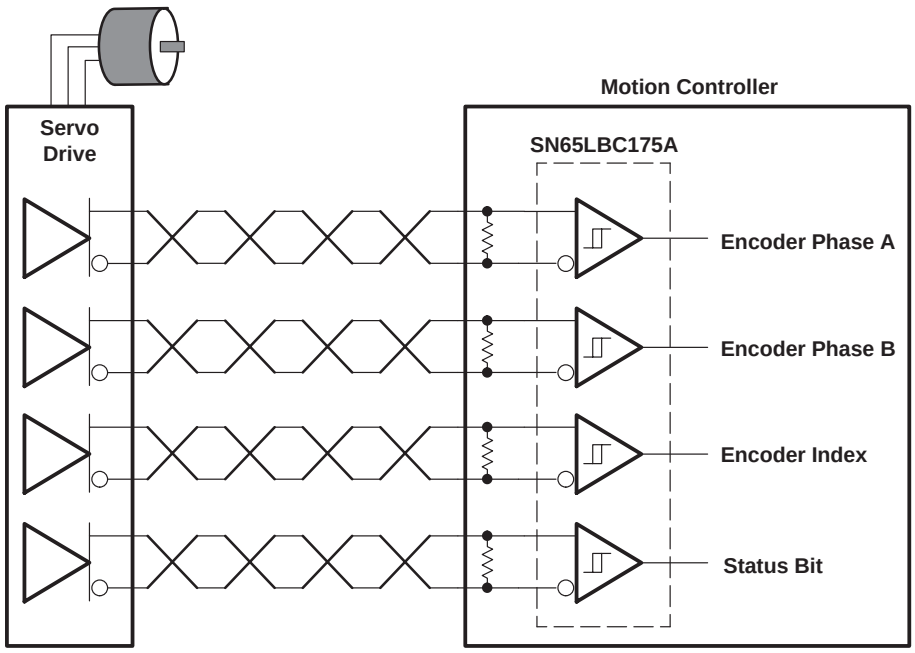


Figure 12. Typical Application Circuit, High-Speed Servomotor Encoder Interface

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
SN65LBC175AD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	65LBC175A	Samples
SN65LBC175ADG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	65LBC175A	Samples
SN65LBC175ADR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	65LBC175A	Samples
SN65LBC175ADRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	65LBC175A	Samples
SN65LBC175AN	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	65LBC175A	Samples
SN65LBC175ANE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	65LBC175A	Samples
SN75LBC175AD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	75LBC175A	Samples
SN75LBC175ADG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	75LBC175A	Samples
SN75LBC175ADR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	75LBC175A	Samples
SN75LBC175ADRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	75LBC175A	Samples
SN75LBC175AN	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	75LBC175A	Samples
SN75LBC175ANE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	75LBC175A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.

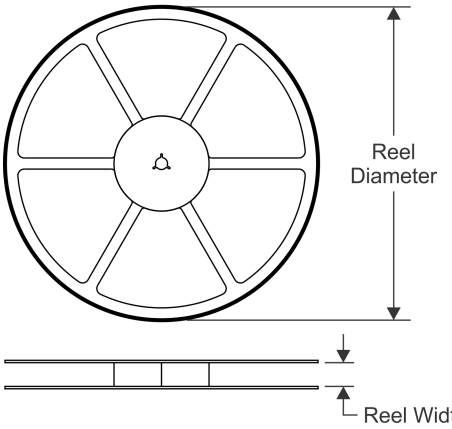
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

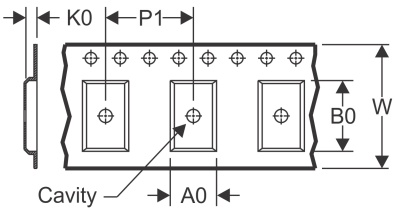
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

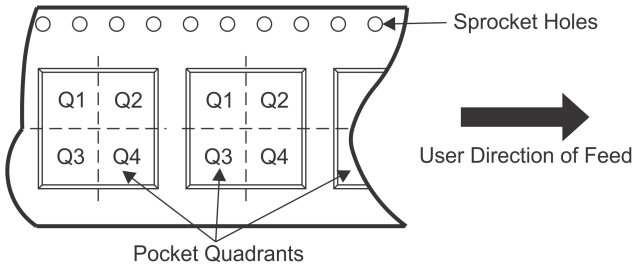


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

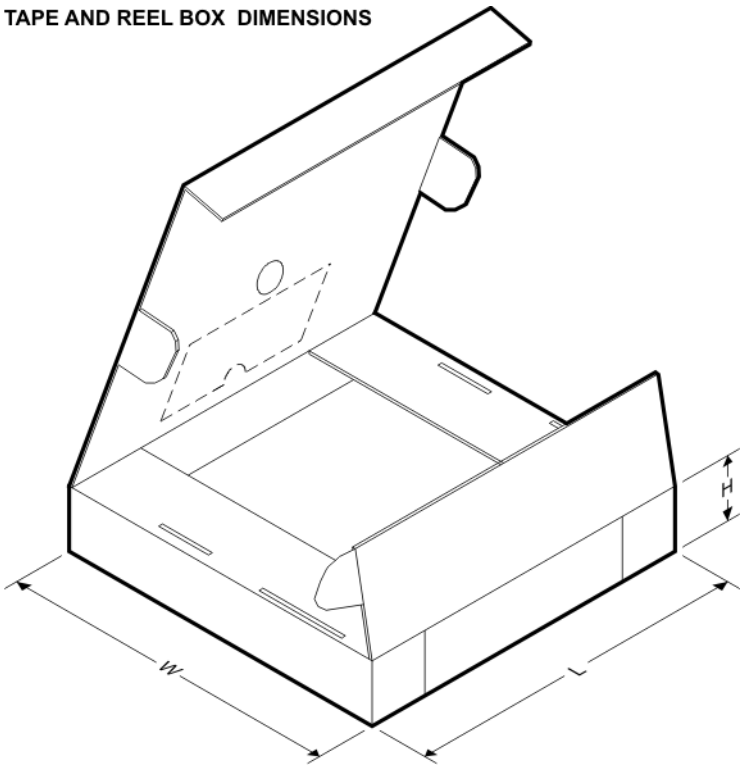
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LBC175ADR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN75LBC175ADR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

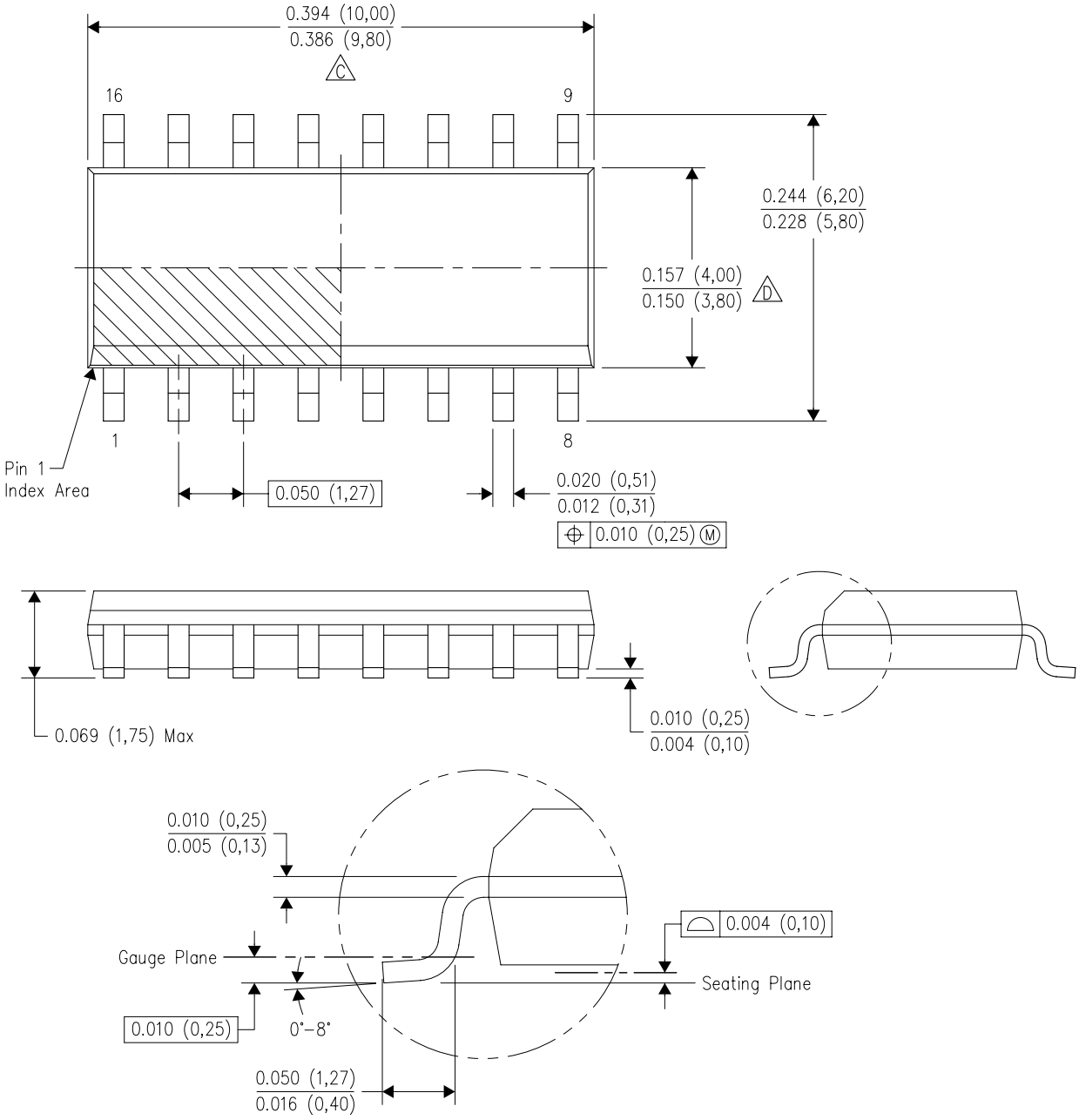
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

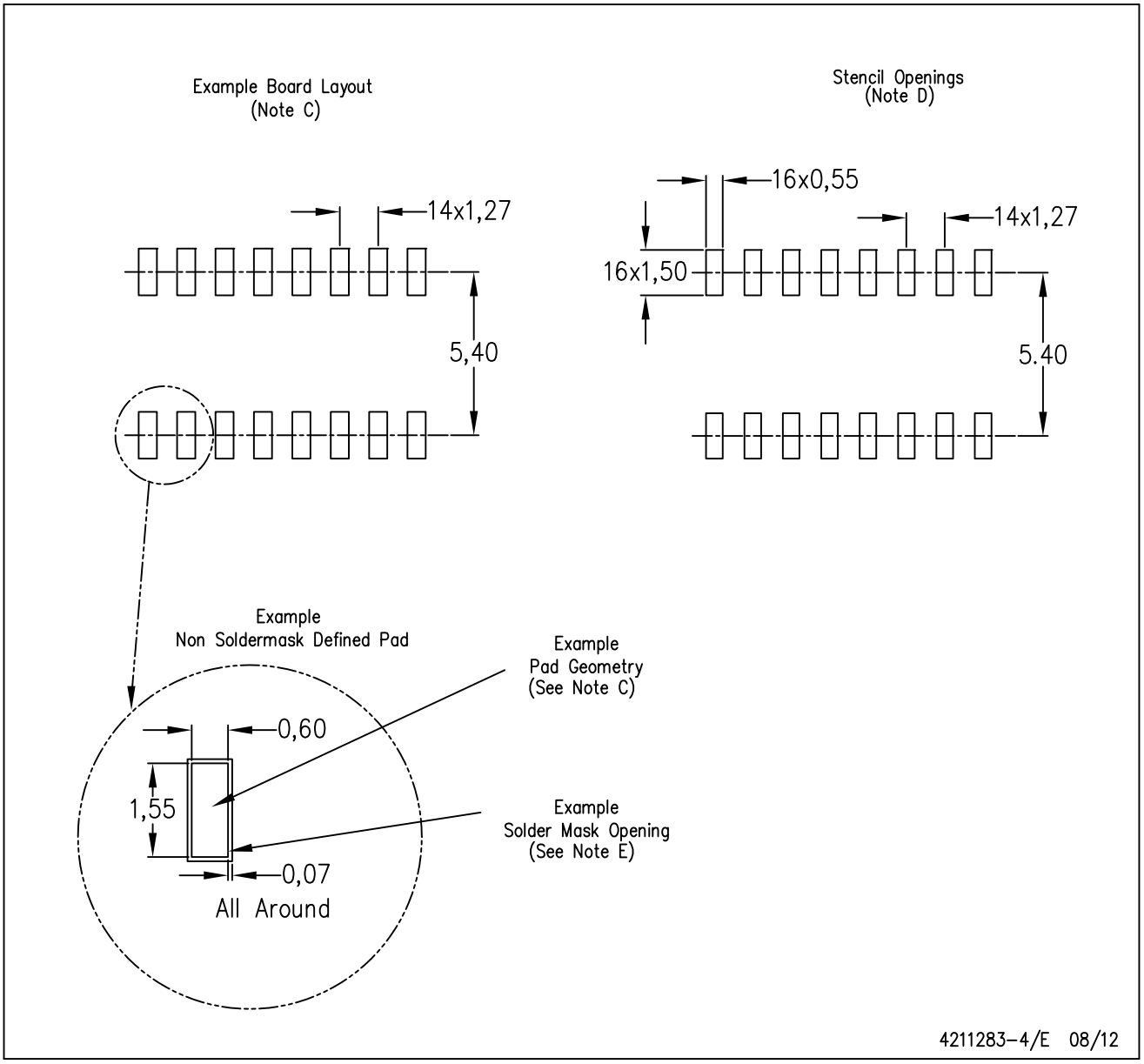
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65LBC175ADR	SOIC	D	16	2500	333.2	345.9	28.6
SN75LBC175ADR	SOIC	D	16	2500	333.2	345.9	28.6

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265