

SPECIFICATION

SPEC. No. C-High-a

D A T E : 2013 Sep.

To

Non-Controlled Copy

CUSTOMER'S PRODUCT NAME

TDK PRODUCT NAME

MULTILAYER CERAMIC CHIP CAPACITORS

C Series / Commercial Grade

High voltage (1000V and over)

Please return this specification to TDK representatives.

If orders are placed without returned specification, please allow us to judge that specification is accepted by your side.

RECEIPT CONFIRMATION

DATE: YEAR MONTH DAY

TDK Corporation
Sales
Electronic Components
Sales & Marketing Group

TDK-EPC Corporation
Engineering
Ceramic Capacitors Business Group

APPROVED	Person in charge

APPROVED	CHECKED	Person in charge

1. SCOPE

This specification is applicable to chip type multilayer ceramic capacitors with a priority over the other relevant specifications.

Production places defined in this specification shall be TDK-EPC Corporation Japan, TDK (Suzhou) Co., Ltd, and TDK Components U.S.A. Inc.

EXPLANATORY NOTE:

This specification warrants the quality of the ceramic chip capacitors. The chips should be evaluated or confirmed a state of mounted on your product.

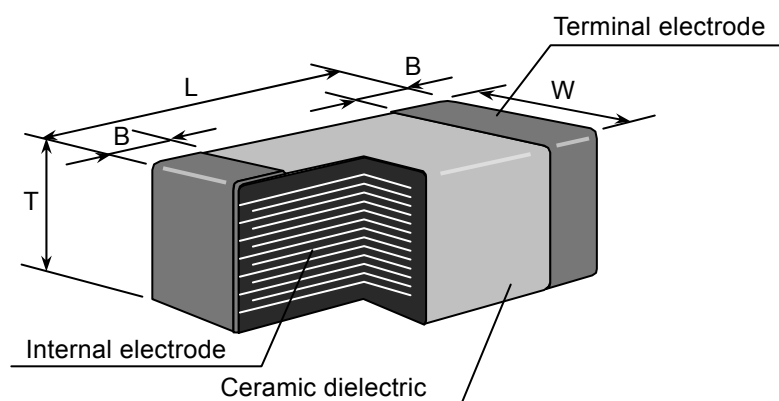
If the use of the chips goes beyond the bounds of the specification, we can not afford to guarantee.

2. CODE CONSTRUCTION

(Example)

Catalog Number :	<u>C4532</u>	<u>X7R</u>	<u>3D</u>	<u>222</u>	<u>M</u>	<u>130</u>	<u>K</u>	<u>A</u>
(Web)	(1)	(2)	(3)	(4)	(5)	(6)	(7)	(8)
Item Description :	<u>C4532</u>	<u>X7R</u>	<u>3D</u>	<u>222</u>	<u>M</u>	<u>T</u>	<u>xxx</u>	
	(1)	(2)	(3)	(4)	(5)	(9)	(10)	

(1) Type



Please refer to product list for the dimensions of each product.

(2) Temperature Characteristics (Details are shown in table 1 No.7 and No.8 at page 5)

(3) Rated Voltage

Symbol	Rated Voltage
3 A	DC 1 kV
3 D	DC 2 kV
3 F	DC 3 kV

(4) Rated Capacitance

Stated in three digits and in units of pico farads (pF).

The first and Second digits identify the first and second significant figures of the capacitance, the third digit identifies the multiplier.

R is designated for a decimal point.

Example 222 → 2,200pF

(5) Capacitance tolerance

Symbol	Tolerance	Capacitance
F	± 1 pF	10pF
K	± 10 %	Over 10pF
M	± 20 %	

(6) Thickness code (Only Catalog Number)

(7) Package code (Only Catalog Number)

(8) Special code (Only Catalog Number)

(9) Packaging

Symbol	Packaging
B	Bulk
T	Taping

(10) Internal code (Only Item Description)

3. RATED CAPACITANCE AND CAPACITANCE TOLERANCE

3.1 Standard combination of rated capacitance and tolerances

Class	Temperature Characteristics	Capacitance tolerance		Rated capacitance
1	C H C0G	10pF	F ($\pm 1\text{pF}$)	10
		Over 10pF	K ($\pm 10\%$)	E – 12 series
2	J B X7R X7S	K ($\pm 10\%$) M ($\pm 20\%$)		E – 3 series

3.2 Capacitance Step in E series

E series	Capacitance Step											
E- 3	1.0				2.2				4.7			
E- 12	1.0	1.2	1.5	1.8	2.2	2.7	3.3	3.9	4.7	5.6	6.8	8.2

4. OPERATING TEMPERATURE RANGE

T.C.	Min. operating Temperature	Max. operating Temperature	Reference Temperature
C H J B	-25°C	85°C	20°C
C0G X7R X7S	-55°C	125°C	25°C

5. STORING CONDITION AND TERM

5 to 40°C at 20 to 70%RH
6 months Max.

6. P.C. BOARD

When mounting on an aluminum substrate, large case sizes such as C4520 and C4532 types are more likely to be affected by heat stress from the substrate. Please inquire separate specification for the large case sizes when mounted on the substrate.

7. INDUSTRIAL WASTE DISPOSAL

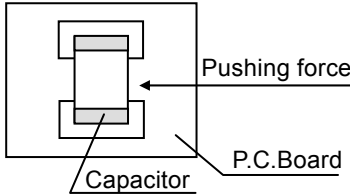
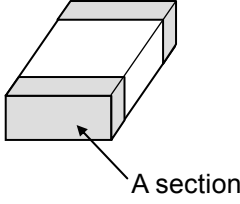
Dispose this product as industrial waste in accordance with the Industrial Waste Law.

8. PERFORMANCE

table 1

No.	Item	Performance	Test or inspection method									
1	External Appearance	No defects which may affect performance.	Inspect with magnifying glass (3×)									
2	Insulation Resistance	10,000MΩ min.	Apply 500V DC for 60s.									
3	Voltage Proof	Withstand test voltage without insulation breakdown or other damage.	1.2 times of rated voltage, above DC voltage shall be applied for 1 to 5s. Charge / discharge current shall not exceed 50mA.									
4	Capacitance	Within the specified tolerance.	<table border="1"> <thead> <tr> <th>Class</th> <th>Measuring frequency</th> <th>Measuring voltage</th> </tr> </thead> <tbody> <tr> <td>Class1</td> <td>1MHz±10%</td> <td>0.5 - 5 Vrms.</td> </tr> <tr> <td>Class2</td> <td>1kHz±10%</td> <td>1.0±0.2 Vrms.</td> </tr> </tbody> </table>	Class	Measuring frequency	Measuring voltage	Class1	1MHz±10%	0.5 - 5 Vrms.	Class2	1kHz±10%	1.0±0.2 Vrms.
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Class1	1MHz±10%	0.5 - 5 Vrms.										
Class2	1kHz±10%	1.0±0.2 Vrms.										
5	Q (Class1)	<table border="1"> <thead> <tr> <th>Rated Capacitance</th> <th>Q</th> </tr> </thead> <tbody> <tr> <td>30pF and over</td> <td>1,000 min.</td> </tr> <tr> <td>Under 30pF</td> <td>400+20×C min.</td> </tr> </tbody> </table> <p>C : Rated capacitance (pF)</p>	Rated Capacitance	Q	30pF and over	1,000 min.	Under 30pF	400+20×C min.	See No.4 in this table for measuring condition.			
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30pF and over	1,000 min.											
Under 30pF	400+20×C min.											
6	Dissipation Factor (Class2)	<table border="1"> <thead> <tr> <th>T.C.</th> <th>D.F.</th> </tr> </thead> <tbody> <tr> <td>J B X7R X7S</td> <td>0.03 max.</td> </tr> </tbody> </table>	T.C.	D.F.	J B X7R X7S	0.03 max.	See No.4 in this table for measuring condition.					
T.C.	D.F.											
J B X7R X7S	0.03 max.											

(continued)

No.	Item	Performance	Test or inspection method										
7	Temperature Characteristics of Capacitance (Class1)	<table border="1" data-bbox="512 259 906 465"> <tr> <td>T.C.</td> <td>Temperature Coefficient</td> </tr> <tr> <td>C H</td> <td>0 ± 60 (ppm/°C)</td> </tr> <tr> <td>C0G</td> <td>0 ± 30 (ppm/°C)</td> </tr> </table> <p data-bbox="499 501 911 566">Capacitance drift within ± 0.2% or ± 0.05pF, whichever larger.</p>	T.C.	Temperature Coefficient	C H	0 ± 60 (ppm/°C)	C0G	0 ± 30 (ppm/°C)	<p data-bbox="948 237 1382 338">Temperature coefficient shall be calculated based on values at 25°C (CH : 20°C) and 85°C temperature.</p> <p data-bbox="948 374 1445 439">Measuring temperature below 20°C shall be -10°C and -25°C.</p>				
T.C.	Temperature Coefficient												
C H	0 ± 60 (ppm/°C)												
C0G	0 ± 30 (ppm/°C)												
8	Temperature Characteristics of Capacitance (Class2)	<p data-bbox="557 620 863 654">Capacitance Change (%)</p> <hr/> <p data-bbox="595 685 825 719">No voltage applied</p> <hr/> <p data-bbox="624 792 777 882">J B : ± 10 X7R : ± 15 X7S : ± 22</p> <hr/>	<p data-bbox="948 607 1431 741">Capacitance shall be measured by the steps shown in the following table after thermal equilibrium is obtained for each step.</p> <p data-bbox="948 745 1398 779">ΔC be calculated ref. STEP3 reading</p> <table border="1" data-bbox="963 779 1437 1070"> <thead> <tr> <th>Step</th> <th>Temperature(°C)</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>Reference Temp. ± 2</td> </tr> <tr> <td>2</td> <td>Min. operating Temp. ± 3</td> </tr> <tr> <td>3</td> <td>Reference Temp. ± 2</td> </tr> <tr> <td>4</td> <td>Max. operating Temp. ± 2</td> </tr> </tbody> </table>	Step	Temperature(°C)	1	Reference Temp. ± 2	2	Min. operating Temp. ± 3	3	Reference Temp. ± 2	4	Max. operating Temp. ± 2
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1	Reference Temp. ± 2												
2	Min. operating Temp. ± 3												
3	Reference Temp. ± 2												
4	Max. operating Temp. ± 2												
9	Robustness of Terminations	<p data-bbox="499 1120 911 1216">No sign of termination coming off, breakage of ceramic, or other abnormal signs.</p>	<p data-bbox="948 1120 1431 1216">Reflow solder the capacitors on a P.C.Board shown in Appendix 1 and apply a pushing force of 5N with 10±1s.</p> 										
10	Solderability	<p data-bbox="499 1496 911 1561">New solder to cover over 75% of termination.</p> <p data-bbox="499 1565 911 1662">25% may have pin holes or rough spots but not concentrated in one spot.</p> <p data-bbox="499 1666 911 1800">Ceramic surface of A sections shall not be exposed due to melting or shifting of termination material.</p> 	<p data-bbox="948 1496 1398 1561">Completely soak both terminations in solder at 235±5°C for 2±0.5s.</p> <p data-bbox="948 1597 1278 1630">Solder : H63A (JIS Z 3282)</p> <p data-bbox="948 1666 1390 1762">Flux : Isopropyl alcohol (JIS K 8839) Rosin(JIS K 5902) 25% solid solution.</p>										

(continued)

No.	Item		Performance	Test or inspection method		
11	Resistance to solder heat	External appearance	No cracks are allowed and terminations shall be covered at least 60% with new solder.	<p>Completely soak both terminations in solder at 260 ± 5°C for 5± 1s.</p> <p>Preheating condition Temp. : 150 ± 10°C Time : 1 ~ 2min.</p> <p>Flux: Isopropyl alcohol (JIS K 8839) Rosin (JIS K 5902) 25% solid solution.</p> <p>Solder: H63A (JIS Z 3282)</p> <p>Leave the capacitors in ambient condition for 6 to 24h (Class 1) or 24±2h (Class 2) before measurement.</p>		
		Capacitance	Characteristics		Change from the value before test	
			Class 1		C H C0G	Capacitance drift within ± 2.5% or ±0.25pF, whichever larger.
			Class 2		J B X7R X7S	± 7.5 %
		Q Class1	Rated Capacitance		Q	
			30pF and over		1,000 min.	
			Under 30pF		400+20×C min.	
C : Rated capacitance (pF)						
D.F. Class2	Meet the initial spec.					
Insulation Resistance	Meet the initial spec.					
Voltage proof	No insulation breakdown or other damage.					
12	Vibration	External appearance	No mechanical damage.	<p>Reflow solder the capacitors on a P.C.Board shown in Appendix1 before testing.</p> <p>Vibrate the capacitors with amplitude of 1.5mm P-P changing the frequencies from 10Hz to 55Hz and back to 10Hz in about 1min.</p> <p>Repeat this for 2h each in 3 perpendicular directions.</p>		
		Capacitance	Characteristics		Change from the value before test	
			Class 1		C H C0G	Capacitance drift within ± 2.5% or ±0.25pF, whichever larger.
			Class 2		J B X7R X7S	± 7.5 %
Q (Class1)	Rated Capacitance		Q			
	30pF and over		1,000 min.			
	Under 30pF		400+20×C min.			
C : Rated capacitance (pF)						
D.F. Class2	Meet the initial spec.					

(continued)

No.	Item	Performance	Test or inspection method															
13	Temperature cycle	External appearance	<p>Reflow solder the capacitors on a P.C.Board shown in Appendix 1 before testing.</p> <p>Expose the capacitors in the condition step1 through step 4 and repeat 5 times consecutively.</p> <p>Leave the capacitors in ambient condition for 6 to 24h (Class 1) or 24±2h (Class 2) before measurement.</p> <table border="1"> <thead> <tr> <th>Step</th> <th>Temperature(°C)</th> <th>Time(min.)</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>Min. operating Temp. ± 3</td> <td>30 ± 3</td> </tr> <tr> <td>2</td> <td>Reference Temp. ± 2</td> <td>2 - 5</td> </tr> <tr> <td>3</td> <td>Max. operating Temp. ± 2</td> <td>30 ± 2</td> </tr> <tr> <td>4</td> <td>Reference Temp. ± 2</td> <td>2 - 5</td> </tr> </tbody> </table>	Step	Temperature(°C)	Time(min.)	1	Min. operating Temp. ± 3	30 ± 3	2	Reference Temp. ± 2	2 - 5	3	Max. operating Temp. ± 2	30 ± 2	4	Reference Temp. ± 2	2 - 5
		Step		Temperature(°C)	Time(min.)													
		1		Min. operating Temp. ± 3	30 ± 3													
		2		Reference Temp. ± 2	2 - 5													
		3		Max. operating Temp. ± 2	30 ± 2													
		4		Reference Temp. ± 2	2 - 5													
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Under 30pF	400+20×C min.																	
D.F. (Class2)	Meet the initial spec.																	
Insulation Resistance	Meet the initial spec.																	
Voltage proof	No insulation breakdown or other damage.																	
14	Moisture Resistance (Steady State)	External appearance	<p>Reflow solder the capacitors on a P.C.Board shown in Appendix1 before testing.</p> <p>Leave at temperature 40±2°C, 90 to 95%RH for 500 +24,0h.</p> <p>Leave the capacitors in ambient condition for 6 to 24h (Class1) or 24±2h (Class2) before measurement.</p>															
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		Class 2		J B X7R X7S	± 12.5 %													
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Rated Capacitance	Q																	
30pF and over	350 min.																	
10pF and over to under 30pF	275+5/2×C min.																	
D.F. (Class2)	200% of initial spec. max.																	
Insulation Resistance	1,000MΩ min.																	

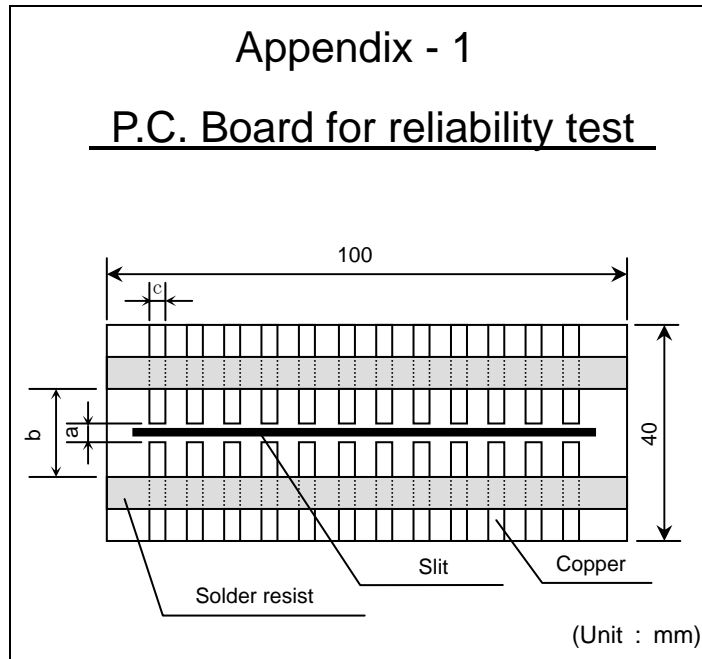
(continued)

No.	Item		Performance	Test or inspection method									
15	Life	External appearance	No mechanical damage.	<p>Reflow solder the capacitors on a P.C.Board shown in Appendix 1 before testing.</p> <p>Apply rated voltage at maximum operating temperature $\pm 2^{\circ}\text{C}$ for 1,000 +48, 0h.</p> <p>Charge/discharge current shall not exceed 50mA.</p> <p>Leave the capacitors in ambient condition for 6 to 24h (Class1) or 24\pm2h (Class2) before measurement.</p> <p>Voltage conditioning (only for class 2) Voltage treat the capacitors under testing temperature and voltage for 1 hour.</p> <p>Leave the capacitors in ambient condition for 24\pm2h before measurement. Use this measurement for initial value.</p>									
		Capacitance	<table border="1"> <thead> <tr> <th colspan="2">Characteristics</th> <th>Change from the value before test</th> </tr> </thead> <tbody> <tr> <td>Class 1</td> <td>C H C0G</td> <td>Capacitance drift within $\pm 3\%$ or $\pm 0.3\text{pF}$, whichever larger.</td> </tr> <tr> <td>Class 2</td> <td>J B X7R X7S</td> <td>$\pm 15\%$</td> </tr> </tbody> </table>		Characteristics		Change from the value before test	Class 1	C H C0G	Capacitance drift within $\pm 3\%$ or $\pm 0.3\text{pF}$, whichever larger.	Class 2	J B X7R X7S	$\pm 15\%$
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10pF and over to under 30pF	275+5/2 \times C min.												
D.F. (Class2)	200% of initial spec. max.												
Insulation Resistance	1,000M Ω min.												

*As for the initial measurement of capacitors (Class2) on number 8,11,12, 13 and 14, leave capacitors at 150 -10,0 $^{\circ}\text{C}$ for 1 hour and measure the value after leaving capacitors for 24 \pm 2h in ambient condition.



Appendix - 1

P.C. Board for reliability test



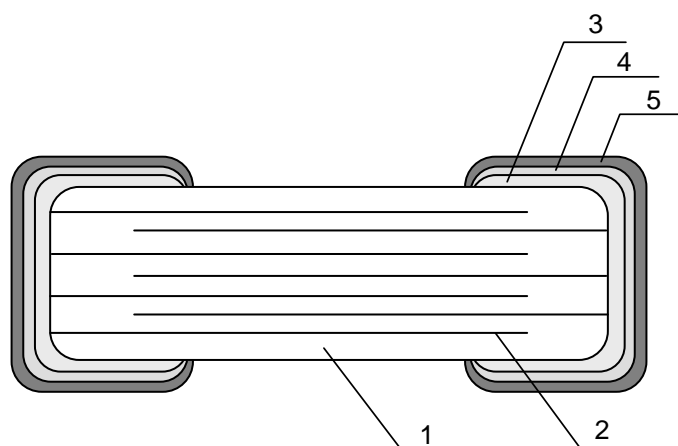
Material : Glass Epoxy (As per JIS C6484 GE4)

P.C. Board thickness : 1.6mm

-  Copper (thickness 0.035mm)
-  Solder resist

TDK (EIA style)	Dimensions (mm)		
	a	b	c
C3216 (CC1206)	2.2	5.0	2.0
C3225 (CC1210)	2.2	5.0	2.9
C4520 (CC1808)	3.5	7.0	2.5
C4532 (CC1812)	3.5	7.0	3.7
C5750 (CC2220)	4.5	8.0	5.6

9. INSIDE STRUCTURE AND MATERIAL



No.	NAME	MATERIAL	
		Class1	Class2
1	Dielectric	CaZrO ₃	BaTiO ₃
2	Electrode	Nickel (Ni)	
3	Termination	Copper (Cu)	
4		Nickel (Ni)	
5		Tin (Sn)	

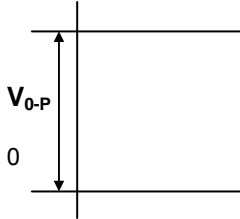
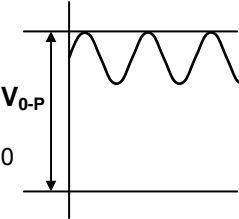
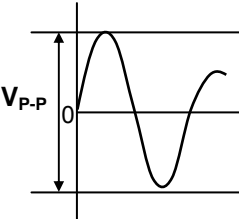
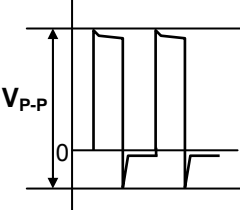
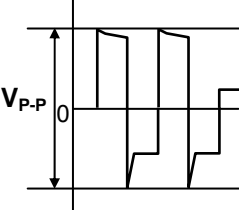
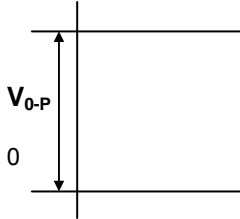
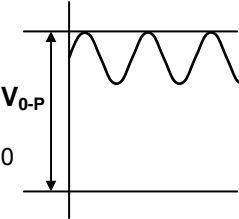
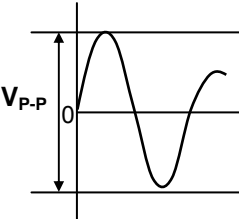
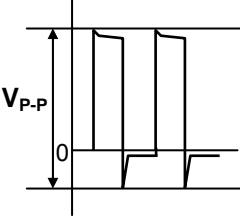
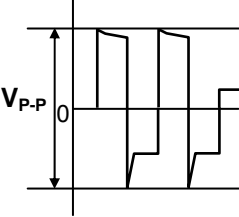
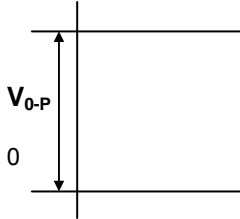
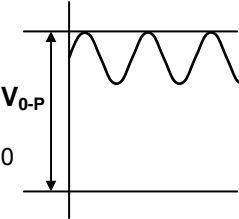
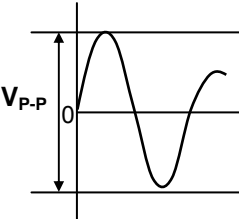
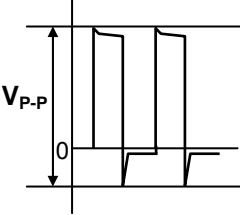
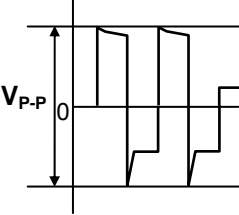
10. RECOMMENDATION

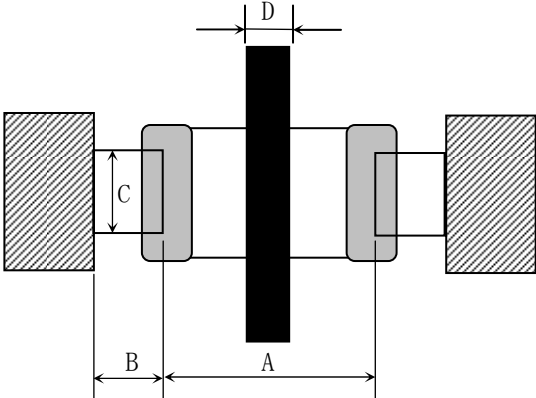
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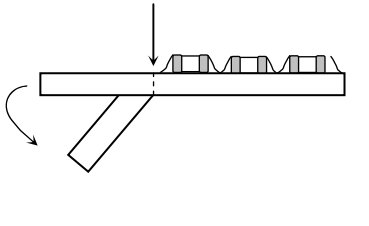
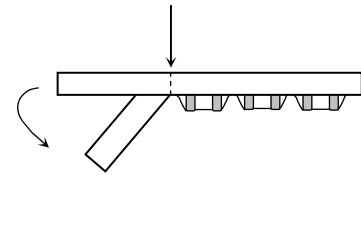
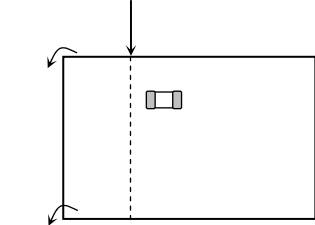
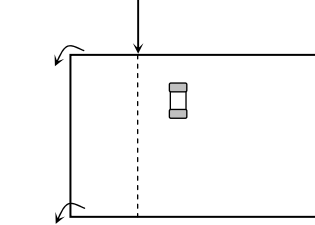
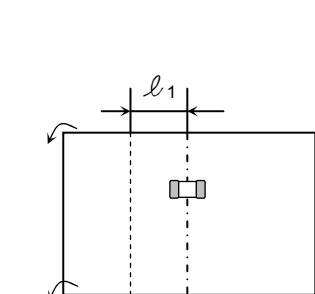
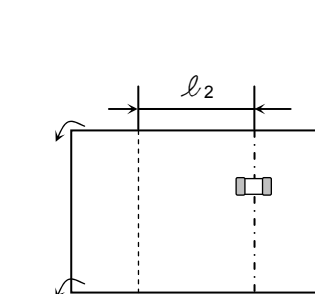
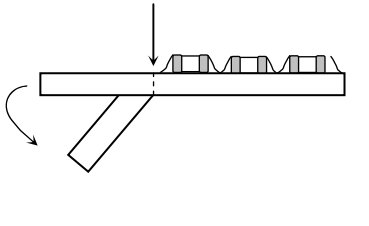
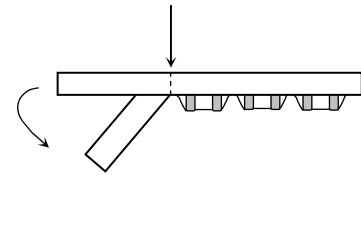
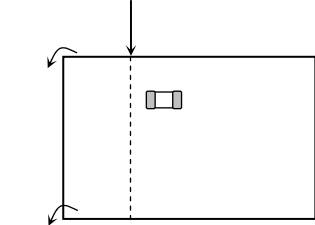
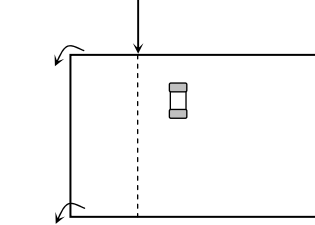
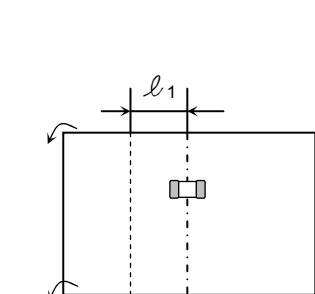
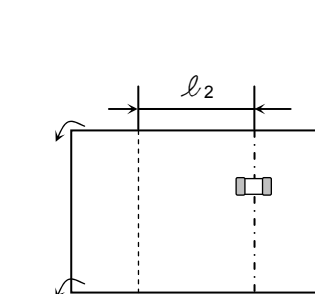
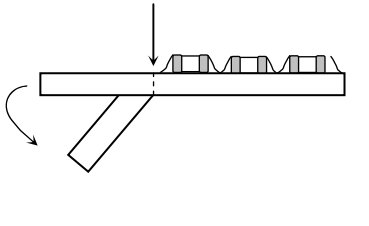
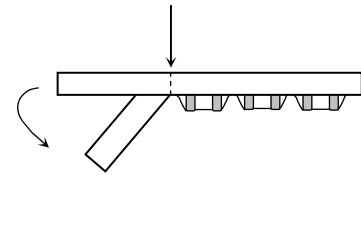
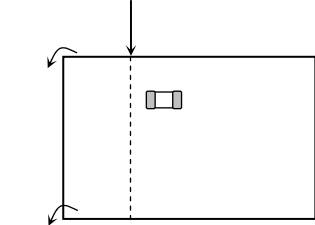
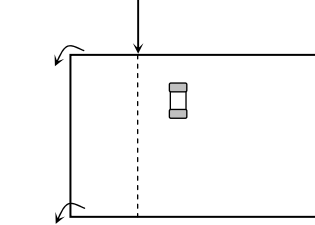
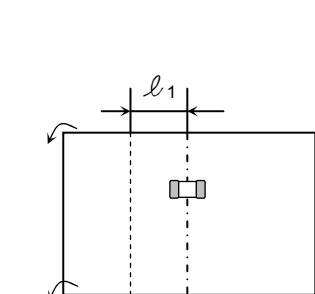
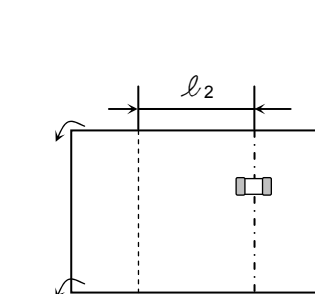
11. SOLDERING CONDITION

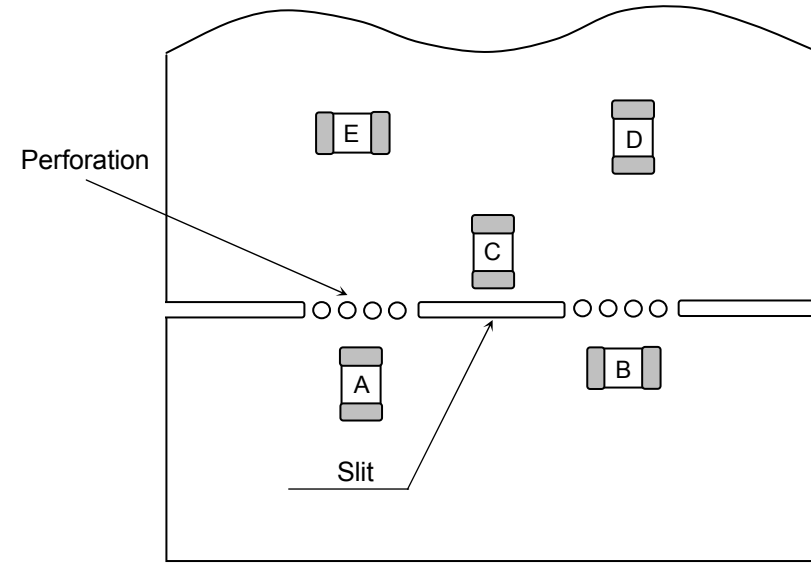
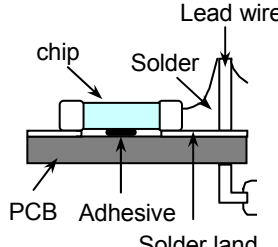
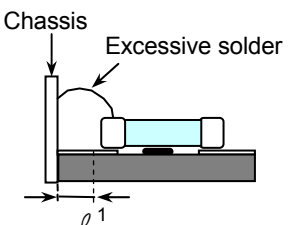
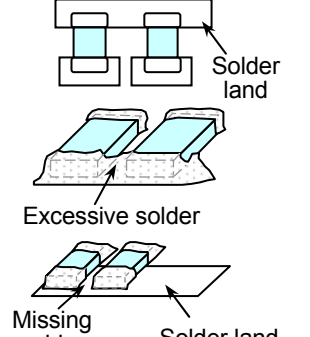
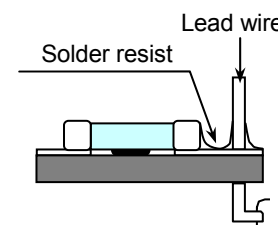
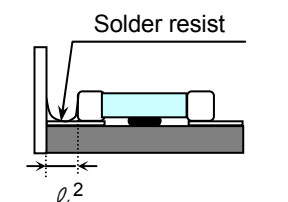
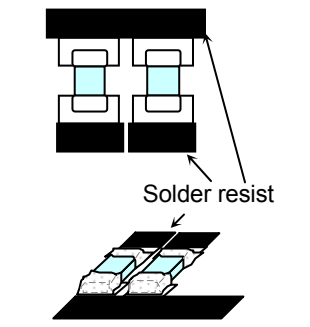
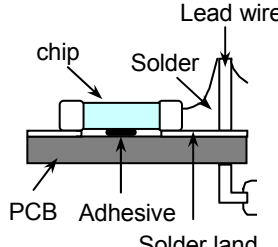
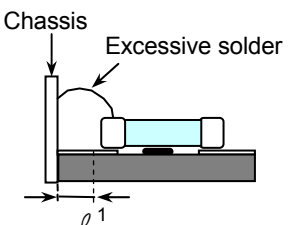
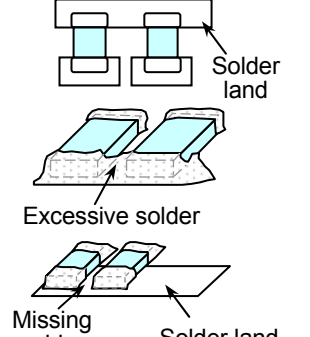
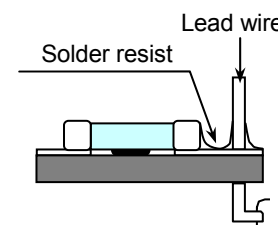
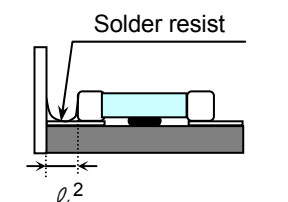
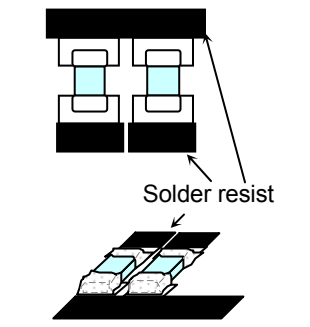
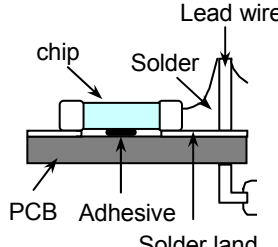
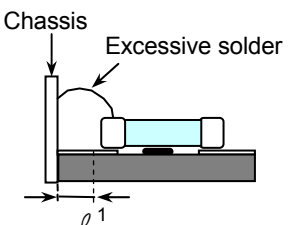
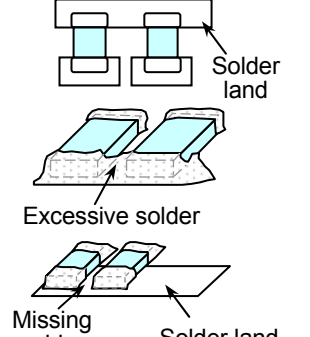
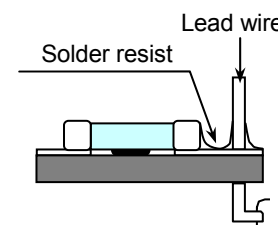
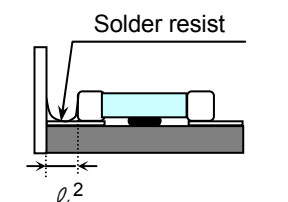
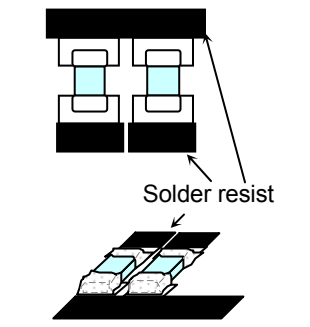
Reflow soldering only.

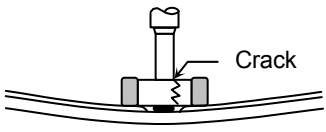
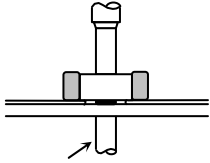
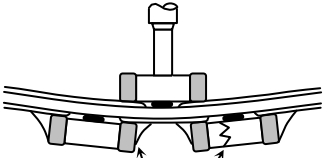
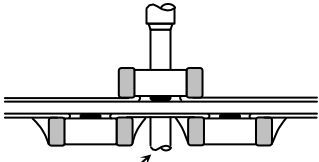
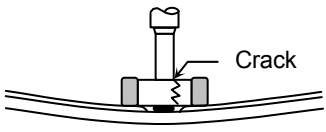
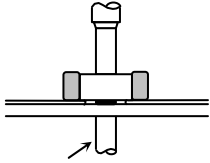
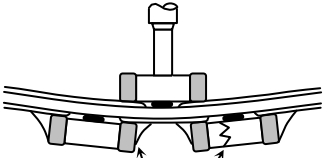
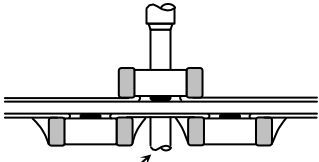
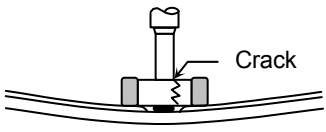
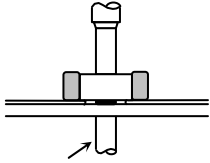
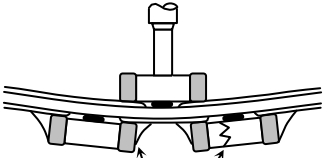
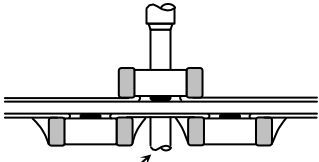
12. Caution

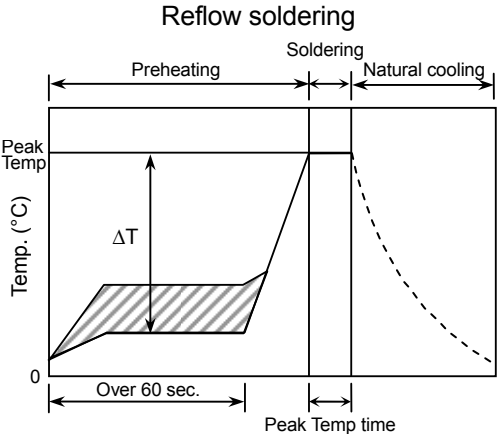
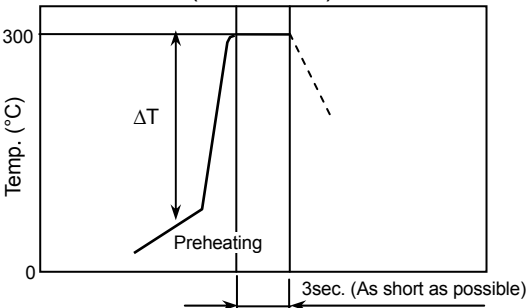
No.	Process	Condition														
1	Operating Condition (Storage, Transportation)	<p>1-1. Storage</p> <ol style="list-style-type: none"> 1) The capacitors must be stored in an ambient temperature of 5 to 40°C with a relative humidity of 20 to 70%RH. The products should be used within 6 months upon receipt. 2) The capacitors must be operated and stored in an environment free of dew condensation and these gases such as Hydrogen Sulphide, Hydrogen Sulphate, Chlorine, Ammonia and sulfur. 3) Avoid storing in sun light and falling of dew. 4) Do not use capacitors under high humidity and high and low atmospheric pressure which may affect capacitors reliability. 5) Capacitors should be tested for the solderability when they are stored for long time. <p>1-2. Handling in transportation</p> <p>In case of the transportation of the capacitors, the performance of the capacitors may be deteriorated depending on the transportation condition. (Refer to JEITA RCR-2335B 9.2 Handling in transportation)</p>														
2	Circuit design ⚠ Caution	<p>2-1. Operating temperature</p> <p>Operating temperature should be followed strictly within this specification, especially be careful with maximum temperature.</p> <ol style="list-style-type: none"> 1) Do not use capacitors above the maximum allowable operating temperature. 2) Surface temperature including self heating should be below maximum operating temperature. (Due to dielectric loss, capacitors will heat itself when AC is applied. Especially at high frequencies around its SRF, the heat might be so extreme that it may damage itself or the product mounted on. Please design the circuit so that the maximum temperature of the capacitors including the self heating to be below the maximum allowable operating temperature. Temperature rise at capacitor surface shall be below 20°C) 3) The electrical characteristics of the capacitors will vary depending on the temperature. The capacitors should be selected and designed in taking the temperature into consideration. <p>2-2. Operating voltage</p> <ol style="list-style-type: none"> 1) Operating voltage across the terminals should be below the rated voltage. When AC and DC are super imposed, V_{0-P} must be below the rated voltage. _____ (1) and (2) AC or pulse with overshooting, V_{P-P} must be below the rated voltage. _____ (3), (4) and (5) When the voltage is started to apply to the circuit or it is stopped applying, the irregular voltage may be generated for a transit period because of resonance or switching. Be sure to use the capacitors within rated voltage containing these Irregular voltage. <table border="1" data-bbox="472 1451 1445 1727"> <thead> <tr> <th data-bbox="472 1451 660 1496">Voltage</th> <th data-bbox="660 1451 922 1496">(1) DC voltage</th> <th data-bbox="922 1451 1184 1496">(2) DC+AC voltage</th> <th data-bbox="1184 1451 1445 1496">(3) AC voltage</th> </tr> </thead> <tbody> <tr> <td data-bbox="472 1496 660 1727">Positional Measurement (Rated voltage)</td> <td data-bbox="660 1496 922 1727">  </td> <td data-bbox="922 1496 1184 1727">  </td> <td data-bbox="1184 1496 1445 1727">  </td> </tr> </tbody> </table> <table border="1" data-bbox="472 1753 1184 2020"> <thead> <tr> <th data-bbox="472 1753 660 1798">Voltage</th> <th data-bbox="660 1753 922 1798">(4) Pulse voltage (A)</th> <th data-bbox="922 1753 1184 1798">(5) Pulse voltage (B)</th> </tr> </thead> <tbody> <tr> <td data-bbox="472 1798 660 2020">Positional Measurement (Rated voltage)</td> <td data-bbox="660 1798 922 2020">  </td> <td data-bbox="922 1798 1184 2020">  </td> </tr> </tbody> </table>	Voltage	(1) DC voltage	(2) DC+AC voltage	(3) AC voltage	Positional Measurement (Rated voltage)				Voltage	(4) Pulse voltage (A)	(5) Pulse voltage (B)	Positional Measurement (Rated voltage)		
Voltage	(1) DC voltage	(2) DC+AC voltage	(3) AC voltage													
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Voltage	(4) Pulse voltage (A)	(5) Pulse voltage (B)														
Positional Measurement (Rated voltage)																

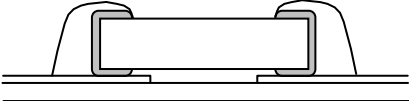
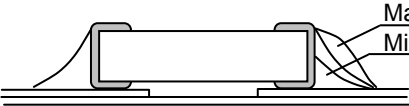
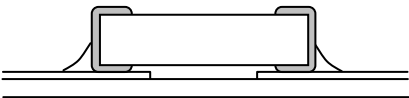
No.	Process	Condition																																			
2	Circuit design ⚠ Caution	<p>2) Even below the rated voltage, if repetitive high frequency AC or pulse is applied, the reliability of the capacitors may be reduced.</p> <p>3) The effective capacitance will vary depending on applied DC and AC voltages. The capacitors should be selected and designed in taking the voltages into consideration.</p> <p>2-3. Frequency When the capacitors (Class 2) are used in AC and/or pulse voltages, the capacitors may vibrate themselves and generate audible sound.</p>																																			
3	Designing P.C.board	<p>The amount of solder at the terminations has a direct effect on the reliability of the capacitors.</p> <p>1) The greater the amount of solder, the higher the stress on the chip capacitors, and the more likely that it will break. When designing a P.C.board, determine the shape and size of the solder lands to have proper amount of solder on the terminations.</p> <p>2) Avoid using common solder land for multiple terminations and provide individual solder land for each terminations.</p> <p>3) Size and recommended land dimensions.</p> <div style="text-align: center;">  <p style="text-align: right;">(mm)</p> </div> <table border="1" data-bbox="497 1283 1147 1518"> <thead> <tr> <th>Type</th> <th>C3216</th> <th>C3225</th> </tr> </thead> <tbody> <tr> <td>A</td> <td>2.0 – 2.4</td> <td>2.0 – 2.4</td> </tr> <tr> <td>B</td> <td>1.0 – 1.2</td> <td>1.0 – 1.2</td> </tr> <tr> <td>C</td> <td>1.1 – 1.6</td> <td>1.9 – 2.5</td> </tr> <tr> <td>D</td> <td>1.0 – 1.3</td> <td>1.0 – 1.3</td> </tr> </tbody> </table> <table border="1" data-bbox="497 1556 1382 1792"> <thead> <tr> <th>Type</th> <th>C4520</th> <th>C4532</th> <th>C5750</th> </tr> </thead> <tbody> <tr> <td>A</td> <td>3.1 - 3.7</td> <td>3.1 - 3.7</td> <td>4.1 – 4.8</td> </tr> <tr> <td>B</td> <td>1.2 - 1.4</td> <td>1.2 - 1.4</td> <td>1.2 – 1.4</td> </tr> <tr> <td>C</td> <td>1.5 - 2.0</td> <td>2.4 - 3.2</td> <td>4.0 – 5.0</td> </tr> <tr> <td>D</td> <td>1.0 - 1.3</td> <td>1.0 - 1.3</td> <td>1.0 – 1.3</td> </tr> </tbody> </table> <p>4) It is recommended to provide a slit (about 1mm width) in the board under the components to improve washing flux. And please make sure to dry detergent up completely before. It is recommended to use low activated flux (Chlorine content : less than 0.1wt%) such Rosin due to high voltage usage.</p>	Type	C3216	C3225	A	2.0 – 2.4	2.0 – 2.4	B	1.0 – 1.2	1.0 – 1.2	C	1.1 – 1.6	1.9 – 2.5	D	1.0 – 1.3	1.0 – 1.3	Type	C4520	C4532	C5750	A	3.1 - 3.7	3.1 - 3.7	4.1 – 4.8	B	1.2 - 1.4	1.2 - 1.4	1.2 – 1.4	C	1.5 - 2.0	2.4 - 3.2	4.0 – 5.0	D	1.0 - 1.3	1.0 - 1.3	1.0 – 1.3
Type	C3216	C3225																																			
A	2.0 – 2.4	2.0 – 2.4																																			
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C	1.1 – 1.6	1.9 – 2.5																																			
D	1.0 – 1.3	1.0 – 1.3																																			
Type	C4520	C4532	C5750																																		
A	3.1 - 3.7	3.1 - 3.7	4.1 – 4.8																																		
B	1.2 - 1.4	1.2 - 1.4	1.2 – 1.4																																		
C	1.5 - 2.0	2.4 - 3.2	4.0 – 5.0																																		
D	1.0 - 1.3	1.0 - 1.3	1.0 – 1.3																																		

No.	Process	Condition												
3	Designing P.C.board	<p data-bbox="437 147 1098 181">5) Recommended chip capacitors layout is as following.</p> <table border="1" data-bbox="472 217 1428 1637"> <thead> <tr> <th data-bbox="472 217 660 297"></th> <th data-bbox="660 217 1043 297">Disadvantage against bending stress</th> <th data-bbox="1043 217 1428 297">Advantage against bending stress</th> </tr> </thead> <tbody> <tr> <td data-bbox="472 297 660 712">Mounting face</td> <td data-bbox="660 297 1043 712"> <p data-bbox="748 342 956 371">Perforation or slit</p>  <p data-bbox="695 607 943 674">Break P.C.board with mounted side up.</p> </td> <td data-bbox="1043 297 1428 712"> <p data-bbox="1131 342 1339 371">Perforation or slit</p>  <p data-bbox="1091 607 1339 674">Break P.C.board with mounted side down.</p> </td> </tr> <tr> <td data-bbox="472 712 660 1160">Chip arrangement (Direction)</td> <td data-bbox="660 712 1043 1160"> <p data-bbox="748 835 956 864">Perforation or slit</p>  </td> <td data-bbox="1043 712 1428 1160"> <p data-bbox="1131 835 1339 864">Perforation or slit</p>  </td> </tr> <tr> <td data-bbox="472 1160 660 1637">Distance from slit</td> <td data-bbox="660 1160 1043 1637"> <p data-bbox="671 1171 1002 1200">Closer to slit is higher stress</p>  <p data-bbox="879 1541 1007 1570">$(l_1 < l_2)$</p> </td> <td data-bbox="1043 1160 1428 1637"> <p data-bbox="1054 1171 1385 1200">Away from slit is less stress</p>  <p data-bbox="1273 1541 1401 1570">$(l_1 < l_2)$</p> </td> </tr> </tbody> </table>		Disadvantage against bending stress	Advantage against bending stress	Mounting face	<p data-bbox="748 342 956 371">Perforation or slit</p>  <p data-bbox="695 607 943 674">Break P.C.board with mounted side up.</p>	<p data-bbox="1131 342 1339 371">Perforation or slit</p>  <p data-bbox="1091 607 1339 674">Break P.C.board with mounted side down.</p>	Chip arrangement (Direction)	<p data-bbox="748 835 956 864">Perforation or slit</p> 	<p data-bbox="1131 835 1339 864">Perforation or slit</p> 	Distance from slit	<p data-bbox="671 1171 1002 1200">Closer to slit is higher stress</p>  <p data-bbox="879 1541 1007 1570">$(l_1 < l_2)$</p>	<p data-bbox="1054 1171 1385 1200">Away from slit is less stress</p>  <p data-bbox="1273 1541 1401 1570">$(l_1 < l_2)$</p>
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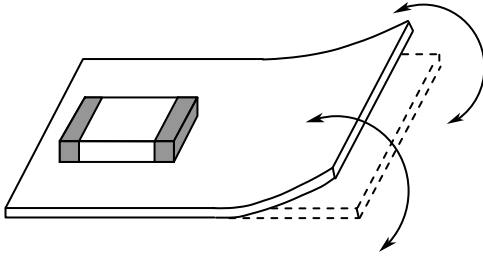
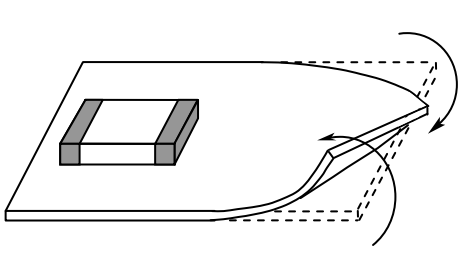
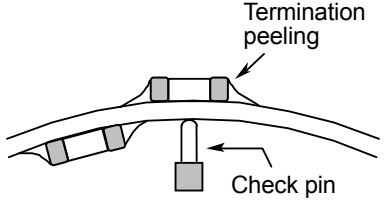
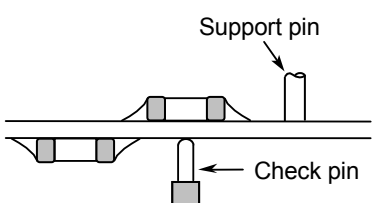
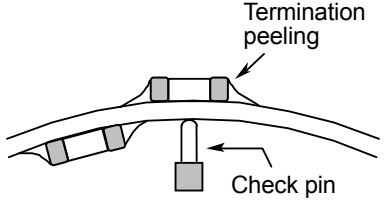
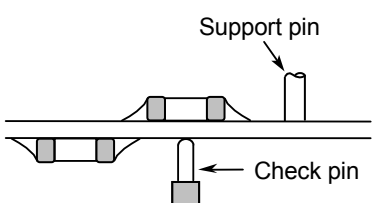
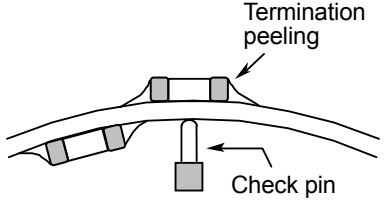
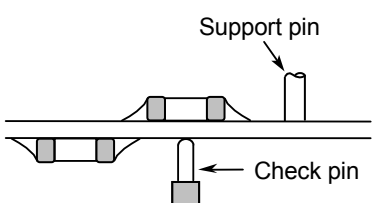
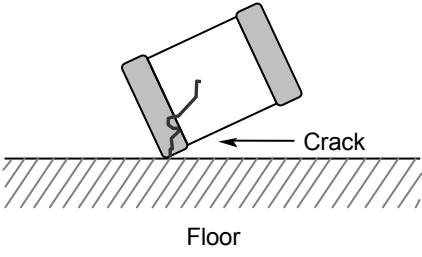
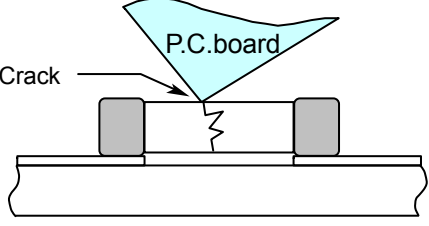
No.	Process	Condition												
3	Designing P.C.board	<p>6) Mechanical stress varies according to location of chip capacitors on the P.C.board.</p>  <p>The stress in capacitors is in the following order. $A > B = C > D > E$</p> <p>7) Layout recommendation</p> <table border="1"> <thead> <tr> <th data-bbox="379 1008 539 1120">Example</th> <th data-bbox="539 1008 842 1120">Use of common solder land</th> <th data-bbox="842 1008 1153 1120">Soldering with chassis</th> <th data-bbox="1153 1008 1489 1120">Use of common solder land with other SMD</th> </tr> </thead> <tbody> <tr> <td data-bbox="379 1120 539 1500">Need to avoid</td> <td data-bbox="539 1120 842 1500">  </td> <td data-bbox="842 1120 1153 1500">  </td> <td data-bbox="1153 1120 1489 1500">  </td> </tr> <tr> <td data-bbox="379 1500 539 1915">Recommendation</td> <td data-bbox="539 1500 842 1915">  </td> <td data-bbox="842 1500 1153 1915">  </td> <td data-bbox="1153 1500 1489 1915">  </td> </tr> </tbody> </table>	Example	Use of common solder land	Soldering with chassis	Use of common solder land with other SMD	Need to avoid				Recommendation			
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No.	Process	Condition									
4	Mounting	<p>4-1. Stress from mounting head</p> <p>If the mounting head is adjusted too low, it may induce excessive stress in the chip capacitors to result in cracking. Please take following precautions.</p> <ol style="list-style-type: none"> 1) Adjust the bottom dead center of the mounting head to reach on the P.C.board surface and not press it. 2) Adjust the mounting head pressure to be 1 to 3N of static weight. 3) To minimize the impact energy from mounting head, it is important to provide support from the bottom side of the P.C.board. See following examples. <table border="1" data-bbox="480 600 1433 1160"> <thead> <tr> <th data-bbox="480 600 663 647"></th> <th data-bbox="663 600 1061 647">Not recommended</th> <th data-bbox="1061 600 1433 647">Recommended</th> </tr> </thead> <tbody> <tr> <td data-bbox="480 647 663 898">Single sided mounting</td> <td data-bbox="663 647 1061 898">  <p>Crack</p> </td> <td data-bbox="1061 647 1433 898">  <p>Support pin</p> </td> </tr> <tr> <td data-bbox="480 898 663 1160">Double-sides mounting</td> <td data-bbox="663 898 1061 1160">  <p>Solder peeling</p> <p>Crack</p> </td> <td data-bbox="1061 898 1433 1160">  <p>Support pin</p> </td> </tr> </tbody> </table> <p>When the centering jaw is worn out, it may give mechanical impact on the capacitors to cause crack. Please control the close up dimension of the centering jaw and provide sufficient preventive maintenance and replacement of it.</p>		Not recommended	Recommended	Single sided mounting	 <p>Crack</p>	 <p>Support pin</p>	Double-sides mounting	 <p>Solder peeling</p> <p>Crack</p>	 <p>Support pin</p>
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No.	Process	Condition														
5	Soldering	<p>5-1. Flux selection</p> <p>Although highly-activated flux gives better solderability, substances which increase activity may also degrade the insulation of the chip capacitors. To avoid such degradation, it is recommended following.</p> <ol style="list-style-type: none"> 1) It is recommended to use a mildly activated rosin flux (less than 0.1wt% chlorine). Strong flux is not recommended. 2) Excessive flux must be avoided. Please provide proper amount of flux. 3) When water-soluble flux is used, enough washing is necessary. <p>5-2. Recommended soldering profile by various methods</p> <div style="text-align: center;"> <p>Reflow soldering</p>  </div> <div style="text-align: center; margin-top: 20px;"> <p>Manual soldering (Solder iron)</p>  </div> <p>5-3. Recommended soldering peak temp and peak temp duration</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th rowspan="2" style="text-align: center;">Temp./Duration</th> <th colspan="2" style="text-align: center;">Reflow soldering</th> </tr> <tr> <th style="text-align: center;">Peak temp(°C)</th> <th style="text-align: center;">Duration(sec.)</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">Solder</td> <td></td> <td></td> </tr> <tr> <td style="text-align: center;">Sn-Pb Solder</td> <td style="text-align: center;">230 max.</td> <td style="text-align: center;">20 max.</td> </tr> <tr> <td style="text-align: center;">Lead Free Solder</td> <td style="text-align: center;">260 max.</td> <td style="text-align: center;">10 max.</td> </tr> </tbody> </table> <p>Recommended solder compositions</p> <p>Sn-37Pb (Sn-Pb solder)</p> <p>Sn-3.0Ag-0.5Cu (Lead Free Solder)</p>	Temp./Duration	Reflow soldering		Peak temp(°C)	Duration(sec.)	Solder			Sn-Pb Solder	230 max.	20 max.	Lead Free Solder	260 max.	10 max.
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5	Soldering	<p>5-4. Avoiding thermal shock</p> <p>1) Preheating condition</p> <table border="1" data-bbox="552 264 1396 551"> <thead> <tr> <th>Soldering</th> <th>Type</th> <th>Temp. (°C)</th> </tr> </thead> <tbody> <tr> <td rowspan="2">Reflow soldering</td> <td>C3216</td> <td>$\Delta T \leq 150$</td> </tr> <tr> <td>C3225, C4520 C4532, C5750</td> <td>$\Delta T \leq 130$</td> </tr> <tr> <td rowspan="2">Manual soldering</td> <td>C3216</td> <td>$\Delta T \leq 150$</td> </tr> <tr> <td>C3225, C4520 C4532, C5750</td> <td>$\Delta T \leq 130$</td> </tr> </tbody> </table> <p>2) Cooling condition</p> <p>Natural cooling using air is recommended. If the chips are dipped into a solvent for cleaning, the temperature difference (ΔT) must be less than 100°C.</p> <p>5-5. Amount of solder</p> <p>Excessive solder will induce higher tensile force in chip capacitors when temperature changes and it may result in chip cracking. In sufficient solder may detach the capacitors from the P.C.board.</p> <div style="display: flex; justify-content: space-between; align-items: flex-start;"> <div style="width: 30%;">Excessive solder</div> <div style="width: 30%; text-align: center;">  </div> <div style="width: 30%; text-align: right;">Higher tensile force in chip capacitors to cause crack</div> </div> <hr/> <div style="display: flex; justify-content: space-between; align-items: center;"> <div style="width: 30%;">Adequate</div> <div style="width: 30%; text-align: center;">  </div> </div> <hr/> <div style="display: flex; justify-content: space-between; align-items: flex-start;"> <div style="width: 30%;">Insufficient solder</div> <div style="width: 30%; text-align: center;">  </div> <div style="width: 30%; text-align: right;">Low robustness may cause contact failure or chip capacitors come off the P.C.board.</div> </div> <p>5-6. Solder repair by solder iron</p> <p>1) Selection of the soldering iron tip</p> <p>Tip temperature of solder iron varies by its type, P.C.board material and solder land size. The higher the tip temperature, the quicker the operation. However, heat shock may cause a crack in the chip capacitors. Please make sure the tip temp. before soldering and keep the peak temp and time in accordance with following recommended condition. (Please preheat the chip capacitors with the condition in 5-4 to avoid the thermal shock.)</p> <p>Recommended solder iron condition (Sn-Pb Solder and Lead Free Solder)</p> <table border="1" data-bbox="552 1751 1396 1859"> <thead> <tr> <th>Temp. (°C)</th> <th>Duration (sec.)</th> <th>Wattage (W)</th> <th>Shape (mm)</th> </tr> </thead> <tbody> <tr> <td>300 max.</td> <td>3 max.</td> <td>20 max.</td> <td>Ø 3.0 max.</td> </tr> </tbody> </table>	Soldering	Type	Temp. (°C)	Reflow soldering	C3216	$\Delta T \leq 150$	C3225, C4520 C4532, C5750	$\Delta T \leq 130$	Manual soldering	C3216	$\Delta T \leq 150$	C3225, C4520 C4532, C5750	$\Delta T \leq 130$	Temp. (°C)	Duration (sec.)	Wattage (W)	Shape (mm)	300 max.	3 max.	20 max.	Ø 3.0 max.
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No.	Process	Condition
5	Soldering	<p>2) Direct contact of the soldering iron with ceramic dielectric of chip capacitors may cause crack. Do not touch the ceramic dielectric and the terminations by solder iron.</p> <p>5-7. Sn-Zn solder Sn-Zn solder affects product reliability. Please contact TDK in advance when utilize Sn-Zn solder.</p> <p>5-8. Countermeasure for tombstone The misalignment between the mounted positions of the capacitors and the land patterns should be minimized. The tombstone phenomenon may occur especially the capacitors are mounted (in longitudinal direction) in the same direction of the reflow soldering. (Refer to JEITA RCR-2335B Annex 1 (Informative) Recommendations to prevent the tombstone phenomenon)</p>
6	Cleaning	<p>1) If an unsuitable cleaning fluid is used, flux residue or some foreign articles may stick to chip capacitors surface to deteriorate especially the insulation resistance.</p> <p>2) If cleaning condition is not suitable, it may damage the chip capacitors.</p> <p>2)-1. Insufficient washing (1) Terminal electrodes may corrode by Halogen in the flux. (2) Halogen in the flux may adhere on the surface of capacitors, and lower the insulation resistance. (3) Water soluble flux has higher tendency to have above mentioned problems (1) and (2).</p> <p>2)-2. Excessive washing When ultrasonic cleaning is used, excessively high ultrasonic energy output can affect the connection between the ceramic chip capacitor's body and the terminal electrode. To avoid this, following is the recommended condition. Power : 20 W/l max. Frequency : 40 kHz max. Washing time : 5 minutes max.</p> <p>2)-3. If the cleaning fluid is contaminated, density of Halogen increases, and it may bring the same result as insufficient cleaning.</p>
7	Coating and molding of the P.C.board	<p>1) When the P.C.board is coated, please verify the quality influence on the product.</p> <p>2) Please verify carefully that there is no harmful decomposing or reaction gas emission during curing which may damage the chip capacitors.</p> <p>3) Please verify the curing temperature.</p>

No.	Process	Condition						
8	Handling after chip mounted ⚠ Caution	<p>1) Please pay attention not to bend or distort the P.C.board after soldering in handling otherwise the chip capacitors may crack.</p> <div style="display: flex; justify-content: space-around; align-items: center;"> <div style="text-align: center;"> <p>Bend</p>  </div> <div style="text-align: center;"> <p>Twist</p>  </div> </div> <p>2) When functional check of the P.C.board is performed, check pin pressure tends to be adjusted higher for fear of loose contact. But if the pressure is excessive and bend the P.C.board, it may crack the chip capacitors or peel the terminations off. Please adjust the check pins not to bend the P.C.board.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th data-bbox="488 860 628 922">Item</th> <th data-bbox="628 860 1046 922">Not recommended</th> <th data-bbox="1046 860 1445 922">Recommended</th> </tr> </thead> <tbody> <tr> <td data-bbox="488 922 628 1223" style="text-align: center; vertical-align: middle;">Board bending</td> <td data-bbox="628 922 1046 1223" style="text-align: center;">  </td> <td data-bbox="1046 922 1445 1223" style="text-align: center;">  </td> </tr> </tbody> </table>	Item	Not recommended	Recommended	Board bending		
Item	Not recommended	Recommended						
Board bending								
9	Handling of loose chip capacitors	<p>1) If dropped the chip capacitors may crack. Once dropped do not use it. Especially, the large case sized chip capacitors are tendency to have cracks easily, so please handle with care.</p> <div style="text-align: center;">  </div> <p>2) Piling the P.C.board after mounting for storage or handling, the corner of the P.C. board may hit the chip capacitors of another board to cause crack.</p> <div style="text-align: center;">  </div>						

No.	Process	Condition
10	Capacitance aging	The capacitors (Class 2) have aging in the capacitance. They may not be used in precision time constant circuit. In case of the time constant circuit, the evaluation should be done well.
11	Estimated life and estimated failure rate of capacitors	As per the estimated life and the estimated failure rate depend on the temperature and the voltage. This can be calculated by the equation described in JEITA RCR-2335B Annex 6 (Informative) Calculation of the estimated lifetime and the estimated failure rate (Voltage acceleration coefficient : 3 multiplication rule, Temperature acceleration coefficient : 10°C rule) The failure rate can be decreased by reducing the temperature and the voltage but they will not be guaranteed.
12	Others △ Caution	<p>The products listed on this specification sheet are intended for use in general electronic equipment (AV equipment, telecommunications equipment, home appliances, amusement equipment, computer equipment, personal equipment, office equipment, measurement equipment, industrial robots) under a normal operation and use condition.</p> <p>The products are not designed or warranted to meet the requirements of the applications listed below, whose performance and/or quality require a more stringent level of safety or reliability, or whose failure, malfunction or trouble could cause serious damage to society, person or property. Please understand that we are not responsible for any damage or liability caused by use of the products in any of the applications below or for any other use exceeding the range or conditions set forth in this specification sheet. If you intend to use the products in the applications listed below or if you have special requirements exceeding the range or conditions set forth in this specification, please contact us.</p> <p>(1) Aerospace/Aviation equipment (2) Transportation equipment (cars, electric trains, ships, etc.) (3) Medical equipment (4) Power-generation control equipment (5) Atomic energy-related equipment (6) Seabed equipment (7) Transportation control equipment (8) Public information-processing equipment (9) Military equipment (10) Electric heating apparatus, burning equipment (11) Disaster prevention/crime prevention equipment (12) Safety equipment (13) Other applications that are not considered general-purpose applications</p> <p>When designing your equipment even for general-purpose applications, you are kindly requested to take into consideration securing protection circuit/device or providing backup circuits in your equipment.</p>

13. Packaging label

Packaging shall be done to protect the components from the damage during transportation and storing, and a label which has the following information shall be attached.

- 1) Inspection No.
- 2) TDK P/N
- 3) Customer's P/N
- 4) Quantity

*Composition of Inspection No.

Example M 2 A - 00 - 000
 (a) (b) (c) (d) (e)

- a) Line code
- b) Last digit of the year
- c) Month and A for January and B for February and so on. (Skip I)
- d) Inspection Date of the month.
- e) Serial No. of the day

14. Bulk packaging quantity

Total number of components in a plastic bag for bulk packaging: 1,000pcs.

15. TAPE PACKAGING SPECIFICATION

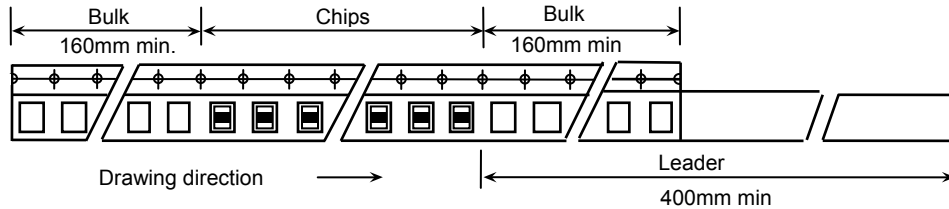
1. CONSTRUCTION AND DIMENSION OF TAPING

1-1. Dimensions of carrier tape

Dimensions of paper tape shall be according to Appendix 2.

Dimensions of plastic tape shall be according to Appendix 3,4.

1-2. Bulk part and leader of taping

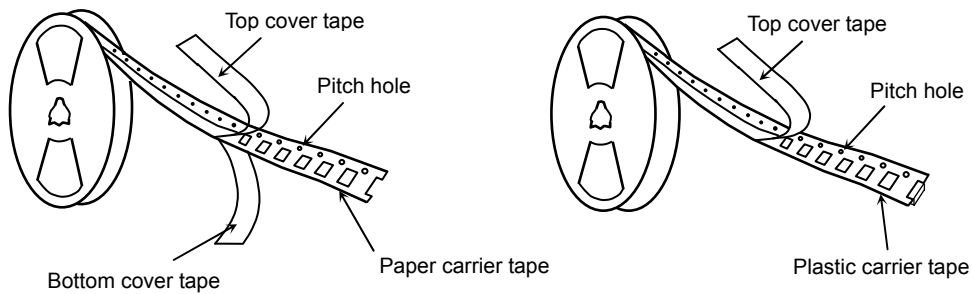


1-3. Dimensions of reel

Dimensions of Ø178 reel shall be according to Appendix 5,6.

Dimensions of Ø330 reel shall be according to Appendix 7,8.

1-4. Structure of taping



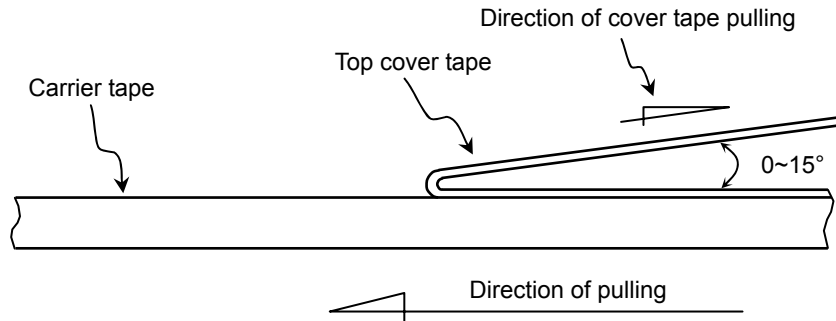
2. CHIP QUANTITY

Type	Thickness of chip	Taping Material	Chip quantity(pcs.)	
			φ178mm reel	φ330mm reel
C3216	0.85 mm	paper	4,000	10,000
	1.30 mm	plastic	2,000	
C3225	1.60 mm	plastic	2,000	8,000
	2.00 mm		1,000	5,000
	2.50 mm			
C4520	0.85 mm	plastic	1,000	5,000
	1.10 mm			
	1.30 mm			3,000
	2.00 mm			
C4532	1.30 mm	plastic	1,000	5,000
	1.60 mm			
	2.00 mm			3,000
	2.30 mm			
	2.50 mm		500	
C5750	1.60 mm	plastic	1,000	3,000
	2.00 mm		500	
	2.50 mm			

3. PERFORMANCE SPECIFICATIONS

3-1. Fixing peeling strength (top tape)

0.05-0.7N. (See the following figure.)



3-2. Carrier tape shall be flexible enough to be wound around a minimum radius of 30mm with components in tape.

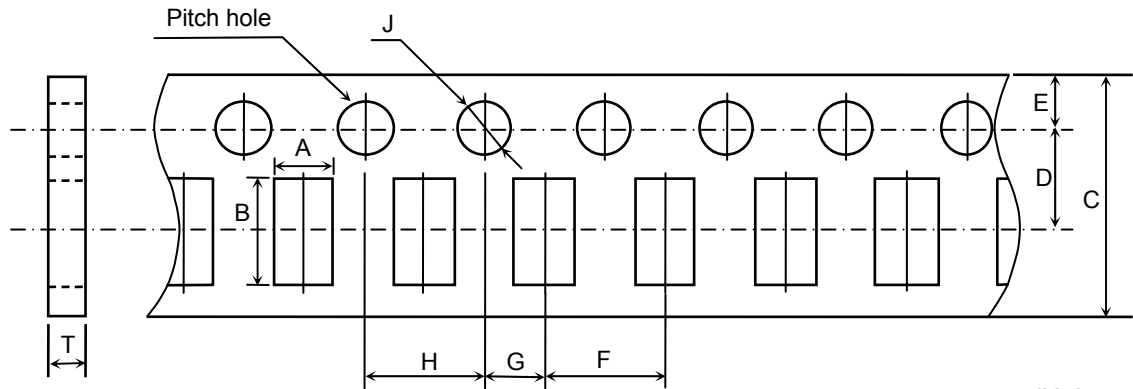
3-3. The missing of components shall be less than 0.1%

3-4. Components shall not stick to fixing tape.

3-5. The fixing tapes shall not protrude beyond the edges of the carrier tape not shall cover the sprocket holes.

Appendix 2

Paper Tape



(Unit : mm)

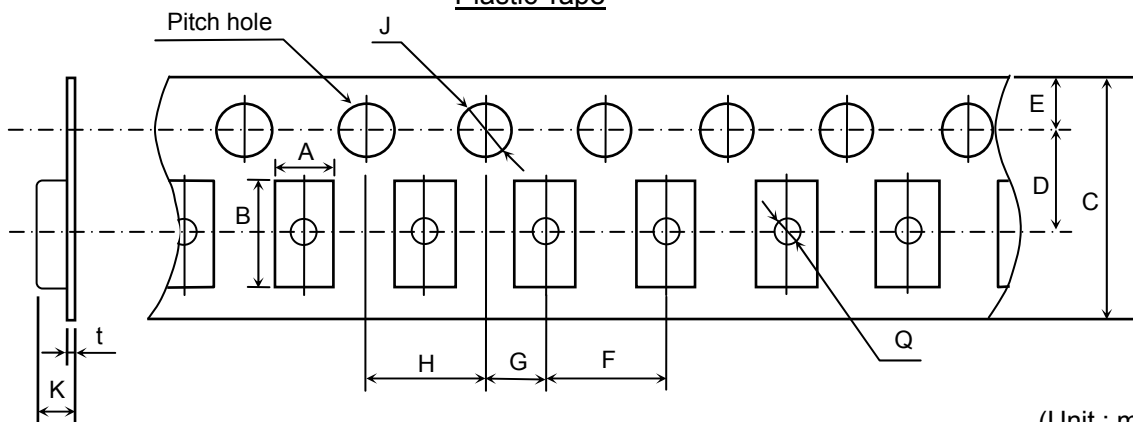
Symbol Type	A	B	C	D	E	F
C3216 (CC1206)	(1.90)	(3.50)	8.00 ± 0.30	3.50 ± 0.05	1.75 ± 0.10	4.00 ± 0.10

Symbol Type	G	H	J	T
C3216 (CC1206)	2.00 ± 0.05	4.00 ± 0.10	$\varnothing 1.5 \begin{smallmatrix} +0.10 \\ 0 \end{smallmatrix}$	1.10 max.

* The values in the parentheses () are for reference.

Appendix 3

Plastic Tape



(Unit : mm)

Symbol Type	A	B	C	D	E	F
C3216 (CC1206)	(1.90)	(3.50)	8.00 ± 0.30	3.50 ± 0.05	1.75 ± 0.10	4.00 ± 0.10
C3225 (CC1210)	(2.90)	(3.60)	$[12.0 \pm 0.30]$	$[5.50 \pm 0.05]$		

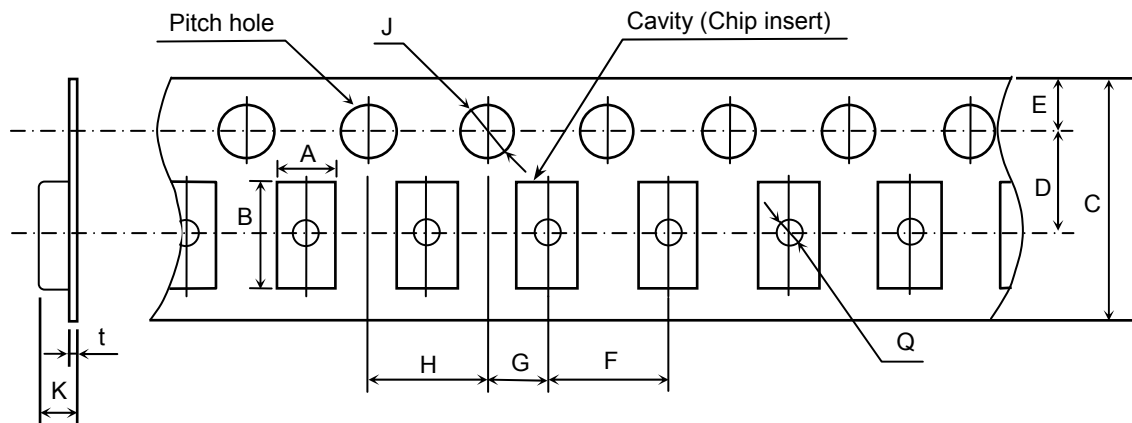
Symbol Type	G	H	J	K	t	Q
C3216 (CC1206)	2.00 ± 0.05	4.00 ± 0.10	$\varnothing 1.5 \begin{smallmatrix} +0.10 \\ 0 \end{smallmatrix}$	2.50 max.	0.30 max.	$\varnothing 0.50$ min.
C3225 (CC1210)				3.20 max.	0.60 max.	

* The values in the parentheses () are for reference.

* As for 2.5mm thickness products, apply values in the brackets [].

Appendix 4

Plastic Tape



(Unit : mm)

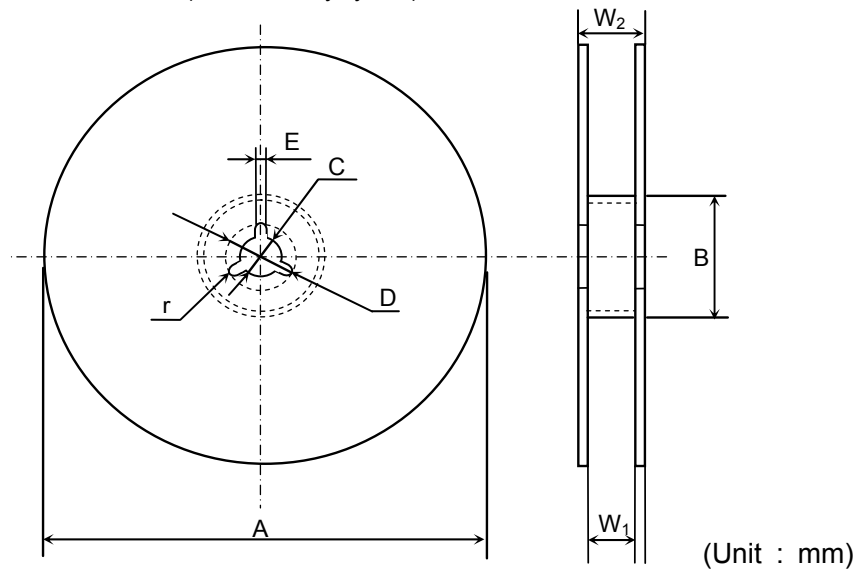
Symbol Type	A	B	C	D	E	F
C4520 (CC1808)	(2.50)	(5.10)	12.0 ± 0.30	5.50 ± 0.05	1.75 ± 0.10	8.00 ± 0.10
C4532 (CC1812)	(3.60)	(4.90)				
C5750 (CC2220)	(5.40)	(6.10)				

Symbol Type	G	H	J	K	t	Q
C4520 (CC1808)	2.00 ± 0.05	4.00 ± 0.10	∅ 1.5 ^{+0.10} ₀	6.50 max.	0.60 max.	∅ 1.50 min.
C4532 (CC1812)						
C5750						

* The values in the parentheses () are for reference.

Appendix 5

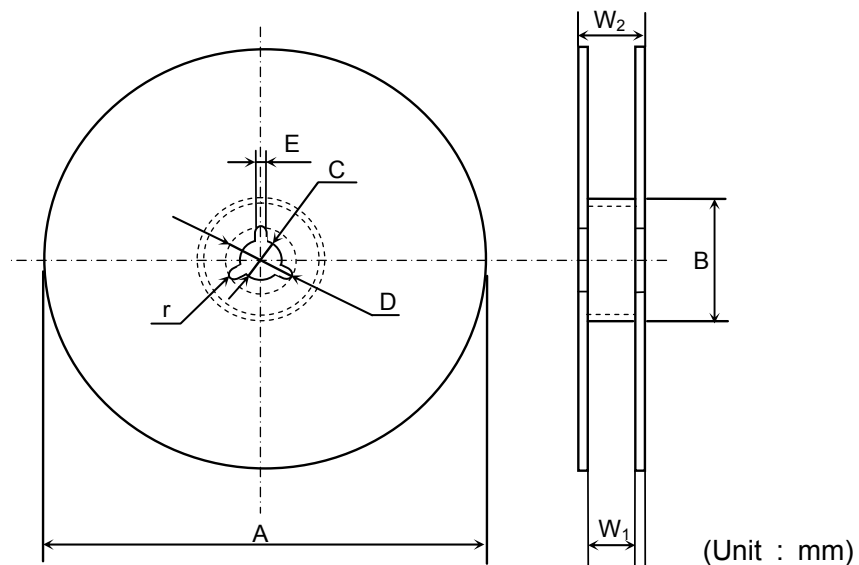
C3216, C3225
 (As for C3225 type, any thickness of the item except 2.5mm)
 (Material : Polystyrene)



Symbol	A	B	C	D	E	W ₁
Dimension	Ø178 ± 2.0	Ø60 ± 2.0	Ø13 ± 0.5	Ø21 ± 0.8	2.0 ± 0.5	9.0 ± 0.3
Symbol	W ₂	r				
Dimension	13.0 ± 1.4	1.0				

Appendix 6

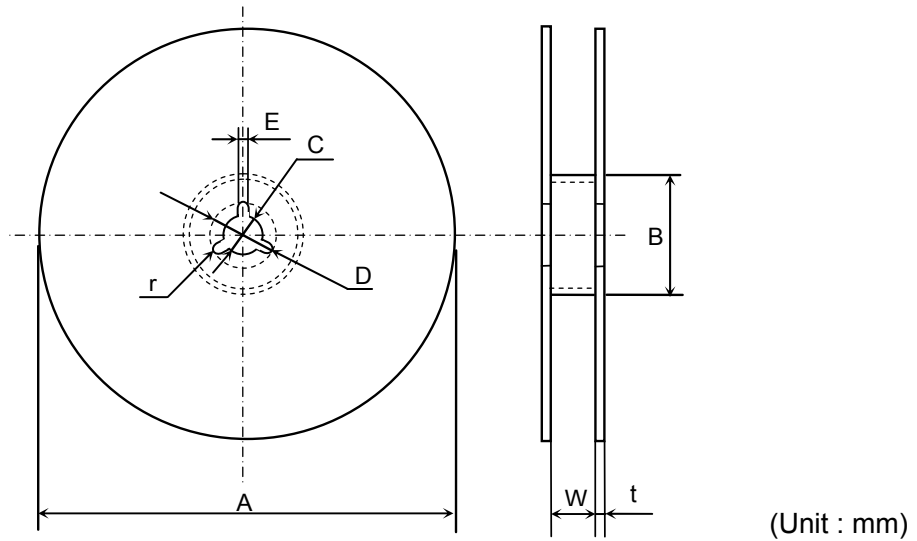
C3225, C4520, C4532, C5750 (As for C3225 type, applied to 2.5mm thickness products)
 (Material : Polystyrene)



Symbol	A	B	C	D	E	W ₁
Dimension	Ø178 ± 2.0	Ø60 ± 2.0	Ø13 ± 0.5	Ø21 ± 0.8	2.0 ± 0.5	13.0 ± 0.3
Symbol	W ₂	r				
Dimension	17.0 ± 1.4	1.0				

Appendix 7

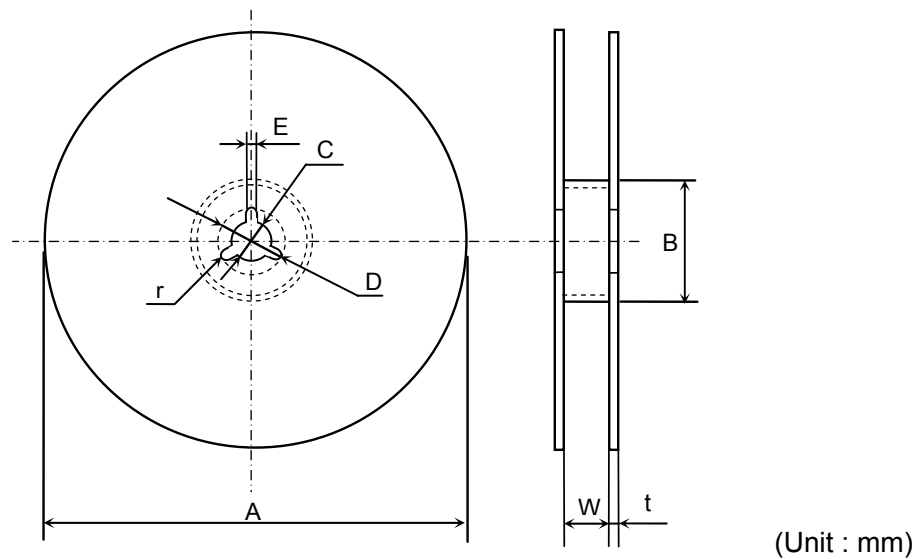
C3216, C3225 (As for C3225 type, any thickness of the item except 2.5mm)
(Material : Polystyrene)



Symbol	A	B	C	D	E	W
Dimension	Ø382 max. (Nominal Ø330)	Ø50 min.	Ø13 ± 0.5	Ø21 ± 0.8	2.0 ± 0.5	10.0 ± 1.5
Symbol	t	r				
Dimension	2.0 ± 0.5	1.0				

Appendix 8

C3225, C4520, C4532, C5750 (As for C3225 type, applied to 2.5mm thickness products)
(Material : Polystyrene)



Symbol	A	B	C	D	E	W
Dimension	Ø382 max. (Nominal Ø330)	Ø50 min.	Ø13 ± 0.5	Ø21 ± 0.8	2.0 ± 0.5	14.0 ± 1.5
Symbol	t	r				
Dimension	2.0 ± 0.5	1.0				