LP5900 Ultra Low Noise, 150 mA Linear Regulator for RF/Analog Circuits Requires No Bypass Capacitor

Check for Samples: LP5900

FEATURES

- **Stable with 0.47 µF Ceramic Input and Output Capacitors**
- **No Noise Bypass Capacitor Required**
- **Logic Controlled Enable**
- **Thermal-Overload and Short-Circuit Protection**
- **−40°C to +125°C Junction Temperature Range for Operation**

KEY SPECIFICATIONS

- **Input Voltage Range, 2.5V to 5.5V**
- **Output Voltage Range, 1.5V to 4.5V**
- **Output Current, 150 mA**
- **Low Output Voltage Noise, 6.5 μV_{RMS}**
- **PSRR, 75 dB at 1 kHz**
- **Output Voltage Tolerance, ± 2%**
- **Virturally Zero I_Q (Disabled), <1 µA**
- **Very Low I_Q (Enabled), 25 µA**
- **Startup Time, 150 µs**
- **Low Dropout, 80 mV Typ.**

PACKAGE

- **4-Bump DSBGA (YZR), 1.057 mm x 1.083 mm x 0.600 mm (lead free)**
- **Extreme Thin 4-Bump DSBGA (YPF), 1.067 mm x 1.092 mm x 0.250 mm (lead free)**
- **6-Pin WSON, 2.2 mm x 2.5 mm x 0.8 mm (SC70 footprint, halogen free)**

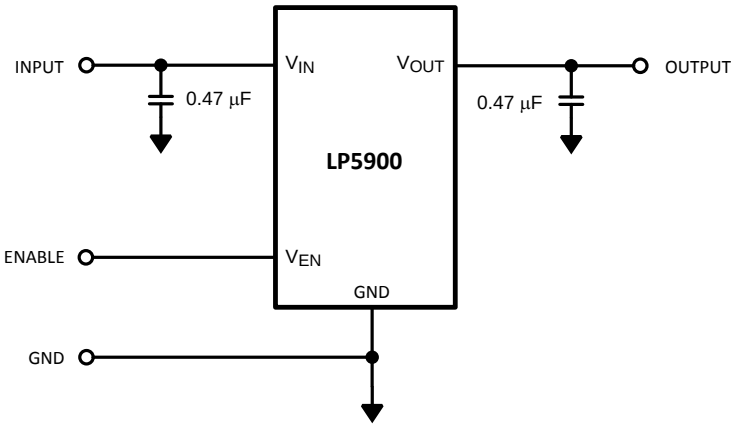
APPLICATIONS

- **Cellular Phones**
- **PDA Handsets**
- **Wireless LAN Devices**

DESCRIPTION

The LP5900 is a linear regulator capable of supplying 150 mA output current. Designed to meet the requirements of RF/Analog circuits, the LP5900 device provides low noise, high PSRR, low quiescent current, and low line transient response figures. Using new innovative design techniques the LP5900 offers class-leading device noise performance without a noise bypass capacitor.

Typical Application Circuit



DESCRIPTION (CONTINUED)

The device is designed to work with 0.47 µF input and output ceramic capacitors. (No Bypass Capacitor is required)

The device is available in DSBGA (YZR) package and WSON package. Also available in Extreme Thin SDBGA (YPF) package. For all other package options, contact your local Texas Instruments sales office.

This device is available with 1.5V,1.575V, 1.8V, 1.9V, 2.0V, 2.1V, 2.2V, 2.3V, 2.5V, 2.6V, 2.65V, 2.7V, 2.75V 2.8V, 2.85V 3.0V, 3.3V and 4.5V outputs. Please contact your local sales office for any other voltage options.

Connection Diagrams

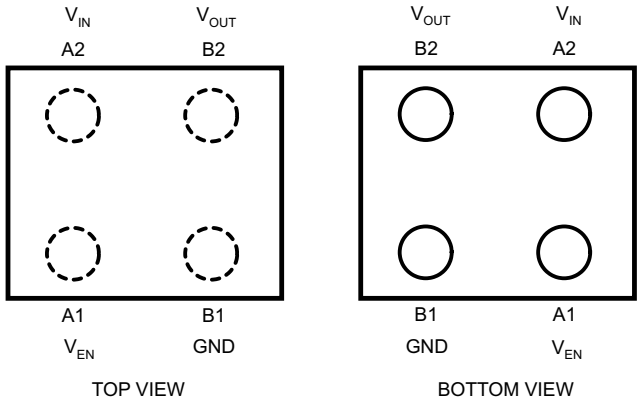


Figure 1. 4-Bump Thin DSBGA (YZR) Package and Extreme Thin DSBGA (YPF) Package, Large Bump (See Package Number YZR0004/YPF0004)

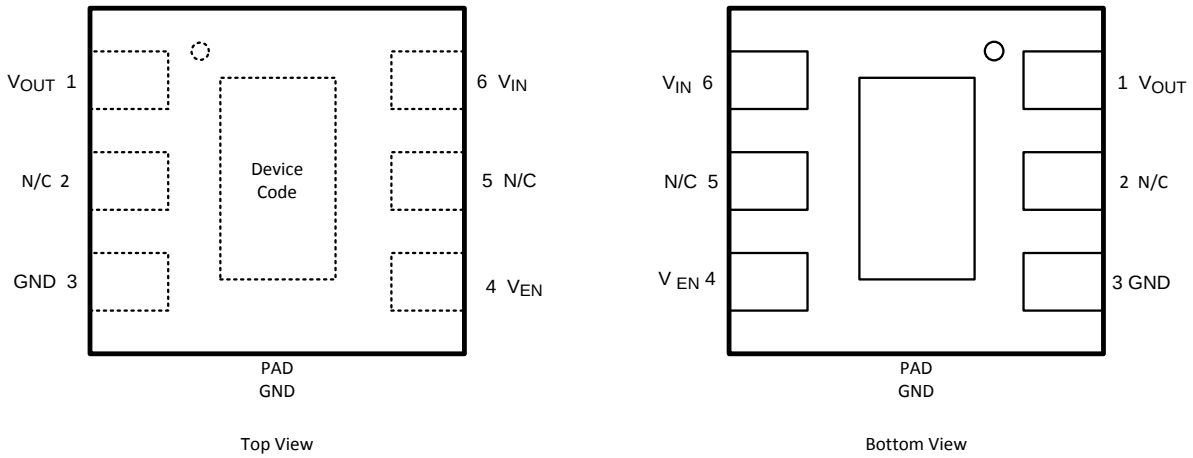


Figure 2. WSON-6 Package (See Package Number NGF0006A)

PIN DESCRIPTIONS

Pin No.		Symbol	Name and Function
DSBGA	WSON		
A1	4	V_{EN}	Enable input; disables the regulator when ≤ 0.4V. Enables the regulator when ≥ 1.2V. An internal 1 MΩ pulldown resistor connects this input to ground.
B1	3	GND	Common ground
B2	1	V_{OUT}	Output voltage. A 0.47 µF Low ESR capacitor should be connected to this Pin. Connect this output to the load circuit.
A2	6	V_{IN}	Input voltage supply. A 0.47 µF capacitor should be connected at this input.

PIN DESCRIPTIONS (continued)

Pin No.		Symbol	Name and Function
DSBGA	WSON		
	Pad	GND	Common Ground. Connect to Pin 3.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)(2)(3)

V_{IN} Pin: Input Voltage	-0.3 to 6.0V
V_{OUT} Pin: Output Voltage	-0.3 to (V_{IN} + 0.3V) to 6.0V (max)
V_{EN} Pin: Enable Input Voltage	-0.3 to (V_{IN} + 0.3V) to 6.0V (max)
Continuous Power Dissipation (4)	Internally Limited
Junction Temperature (T_{JMAX})	150°C
Storage Temperature Range	-65 to 150°C
Maximum Lead Temperature (Soldering, 10 sec.)	260°C
ESD Rating (5)	
Human Body Model	2 kV
Machine Model	200V

(1) Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is ensured. Operating Ratings do not imply ensured performance limits. For ensured performance limits and associated test conditions, see the Electrical Characteristics tables.
(2) All voltages are with respect to the potential at the GND pin.
(3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(4) Internal thermal shutdown circuitry protects the device from permanent damage.
(5) The Human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin. The machine model is a 200 pF capacitor discharged directly into each pin. MIL-STD-883 3015.7

Operating Ratings (1)(2)

V_{IN}: Input Voltage Range	2.5V to 5.5V
V_{EN}: Enable Voltage Range	0 to (V_{IN} + 0.3V) to 5.5V (max)
Recommended Load Current (3)	0 to 150 mA
Junction Temperature Range (T_J)	-40°C to +125°C
Ambient Temperature Range (T_A) (3)	-40°C to +85°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is ensured. Operating Ratings do not imply ensured performance limits. For ensured performance limits and associated test conditions, see the Electrical Characteristics tables.
(2) All voltages are with respect to the potential at the GND pin.
(3) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature ($T_{A\text{-}MAX}$) is dependent on the maximum operating junction temperature ($T_{J\text{-}MAX\text{-}OP}$ = 125°C), the maximum power dissipation of the device in the application ($P_{D\text{-}MAX}$), and the junction-to ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: $T_{A\text{-}MAX} = T_{J\text{-}MAX\text{-}OP} – (\theta_{JA} \times P_{D\text{-}MAX})$. See applications section.

Thermal Properties

Junction to Ambient Thermal Resistance θ_{JA} (1)	
(2) JEDEC Board (DSBGA)	88°C/W
4L Cellphone Board (DSBGA)	157.4°C/W
JEDEC Board (WSON-6) (2)	77.3°C/W

(1) Junction-to-ambient thermal resistance is highly application and board-layout dependent. In applications where high maximum power dissipation exists, special care must be paid to thermal dissipation issues in board design.
(2) Detailed description of the board can be found in JESD51-7

Electrical Characteristics

Limits in standard typeface are for T_A = 25ºC. Limits in **boldface** type apply over the full operating junction temperature range (-40°C ≤ T_J ≤ +125°C). Unless otherwise noted, specifications apply to the LP5900 Typical Application Circuit (pg. 1) with: V_{IN} = $V_{OUT\ (NOM)}$ + 1.0V, V_{EN} = 1.2V, C_{IN} = C_{OUT} = 0.47 µF, I_{OUT} = 1.0 mA. (1), (2)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IN}	Input Voltage			2.5		5.5	V
ΔV_{OUT}	Output Voltage Tolerance	V_{IN} = ($V_{OUT(NOM)}$ + 1.0V) to 5.5V, I_{OUT} = 1 mA to 150mA		**−2**		**2**	%
	Line Regulation	V_{IN} = ($V_{OUT(NOM)}$ + 1.0V) to 5.5V, I_{OUT} = 1 mA			0.05		%/V
	Load Regulation	I_{OUT} = 1 mA to 150 mA			0.001		%/mA
I_{LOAD}	Load Current	(3)		0			mA
	Maximum Output Current			**150**			
I_Q	Quiescent Current (4)	V_{EN} = 1.2V, I_{OUT} = 0 mA			25	**50**	µA
		V_{EN} = 1.2V, I_{OUT} = 150 mA			160	**230**	
		V_{EN} = 0.3V (Disabled)			0.003	**1.0**	
I_G	Ground Current (5)	I_{OUT} = 0 mA (V_{OUT} = 2.5V)			30		µA
V_{DO}	Dropout Voltage (6)	I_{OUT} = 150 mA			80	**150**	mV
I_{SC}	Short Circuit Current Limit	(7)			300		mA
PSRR	Power Supply Rejection Ratio (8)	f = 100 Hz, I_{OUT} = 150 mA			85		dB
		f = 1 kHz, I_{OUT} = 150 mA			75		
		f = 10 kHz, I_{OUT} = 150 mA			65		
		f = 50 kHz, I_{OUT} = 150 mA			52		
		f = 100 kHz, I_{OUT} = 150 mA			40		
e_n	Output Noise Voltage (8)	BW = 10 Hz to 100 kHz, V_{IN} = 4.2V	I_{OUT} = 0 mA		7		μV_{RMS}
			I_{OUT} = 1 mA		10		
			I_{OUT} = 150 mA		6.5		
$T_{SHUTDOWN}$	Thermal Shutdown	Temperature			160		ºC
		Hysteresis			20		
Login Input Thresholds							
V_{IL}	Low Input Threshold (V_{EN})	V_{IN} = 2.5V to 5.5V				**0.4**	V
V_{IH}	High Input Threshold (V_{EN})	V_{IN} = 2.5V to 5.5V		**1.2**			V

(1) All voltages are with respect to the potential at the GND pin.
(2) Min and Max limits are specified by design, test, or statistical analysis. Typical numbers are not ensured, but do represent the most likely norm.
(3) The device maintains a stable, regulated output voltage without a load current.
(4) Quiescent current is defined here as the difference in current between the input voltage source and the load at V_{OUT}.
(5) Ground current is defined here as the total current flowing to ground as a result of all input voltages applied to the device.
(6) Dropout voltage is the voltage difference between the input and the output at which the output voltage drops to 100 mV below its nominal value. This parameter only applies to output voltages above 2.5V.
(7) Short Circuit Current is measured with V_{OUT} pulled to 0v and V_{IN} worst case = 6.0V.
(8) This specification is specified by design.

Electrical Characteristics (continued)

Limits in standard typeface are for T_A = 25ºC. Limits in **boldface** type apply over the full operating junction temperature range (-40°C ≤ T_J ≤ +125°C). Unless otherwise noted, specifications apply to the LP5900 Typical Application Circuit (pg. 1) with: V_{IN} = $V_{OUT\ (NOM)}$ + 1.0V, V_{EN} = 1.2V, C_{IN} = C_{OUT} = 0.47 µF, I_{OUT} = 1.0 mA. (1), (2)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{EN}	Input Current at V_{EN} Pin (9)	V_{EN} = 5.5V and V_{IN} = 5.5V		5.5		µA
		V_{EN} = 0.0V and V_{IN} = 5.5V		0.001		
Transient Characteristics						
ΔV_{OUT}	Line Transient (8)	V_{IN} = ($V_{OUT(NOM)}$) + 1.0V) to ($V_{OUT(NOM)}$) + 1.6V) in 30 µs, I_{OUT} = 1 mA	**−2**			mV
		V_{IN} = ($V_{OUT(NOM)}$) + 1.6V) to ($V_{OUT(NOM)}$ + 1.0V) in 30 µs, I_{OUT} = 1 mA			**2**	
	Load Transient (8)	I_{OUT} = 1 mA to 150 mA in 10 µs	**−110**			mV
		I_{OUT} = 150 mA to 1 mA in 10 µs			**50**	
	Overshoot on Startup (8)				**20**	mV
	Turn on Time	To 95% of $V_{OUT(NOM)}$		150	300	µs

(9) There is a 1 MΩ resistor between V_{EN} and ground on the device.

Output & Input Capacitor, Recommended Specifications

Symbol	Parameter	Conditions	Min	Nom	Max	Units
C_{IN}	Input Capacitance	Capacitance for stability	**0.33**	0.47		µF
C_{OUT}	Output Capacitance		**0.33**	0.47	**10**	
ESR	Output/Input Capacitance		5		500	mΩ

Typical Performance Characteristics.

Unless otherwise specified, $C_{IN} = C_{OUT} = 0.47\mu F$, $V_{IN} = V_{OUT(NOM)} + 1.0V$, $V_{EN} = 1.2V$, $I_{OUT} = 1mA$, $T_A = 25°C$.

Output Noise Density

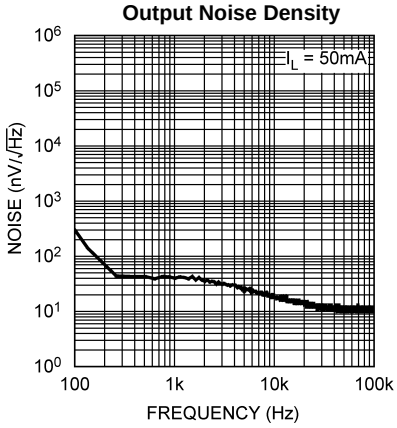


Figure 3.

Power Supply Rejection Ratio

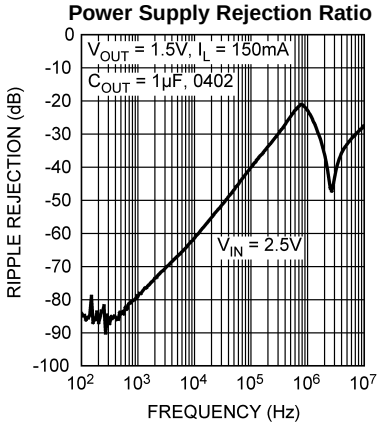


Figure 4.

Power Supply Rejection Ratio

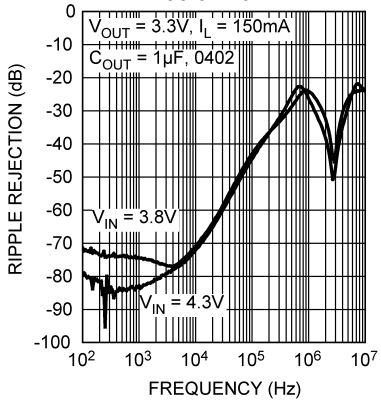


Figure 5.

Output Voltage Change vs Temperature

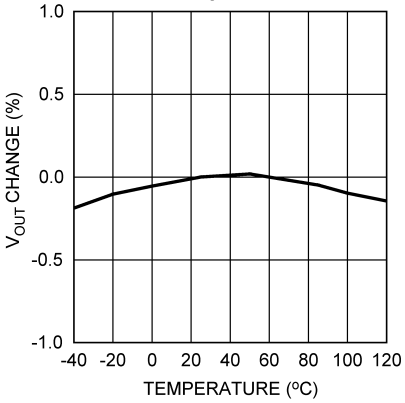


Figure 6.

Ground Current vs V_{IN}, I_{LOAD} = 0mA

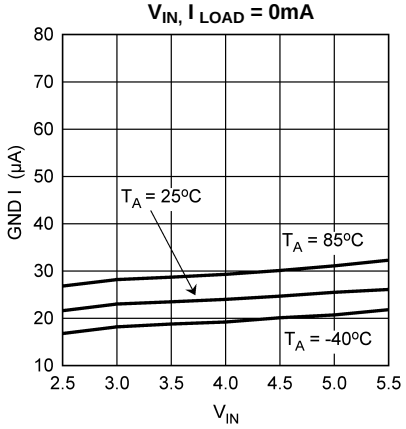


Figure 7.

Ground Current vs V_{IN}, I_{LOAD} = 1mA

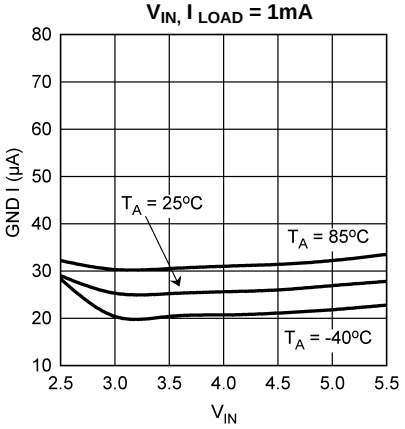


Figure 8.

Typical Performance Characteristics. (continued)

Unless otherwise specified, $C_{IN} = C_{OUT} = 0.47\mu F$, $V_{IN} = V_{OUT(NOM)} + 1.0V$, $V_{EN} = 1.2V$, $I_{OUT} = 1mA$, $T_A = 25°C$.

Ground Current vs V_{IN}, I_{LOAD} = 100mA

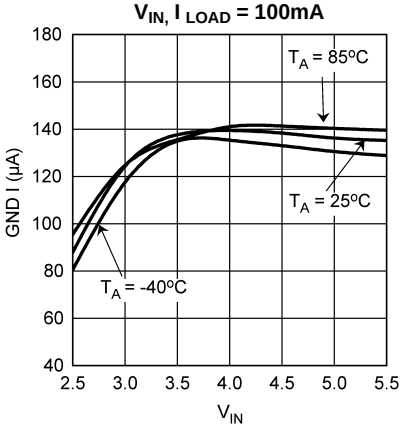


Figure 9.

Ground Current vs Load Current

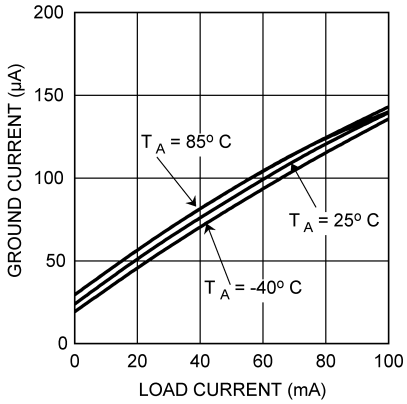


Figure 10.

Short Circuit Current

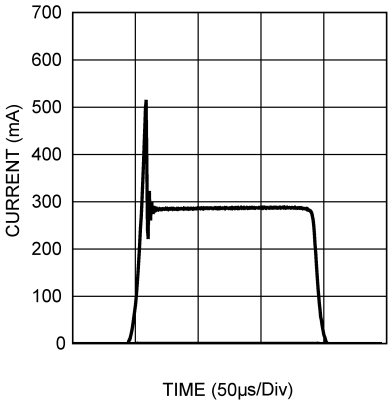


Figure 11.

Load Transient

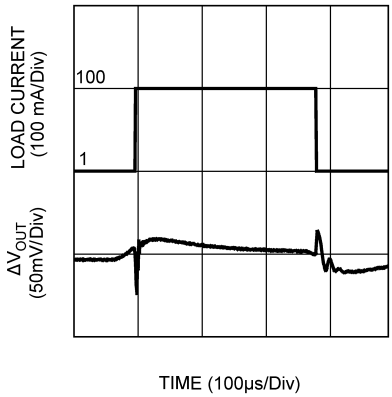


Figure 12.

Line Transient

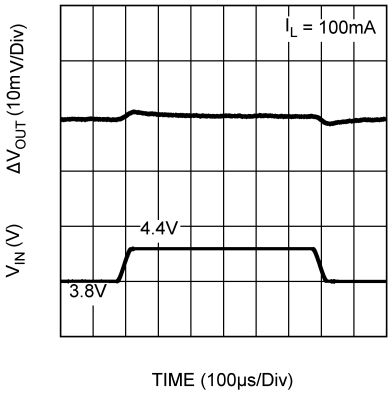


Figure 13.

Enable Startup Time, (I_L= 1mA, V_{OUT} = 2.8V)

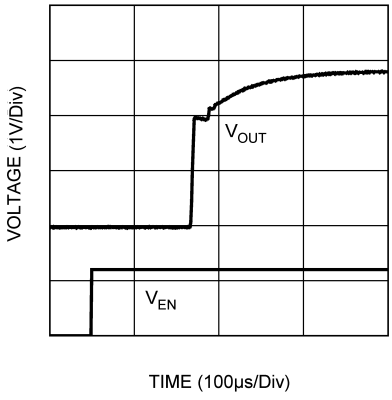


Figure 14.

Typical Performance Characteristics. (continued)

Unless otherwise specified, $C_{IN} = C_{OUT} = 0.47\mu F$, $V_{IN} = V_{OUT(NOM)} + 1.0V$, $V_{EN} = 1.2V$, $I_{OUT} = 1mA$, $T_A = 25°C$.

Enable Startup Time, (I_L= 100mA, V_{OUT} = 2.8V)

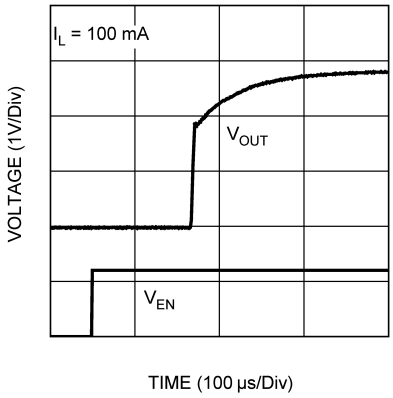


Figure 15.

Enable Startup Time, (I_L= 1mA, V_{OUT} = 2.8V)

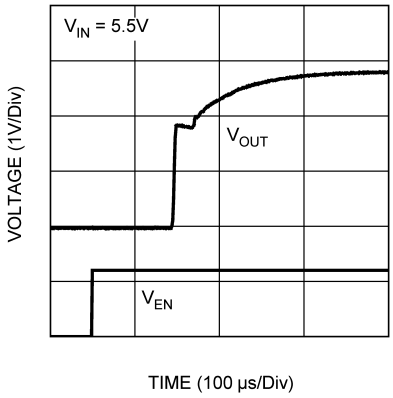


Figure 16.

Enable Startup Time, (I_L= 100mA, V_{OUT} = 2.8V)

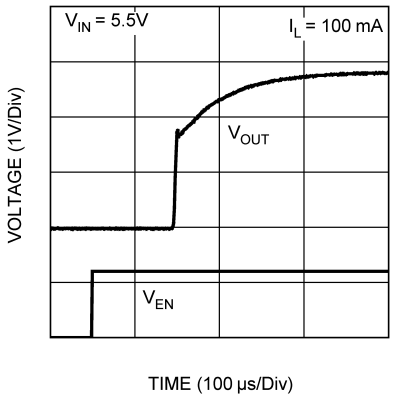


Figure 17.

Dropout Over Temperature (100mA)

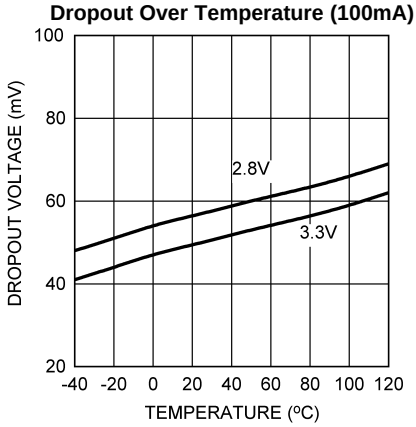


Figure 18.

APPLICATION HINTS

POWER DISSIPATION AND DEVICE OPERATION

The permissible power dissipation for any package is a measure of the capability of the device to pass heat from the power source, the junctions of the IC, to the ultimate heat sink, the ambient environment. Thus the power dissipation is dependent on the ambient temperature and the thermal resistance across the various interfaces between the die and ambient air. As stated in Operating Ratings, the allowable power dissipation for the device in a given package can be calculated using the equation:

$$P_D = \frac{(T_{JMAX} - T_A)}{\theta_{JA}} \quad (1)$$

The actual power dissipation across the device can be represented by the following equation:

$$P_D = (V_{IN} – V_{OUT}) \times I_{OUT} \quad (2)$$

This establishes the relationship between the power dissipation allowed due to thermal consideration, the voltage drop across the device, and the continuous current capability of the device. These two equations should be used to determine the optimum operating conditions for the device in the application.

EXTERNAL CAPACITORS

Like any low-dropout regulator, the LP5900 requires external capacitors for regulator stability. The LP5900 is specifically designed for portable applications requiring minimum board space and smallest components. These capacitors must be correctly selected for good performance.

INPUT CAPACITOR

An input capacitor is required for stability. The input capacitor should be at least equal to or greater than the output capacitor. It is recommended that a 0.47 µF capacitor be connected between the LP5900 input pin and ground.

This capacitor must be located a distance of not more than 1 cm from the input pin and returned to a clean analogue ground. Any good quality ceramic, tantalum, or film capacitor may be used at the input.

Important: To ensure stable operation it is essential that good PCB practices are employed to minimize ground impedance and keep input inductance low. If these conditions cannot be met, or if long leads are to be used to connect the battery or other power source to the LP5900, then it is recommended to increase the input capacitor to at least 2.2 µF. Also, tantalum capacitors can suffer catastrophic failures due to surge current when connected to a low-impedance source of power (like a battery or a very large capacitor). If a tantalum capacitor is used at the input, it must be ensured by the manufacturer to have a surge current rating sufficient for the application. There are no requirements for the ESR (Equivalent Series Resistance) on the input capacitor, but tolerance and temperature coefficient must be considered when selecting the capacitor to ensure the capacitance will remain 0.47 µF ±30% over the entire operating temperature range.

OUTPUT CAPACITOR

The LP5900 is designed specifically to work with very small ceramic output capacitors. A ceramic capacitor (dielectric types X5R or X7R) in the 0.47 µF to 10 µF range, and with ESR between 5 mΩ to 500 mΩ, is suitable in the LP5900 application circuit. For this device the output capacitor should be connected between the V_{OUT} pin and a good ground connection and should be mounted within 1 cm of the device.

It may also be possible to use tantalum or film capacitors at the device output, V_{OUT}, but these are not as attractive for reasons of size and cost (see the CAPACITOR CHARACTERISTICS section below).

The output capacitor must meet the requirement for the minimum value of capacitance and have an ESR value that is within the range 5 mΩ to 500 mΩ for stability.

CAPACITOR CHARACTERISTICS

The LP5900 is designed to work with ceramic capacitors on the input and output to take advantage of the benefits they offer. For capacitance values in the range of 0.47 µF to 4.7 µF, ceramic capacitors are the smallest, least expensive and have the lowest ESR values, thus making them best for eliminating high frequency noise. The ESR of a typical 0.47 µF ceramic capacitor is in the range of 20 mΩ to 40 mΩ, which easily meets the ESR requirement for stability for the LP5900.

The temperature performance of ceramic capacitors varies by type and manufacturer. Most large value ceramic capacitors (≥ 2.2 µF) are manufactured with Z5U or Y5V temperature characteristics, which results in the capacitance dropping by more than 50% as the temperature goes from 25°C to 85°C.

A better choice for temperature coefficient in a ceramic capacitor is X7R. This type of capacitor is the most stable and holds the capacitance within ±15% over the temperature range. Tantalum capacitors are less desirable than ceramic for use as output capacitors because they are more expensive when comparing equivalent capacitance and voltage ratings in the 0.47 µF to 4.7 µF range.

Another important consideration is that tantalum capacitors have higher ESR values than equivalent size ceramics. This means that while it may be possible to find a tantalum capacitor with an ESR value within the stable range, it would have to be larger in capacitance (which means bigger and more costly) than a ceramic capacitor with the same ESR value. It should also be noted that the ESR of a typical tantalum will increase about 2:1 as the temperature goes from 25°C down to −40°C, so some guard band must be allowed.

NO-LOAD STABILITY

The LP5900 will remain stable and in regulation with no external load.

ENABLE CONTROL

The LP5900 may be switched ON or OFF by a logic input at the ENABLE pin. A high voltage at this pin will turn the device on. When the enable pin is low, the regulator output is off and the device typically consumes 3nA. However if the application does not require the shutdown feature, the V_{EN} pin can be tied to V_{IN} to keep the regulator output permanently on. In this case the supply voltage must be fully established 500 µs or less to ensure correct operation of the startup circuit. Failure to comply with this condition may cause a delayed startup time of several seconds.

A 1MΩ pulldown resistor ties the V_{EN} input to ground, this ensures that the device will remain off when the enable pin is left open circuit. To ensure proper operation, the signal source used to drive the V_{EN} input must be able to swing above and below the specified turn-on/off voltage thresholds listed in the Electrical Characteristics section under V_{IL} and V_{IH}.

DSBGA MOUNTING

The DSBGA package requires specific mounting techniques, which are detailed in Texas Instruments Application Note AN-1112, SNVS009.

For best results during assembly, alignment ordinals on the PC board may be used to facilitate placement of the micro SMD device.

DSBGA LIGHT SENSITIVITY

Exposing the DSBGA device to direct light may cause incorrect operation of the device. Light sources such as halogen lamps can affect electrical performance if they are situated in proximity to the device.

Light with wavelengths in the red and infra-red part of the spectrum has the most detrimental effect; thus, the fluorescent lighting used inside most buildings has very little effect on performance.

REVISION HISTORY

Changes from Revision N (April 2013) to Revision O	Page
• Changed layout of National Data Sheet to TI format	10

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP5900SD-1.5	NRND	WSON	NGF	6	1000	TBD	Call TI	Call TI	-40 to 125	L15	
LP5900SD-1.5/NOPB	ACTIVE	WSON	NGF	6	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L15	Samples
LP5900SD-1.8/NOPB	ACTIVE	WSON	NGF	6	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L17	Samples
LP5900SD-2.0/NOPB	ACTIVE	WSON	NGF	6	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L18	Samples
LP5900SD-2.2/NOPB	ACTIVE	WSON	NGF	6	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L19	Samples
LP5900SD-2.5	NRND	WSON	NGF	6	1000	TBD	Call TI	Call TI	-40 to 125	L13	
LP5900SD-2.5/NOPB	ACTIVE	WSON	NGF	6	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L13	Samples
LP5900SD-2.7/NOPB	ACTIVE	WSON	NGF	6	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L14	Samples
LP5900SD-2.8/NOPB	ACTIVE	WSON	NGF	6	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L12	Samples
LP5900SD-3.0/NOPB	ACTIVE	WSON	NGF	6	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L20	Samples
LP5900SD-3.3/NOPB	ACTIVE	WSON	NGF	6	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L16	Samples
LP5900SDX-1.5/NOPB	ACTIVE	WSON	NGF	6	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L15	Samples
LP5900SDX-1.8	NRND	WSON	NGF	6	4500	TBD	Call TI	Call TI	-40 to 125	L17	
LP5900SDX-1.8/NOPB	ACTIVE	WSON	NGF	6	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L17	Samples
LP5900SDX-2.0/NOPB	ACTIVE	WSON	NGF	6	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L18	Samples
LP5900SDX-2.2/NOPB	ACTIVE	WSON	NGF	6	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L19	Samples
LP5900SDX-2.5/NOPB	ACTIVE	WSON	NGF	6	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L13	Samples
LP5900SDX-2.7/NOPB	ACTIVE	WSON	NGF	6	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L14	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP5900SDX-2.8/NOPB	ACTIVE	WSON	NGF	6	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L12	Samples
LP5900SDX-3.0/NOPB	ACTIVE	WSON	NGF	6	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L20	Samples
LP5900SDX-3.3/NOPB	ACTIVE	WSON	NGF	6	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L16	Samples
LP5900TL-1.5/NOPB	ACTIVE	DSBGA	YZR	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125		Samples
LP5900TL-1.575/NOPB	ACTIVE	DSBGA	YZR	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125		Samples
LP5900TL-1.8/NOPB	ACTIVE	DSBGA	YZR	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125		Samples
LP5900TL-1.9/NOPB	ACTIVE	DSBGA	YZR	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125		Samples
LP5900TL-2.0/NOPB	ACTIVE	DSBGA	YZR	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125		Samples
LP5900TL-2.1/NOPB	ACTIVE	DSBGA	YZR	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125		Samples
LP5900TL-2.2/NOPB	ACTIVE	DSBGA	YZR	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125		Samples
LP5900TL-2.3/NOPB	ACTIVE	DSBGA	YZR	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125		Samples
LP5900TL-2.5/NOPB	ACTIVE	DSBGA	YZR	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125		Samples
LP5900TL-2.6/NOPB	ACTIVE	DSBGA	YZR	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125		Samples
LP5900TL-2.65/NOPB	ACTIVE	DSBGA	YZR	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125		Samples
LP5900TL-2.7/NOPB	ACTIVE	DSBGA	YZR	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125		Samples
LP5900TL-2.75/NOPB	ACTIVE	DSBGA	YZR	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125		Samples
LP5900TL-2.8/NOPB	ACTIVE	DSBGA	YZR	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125		Samples
LP5900TL-2.85/NOPB	ACTIVE	DSBGA	YZR	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125		Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP5900TL-3.0/NOPB	ACTIVE	DSBGA	YZR	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125		Samples
LP5900TL-3.3/NOPB	ACTIVE	DSBGA	YZR	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125		Samples
LP5900TL-4.5/NOPB	ACTIVE	DSBGA	YZR	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125		Samples
LP5900TLX-1.5/NOPB	ACTIVE	DSBGA	YZR	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125		Samples
LP5900TLX-1.575/NOPB	ACTIVE	DSBGA	YZR	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125		Samples
LP5900TLX-1.8/NOPB	ACTIVE	DSBGA	YZR	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125		Samples
LP5900TLX-1.9/NOPB	ACTIVE	DSBGA	YZR	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125		Samples
LP5900TLX-2.0/NOPB	ACTIVE	DSBGA	YZR	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125		Samples
LP5900TLX-2.1/NOPB	ACTIVE	DSBGA	YZR	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125		Samples
LP5900TLX-2.2/NOPB	ACTIVE	DSBGA	YZR	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125		Samples
LP5900TLX-2.3/NOPB	ACTIVE	DSBGA	YZR	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125		Samples
LP5900TLX-2.5/NOPB	ACTIVE	DSBGA	YZR	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125		Samples
LP5900TLX-2.6/NOPB	ACTIVE	DSBGA	YZR	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125		Samples
LP5900TLX-2.65/NOPB	ACTIVE	DSBGA	YZR	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125		Samples
LP5900TLX-2.7/NOPB	ACTIVE	DSBGA	YZR	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125		Samples
LP5900TLX-2.75/NOPB	ACTIVE	DSBGA	YZR	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125		Samples
LP5900TLX-2.8/NOPB	ACTIVE	DSBGA	YZR	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125		Samples
LP5900TLX-2.85/NOPB	ACTIVE	DSBGA	YZR	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125		Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP5900TLX-3.0/NOPB	ACTIVE	DSBGA	YZR	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125		Samples
LP5900TLX-3.3/NOPB	ACTIVE	DSBGA	YZR	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125		Samples
LP5900TLX-4.5/NOPB	ACTIVE	DSBGA	YZR	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125		Samples
LP5900XR-1.8/NOPB	ACTIVE	DSBGA	YPF	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125		Samples
LP5900XR-2.8/NOPB	ACTIVE	DSBGA	YPF	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125		Samples
LP5900XRX-1.8/NOPB	ACTIVE	DSBGA	YPF	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125		Samples
LP5900XRX-2.8/NOPB	ACTIVE	DSBGA	YPF	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

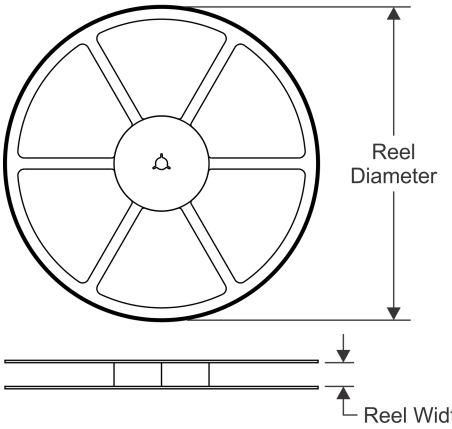
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

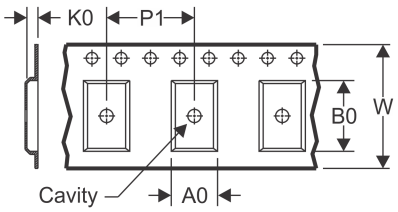
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

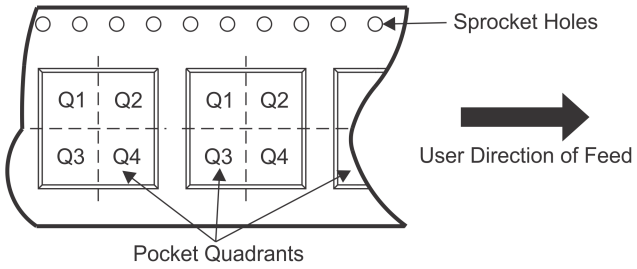


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

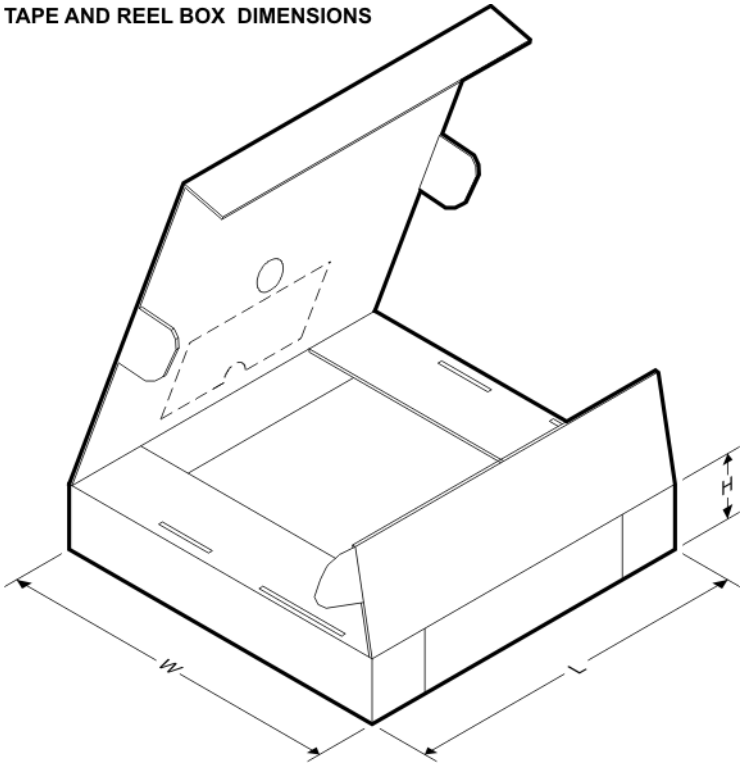


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP5900SD-1.5	WSON	NGF	6	1000	178.0	12.4	2.8	2.5	1.0	8.0	12.0	Q1
LP5900SD-1.5/NOPB	WSON	NGF	6	1000	178.0	12.4	2.8	2.5	1.0	8.0	12.0	Q1
LP5900SD-1.8/NOPB	WSON	NGF	6	1000	178.0	12.4	2.8	2.5	1.0	8.0	12.0	Q1
LP5900SD-2.0/NOPB	WSON	NGF	6	1000	178.0	12.4	2.8	2.5	1.0	8.0	12.0	Q1
LP5900SD-2.2/NOPB	WSON	NGF	6	1000	178.0	12.4	2.8	2.5	1.0	8.0	12.0	Q1
LP5900SD-2.5	WSON	NGF	6	1000	178.0	12.4	2.8	2.5	1.0	8.0	12.0	Q1
LP5900SD-2.5/NOPB	WSON	NGF	6	1000	178.0	12.4	2.8	2.5	1.0	8.0	12.0	Q1
LP5900SD-2.7/NOPB	WSON	NGF	6	1000	178.0	12.4	2.8	2.5	1.0	8.0	12.0	Q1
LP5900SD-2.8/NOPB	WSON	NGF	6	1000	178.0	12.4	2.8	2.5	1.0	8.0	12.0	Q1
LP5900SD-3.0/NOPB	WSON	NGF	6	1000	178.0	12.4	2.8	2.5	1.0	8.0	12.0	Q1
LP5900SD-3.3/NOPB	WSON	NGF	6	1000	178.0	12.4	2.8	2.5	1.0	8.0	12.0	Q1
LP5900SDX-1.5/NOPB	WSON	NGF	6	4500	330.0	12.4	2.8	2.5	1.0	8.0	12.0	Q1
LP5900SDX-1.8	WSON	NGF	6	4500	330.0	12.4	2.8	2.5	1.0	8.0	12.0	Q1
LP5900SDX-1.8/NOPB	WSON	NGF	6	4500	330.0	12.4	2.8	2.5	1.0	8.0	12.0	Q1
LP5900SDX-2.0/NOPB	WSON	NGF	6	4500	330.0	12.4	2.8	2.5	1.0	8.0	12.0	Q1
LP5900SDX-2.2/NOPB	WSON	NGF	6	4500	330.0	12.4	2.8	2.5	1.0	8.0	12.0	Q1
LP5900SDX-2.5/NOPB	WSON	NGF	6	4500	330.0	12.4	2.8	2.5	1.0	8.0	12.0	Q1
LP5900SDX-2.7/NOPB	WSON	NGF	6	4500	330.0	12.4	2.8	2.5	1.0	8.0	12.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP5900SDX-2.8/NOPB	WSON	NGF	6	4500	330.0	12.4	2.8	2.5	1.0	8.0	12.0	Q1
LP5900SDX-3.0/NOPB	WSON	NGF	6	4500	330.0	12.4	2.8	2.5	1.0	8.0	12.0	Q1
LP5900SDX-3.3/NOPB	WSON	NGF	6	4500	330.0	12.4	2.8	2.5	1.0	8.0	12.0	Q1
LP5900TL-1.5/NOPB	DSBGA	YZR	4	250	178.0	8.4	1.15	1.16	0.79	4.0	8.0	Q1
LP5900TL-1.575/NOPB	DSBGA	YZR	4	250	178.0	8.4	1.15	1.16	0.79	4.0	8.0	Q1
LP5900TL-1.8/NOPB	DSBGA	YZR	4	250	178.0	8.4	1.15	1.16	0.79	4.0	8.0	Q1
LP5900TL-1.9/NOPB	DSBGA	YZR	4	250	178.0	8.4	1.15	1.16	0.79	4.0	8.0	Q1
LP5900TL-2.0/NOPB	DSBGA	YZR	4	250	178.0	8.4	1.15	1.16	0.79	4.0	8.0	Q1
LP5900TL-2.1/NOPB	DSBGA	YZR	4	250	178.0	8.4	1.15	1.16	0.79	4.0	8.0	Q1
LP5900TL-2.2/NOPB	DSBGA	YZR	4	250	178.0	8.4	1.15	1.16	0.79	4.0	8.0	Q1
LP5900TL-2.3/NOPB	DSBGA	YZR	4	250	178.0	8.4	1.15	1.16	0.79	4.0	8.0	Q1
LP5900TL-2.5/NOPB	DSBGA	YZR	4	250	178.0	8.4	1.15	1.16	0.79	4.0	8.0	Q1
LP5900TL-2.6/NOPB	DSBGA	YZR	4	250	178.0	8.4	1.15	1.16	0.79	4.0	8.0	Q1
LP5900TL-2.65/NOPB	DSBGA	YZR	4	250	178.0	8.4	1.15	1.16	0.79	4.0	8.0	Q1
LP5900TL-2.7/NOPB	DSBGA	YZR	4	250	178.0	8.4	1.15	1.16	0.79	4.0	8.0	Q1
LP5900TL-2.75/NOPB	DSBGA	YZR	4	250	178.0	8.4	1.15	1.16	0.79	4.0	8.0	Q1
LP5900TL-2.8/NOPB	DSBGA	YZR	4	250	178.0	8.4	1.15	1.16	0.79	4.0	8.0	Q1
LP5900TL-2.85/NOPB	DSBGA	YZR	4	250	178.0	8.4	1.15	1.16	0.79	4.0	8.0	Q1
LP5900TL-3.0/NOPB	DSBGA	YZR	4	250	178.0	8.4	1.15	1.16	0.79	4.0	8.0	Q1
LP5900TL-3.3/NOPB	DSBGA	YZR	4	250	178.0	8.4	1.15	1.16	0.79	4.0	8.0	Q1
LP5900TL-4.5/NOPB	DSBGA	YZR	4	250	178.0	8.4	1.15	1.16	0.79	4.0	8.0	Q1
LP5900TLX-1.5/NOPB	DSBGA	YZR	4	3000	178.0	8.4	1.15	1.16	0.79	4.0	8.0	Q1
LP5900TLX-1.575/NOPB	DSBGA	YZR	4	3000	178.0	8.4	1.15	1.16	0.79	4.0	8.0	Q1
LP5900TLX-1.8/NOPB	DSBGA	YZR	4	3000	178.0	8.4	1.15	1.16	0.79	4.0	8.0	Q1
LP5900TLX-1.9/NOPB	DSBGA	YZR	4	3000	178.0	8.4	1.15	1.16	0.79	4.0	8.0	Q1
LP5900TLX-2.0/NOPB	DSBGA	YZR	4	3000	178.0	8.4	1.15	1.16	0.79	4.0	8.0	Q1
LP5900TLX-2.1/NOPB	DSBGA	YZR	4	3000	178.0	8.4	1.15	1.16	0.79	4.0	8.0	Q1
LP5900TLX-2.2/NOPB	DSBGA	YZR	4	3000	178.0	8.4	1.15	1.16	0.79	4.0	8.0	Q1
LP5900TLX-2.3/NOPB	DSBGA	YZR	4	3000	178.0	8.4	1.15	1.16	0.79	4.0	8.0	Q1
LP5900TLX-2.5/NOPB	DSBGA	YZR	4	3000	178.0	8.4	1.15	1.16	0.79	4.0	8.0	Q1
LP5900TLX-2.6/NOPB	DSBGA	YZR	4	3000	178.0	8.4	1.15	1.16	0.79	4.0	8.0	Q1
LP5900TLX-2.65/NOPB	DSBGA	YZR	4	3000	178.0	8.4	1.15	1.16	0.79	4.0	8.0	Q1
LP5900TLX-2.7/NOPB	DSBGA	YZR	4	3000	178.0	8.4	1.15	1.16	0.79	4.0	8.0	Q1
LP5900TLX-2.75/NOPB	DSBGA	YZR	4	3000	178.0	8.4	1.15	1.16	0.79	4.0	8.0	Q1
LP5900TLX-2.8/NOPB	DSBGA	YZR	4	3000	178.0	8.4	1.15	1.16	0.79	4.0	8.0	Q1
LP5900TLX-2.85/NOPB	DSBGA	YZR	4	3000	178.0	8.4	1.15	1.16	0.79	4.0	8.0	Q1
LP5900TLX-3.0/NOPB	DSBGA	YZR	4	3000	178.0	8.4	1.15	1.16	0.79	4.0	8.0	Q1
LP5900TLX-3.3/NOPB	DSBGA	YZR	4	3000	178.0	8.4	1.15	1.16	0.79	4.0	8.0	Q1
LP5900TLX-4.5/NOPB	DSBGA	YZR	4	3000	178.0	8.4	1.15	1.16	0.79	4.0	8.0	Q1
LP5900XR-1.8/NOPB	DSBGA	YPF	4	250	178.0	8.4	1.16	1.2	0.4	4.0	8.0	Q1
LP5900XR-2.8/NOPB	DSBGA	YPF	4	250	178.0	8.4	1.16	1.2	0.4	4.0	8.0	Q1
LP5900XRX-1.8/NOPB	DSBGA	YPF	4	3000	178.0	8.4	1.16	1.2	0.4	4.0	8.0	Q1
LP5900XRX-2.8/NOPB	DSBGA	YPF	4	3000	178.0	8.4	1.16	1.2	0.4	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS

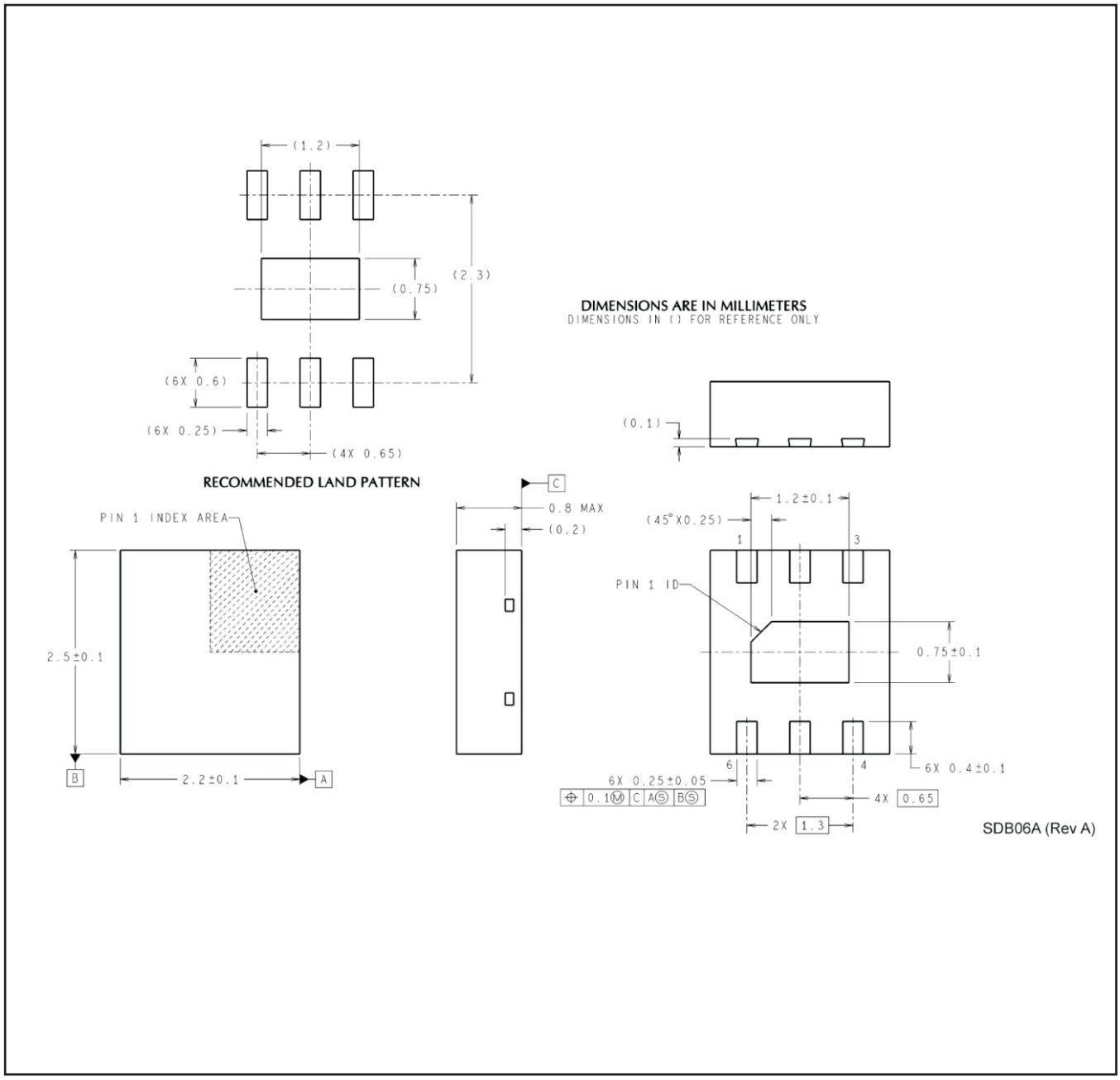


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP5900SD-1.5	WSON	NGF	6	1000	210.0	185.0	35.0
LP5900SD-1.5/NOPB	WSON	NGF	6	1000	210.0	185.0	35.0
LP5900SD-1.8/NOPB	WSON	NGF	6	1000	210.0	185.0	35.0
LP5900SD-2.0/NOPB	WSON	NGF	6	1000	210.0	185.0	35.0
LP5900SD-2.2/NOPB	WSON	NGF	6	1000	210.0	185.0	35.0
LP5900SD-2.5	WSON	NGF	6	1000	210.0	185.0	35.0
LP5900SD-2.5/NOPB	WSON	NGF	6	1000	210.0	185.0	35.0
LP5900SD-2.7/NOPB	WSON	NGF	6	1000	210.0	185.0	35.0
LP5900SD-2.8/NOPB	WSON	NGF	6	1000	210.0	185.0	35.0
LP5900SD-3.0/NOPB	WSON	NGF	6	1000	210.0	185.0	35.0
LP5900SD-3.3/NOPB	WSON	NGF	6	1000	210.0	185.0	35.0
LP5900SDX-1.5/NOPB	WSON	NGF	6	4500	367.0	367.0	35.0
LP5900SDX-1.8	WSON	NGF	6	4500	367.0	367.0	35.0
LP5900SDX-1.8/NOPB	WSON	NGF	6	4500	367.0	367.0	35.0
LP5900SDX-2.0/NOPB	WSON	NGF	6	4500	367.0	367.0	35.0
LP5900SDX-2.2/NOPB	WSON	NGF	6	4500	367.0	367.0	35.0
LP5900SDX-2.5/NOPB	WSON	NGF	6	4500	367.0	367.0	35.0
LP5900SDX-2.7/NOPB	WSON	NGF	6	4500	367.0	367.0	35.0
LP5900SDX-2.8/NOPB	WSON	NGF	6	4500	367.0	367.0	35.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP5900SDX-3.0/NOPB	WSON	NGF	6	4500	367.0	367.0	35.0
LP5900SDX-3.3/NOPB	WSON	NGF	6	4500	367.0	367.0	35.0
LP5900TL-1.5/NOPB	DSBGA	YZR	4	250	210.0	185.0	35.0
LP5900TL-1.575/NOPB	DSBGA	YZR	4	250	210.0	185.0	35.0
LP5900TL-1.8/NOPB	DSBGA	YZR	4	250	210.0	185.0	35.0
LP5900TL-1.9/NOPB	DSBGA	YZR	4	250	210.0	185.0	35.0
LP5900TL-2.0/NOPB	DSBGA	YZR	4	250	210.0	185.0	35.0
LP5900TL-2.1/NOPB	DSBGA	YZR	4	250	210.0	185.0	35.0
LP5900TL-2.2/NOPB	DSBGA	YZR	4	250	210.0	185.0	35.0
LP5900TL-2.3/NOPB	DSBGA	YZR	4	250	210.0	185.0	35.0
LP5900TL-2.5/NOPB	DSBGA	YZR	4	250	210.0	185.0	35.0
LP5900TL-2.6/NOPB	DSBGA	YZR	4	250	210.0	185.0	35.0
LP5900TL-2.65/NOPB	DSBGA	YZR	4	250	210.0	185.0	35.0
LP5900TL-2.7/NOPB	DSBGA	YZR	4	250	210.0	185.0	35.0
LP5900TL-2.75/NOPB	DSBGA	YZR	4	250	210.0	185.0	35.0
LP5900TL-2.8/NOPB	DSBGA	YZR	4	250	210.0	185.0	35.0
LP5900TL-2.85/NOPB	DSBGA	YZR	4	250	210.0	185.0	35.0
LP5900TL-3.0/NOPB	DSBGA	YZR	4	250	210.0	185.0	35.0
LP5900TL-3.3/NOPB	DSBGA	YZR	4	250	210.0	185.0	35.0
LP5900TL-4.5/NOPB	DSBGA	YZR	4	250	210.0	185.0	35.0
LP5900TLX-1.5/NOPB	DSBGA	YZR	4	3000	210.0	185.0	35.0
LP5900TLX-1.575/NOPB	DSBGA	YZR	4	3000	210.0	185.0	35.0
LP5900TLX-1.8/NOPB	DSBGA	YZR	4	3000	210.0	185.0	35.0
LP5900TLX-1.9/NOPB	DSBGA	YZR	4	3000	210.0	185.0	35.0
LP5900TLX-2.0/NOPB	DSBGA	YZR	4	3000	210.0	185.0	35.0
LP5900TLX-2.1/NOPB	DSBGA	YZR	4	3000	210.0	185.0	35.0
LP5900TLX-2.2/NOPB	DSBGA	YZR	4	3000	210.0	185.0	35.0
LP5900TLX-2.3/NOPB	DSBGA	YZR	4	3000	210.0	185.0	35.0
LP5900TLX-2.5/NOPB	DSBGA	YZR	4	3000	210.0	185.0	35.0
LP5900TLX-2.6/NOPB	DSBGA	YZR	4	3000	210.0	185.0	35.0
LP5900TLX-2.65/NOPB	DSBGA	YZR	4	3000	210.0	185.0	35.0
LP5900TLX-2.7/NOPB	DSBGA	YZR	4	3000	210.0	185.0	35.0
LP5900TLX-2.75/NOPB	DSBGA	YZR	4	3000	210.0	185.0	35.0
LP5900TLX-2.8/NOPB	DSBGA	YZR	4	3000	210.0	185.0	35.0
LP5900TLX-2.85/NOPB	DSBGA	YZR	4	3000	210.0	185.0	35.0
LP5900TLX-3.0/NOPB	DSBGA	YZR	4	3000	210.0	185.0	35.0
LP5900TLX-3.3/NOPB	DSBGA	YZR	4	3000	210.0	185.0	35.0
LP5900TLX-4.5/NOPB	DSBGA	YZR	4	3000	210.0	185.0	35.0
LP5900XR-1.8/NOPB	DSBGA	YPF	4	250	210.0	185.0	35.0
LP5900XR-2.8/NOPB	DSBGA	YPF	4	250	210.0	185.0	35.0
LP5900XRX-1.8/NOPB	DSBGA	YPF	4	3000	210.0	185.0	35.0
LP5900XRX-2.8/NOPB	DSBGA	YPF	4	3000	210.0	185.0	35.0

NGF0006A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(2.3)
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RECOMMENDED LAND PATTERN
DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY
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2.2±0.1
B
A
C
0.8 MAX
(0.2)
1.2±0.1
(45°X0.25)
1
3
PIN 1 ID
0.75±0.1
6
4
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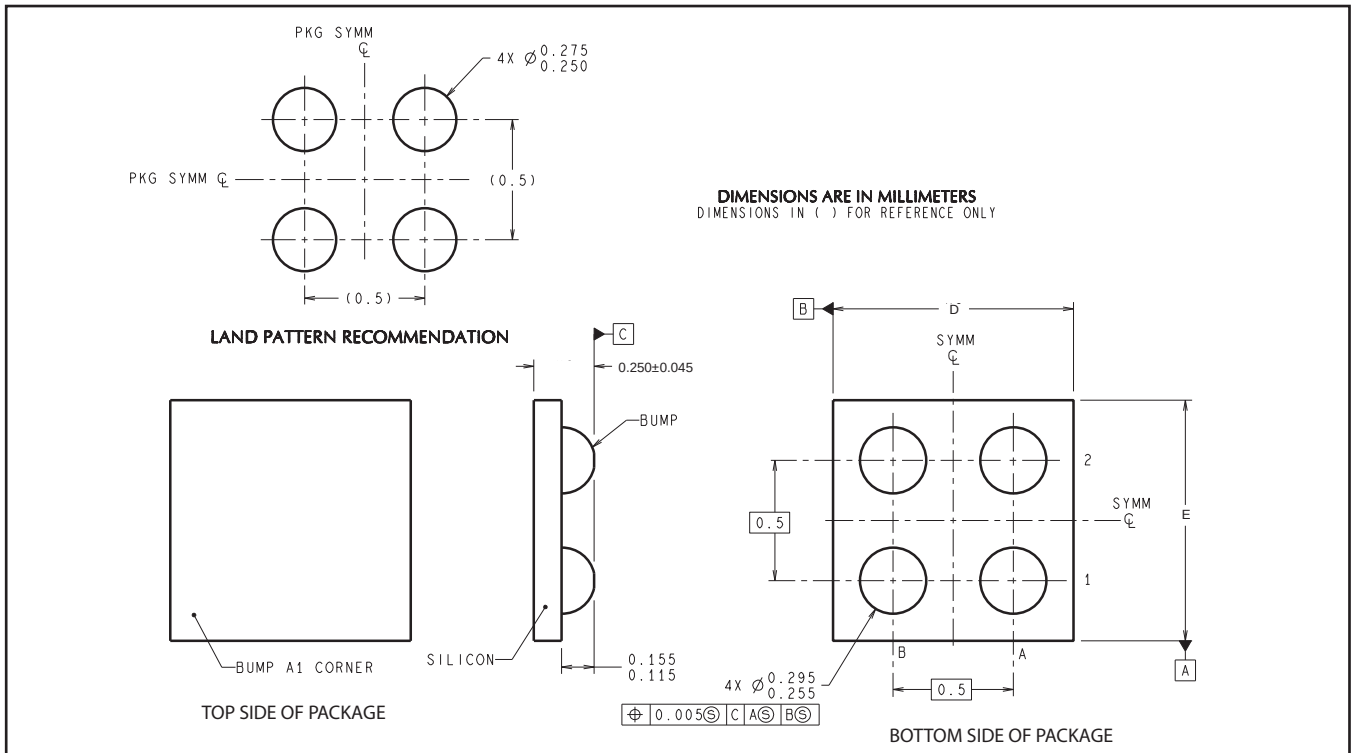
4X 0.65
2X 1.3
SDB06A (Rev A)

YPF0004



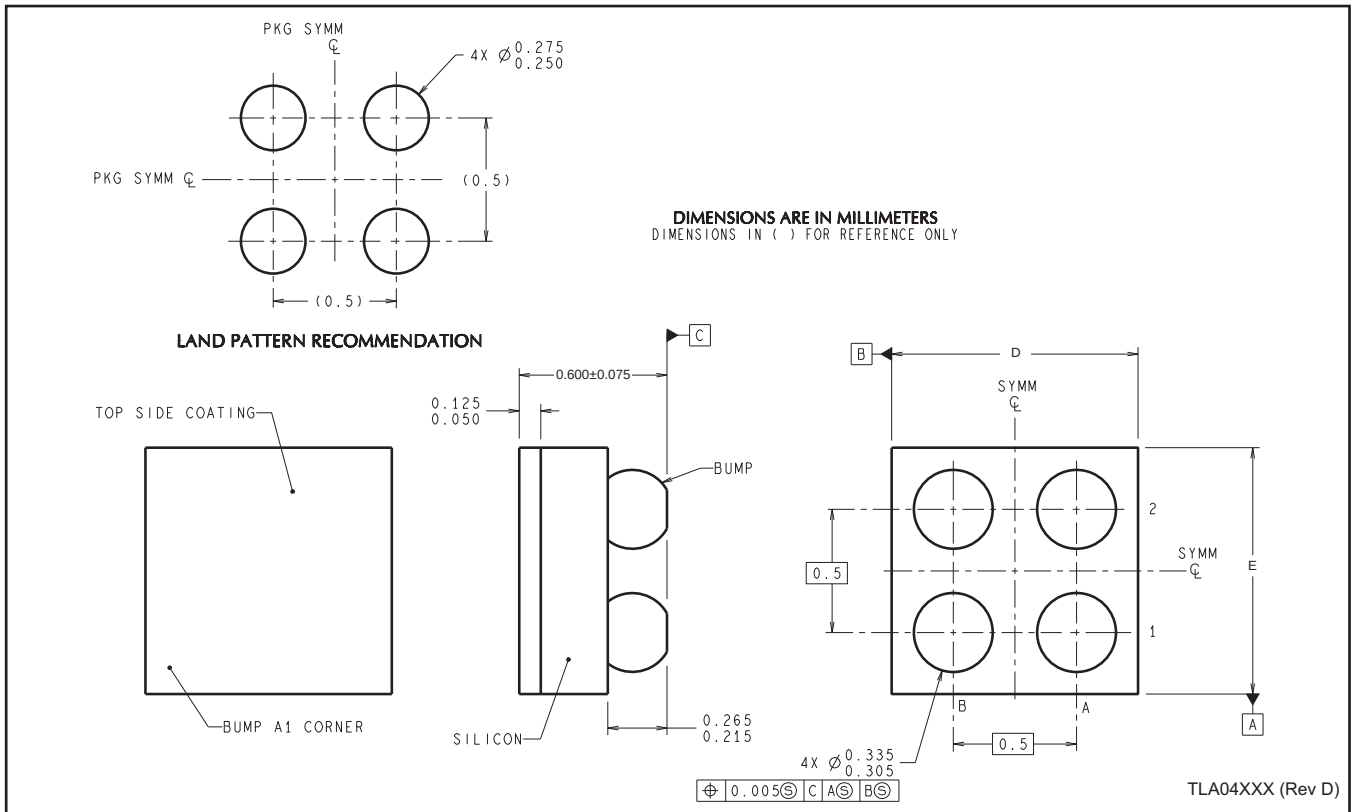
D: Max = 1.108 mm, Min =1.047 mm

E: Max = 1.083 mm, Min =1.022 mm

4215204/A 12/12

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

YZR0004



D: Max = 1.108 mm, Min =1.047 mm

E: Max = 1.083 mm, Min =1.022 mm

4215042/A 12/12

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

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