LP3878-ADJ Micropower 800mA Low Noise "Ceramic Stable" Adjustable Voltage Regulator for 1V to 5V Applications

Check for Samples: LP3878-ADJ

FEATURES

- **1.0V to 5.5V Output**
- **Designed for Use with Low ESR Ceramic Capacitors**
- **Very Low Output Noise**
- **8 Lead SO PowerPAD and WSON Surface Mount Package**
- **<10 µA Quiescent Current in Shutdown**
- **Low Ground Pin Current at all Loads**
- **Over-Temperature/Oover-Current Protection**
- **-40°C to +125°C Operating Junction Temperature Range**

APPLICATIONS

- **ASIC Power Supplies In:**
  - **Desktops, Notebooks and Graphic Cards**
  - **Set Top Boxes, Printers and Copiers**
- **DSP and FPGA Power Supplies**
- **SMPS Post-Regulator**
- **Medical Instrumentation**

DESCRIPTION

The LP3878-ADJ is an 800 mA adjustable output voltage regulator designed to provide high performance and low noise in applications requiring output voltages as low as 1.0V.

Using an optimized VIP™ (Vertically Integrated PNP) process, the LP3878-ADJ delivers superior performance:

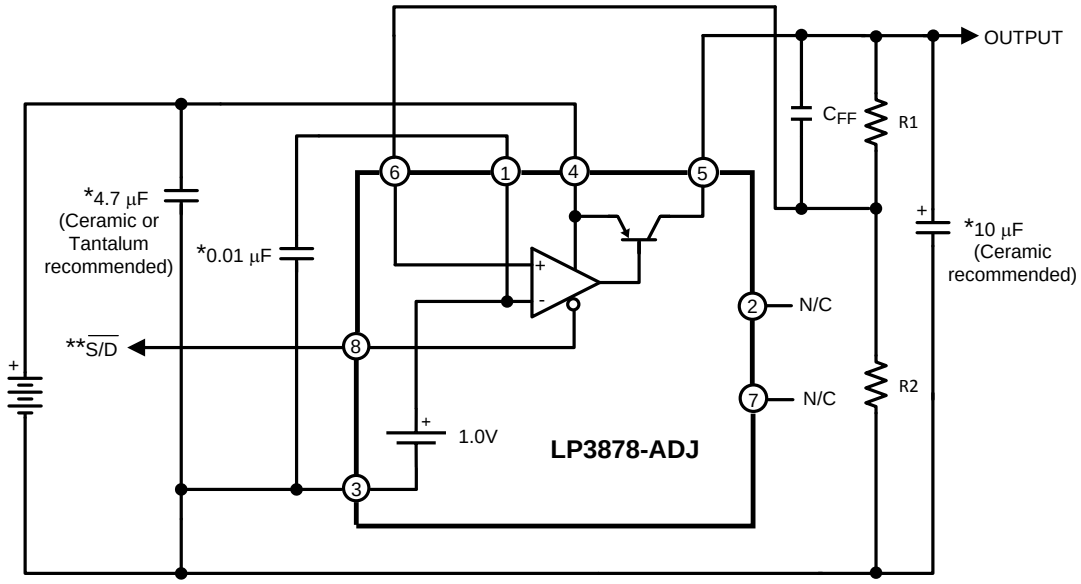
Ground Pin Current: Typically 5.5 mA @ 800 mA load, and 180 µA @ 100 µA load.

Low Power Shutdown: The LP3878-ADJ draws less than 10 µA quiescent current when shutdown pin is pulled low.

Precision Output: Ensured output voltage accuracy is 1% at room temperature.

Low Noise: Broadband output noise is only 18 µV (typical) with 10 nF bypass capacitor.

Basic Application Circuit



*Capacitance values shown are minimum required to assure stability. Larger output capacitor provides improved dynamic response. Output capacitor must meet ESR requirements (see Application Information).
**The Shutdown pin must be actively terminated (see Application Information). Tie to INPUT (Pin 4) if not used.

Connection Diagram

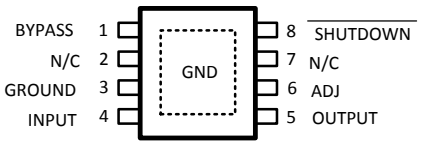


Figure 1. 8 Lead SO PowerPAD Package (DDA) - Top View
See Package Number DDA0008A

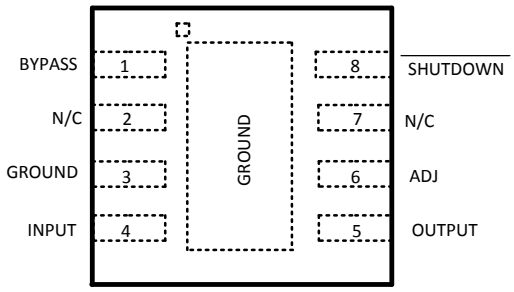


Figure 2. 8 Lead WSON Surface Mount Package (NGT)
Top View
See Package Number NGT0008A

PIN DESCRIPTIONS

Pin	Name	Function
1	BYPASS	The capacitor connected between BYPASS and GROUND lowers output noise voltage level and is required for loop stability.
2	N/C	DO NOT CONNECT. This pin is used for post package test and must be left floating.
3	GROUND	Device ground.
4	INPUT	Input source voltage.
5	OUTPUT	Regulated output voltage.
6	ADJ	Provides feedback to error amplifier from the resistive divider that sets the output voltage.
7	N/C	No internal connection.
8	SHUTDOWN	Output is enabled above turn-on threshold voltage. Pull down to turn off regulator output.
SO PowerPAD, WSON DAP	SUBSTRATE GROUND	The exposed die attach pad should be connected to a thermal pad at ground potential. For additional information on using TI's Non Pull Back WSON package, please refer to WSON application note AN-1187

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)(2)

Storage Temperature Range	−65°C to +150°C
Operating Junction Temperature Range	-40°C to +125°C
Lead Temperature (Soldering, 5 seconds)	260°C
ESD Rating(3)	2 kV
Shutdown Pin	1kV
Power Dissipation(4)	Internally Limited
Input Supply Voltage (Survival)	−0.3V to +16V
Input Supply Voltage (Typical Operating)	2.5V to +16V
ADJ Pin	−0.3V to +6V
Output Voltage (Survival)(5)	−0.3V to +6V
I_{OUT} (Survival)	Short Circuit Protected
Input-Output Voltage (Survival)(6)	−0.3V to +16V

(1) Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Electrical specifications do not apply when operating the device outside of its rated operating conditions.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.
(3) ESD testing was performed using Human Body Model, a 100 pF capacitor discharged through a 1.5 kΩ resistor.
(4) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J(MAX), the junction-to-ambient thermal resistance, θ_{J-A}, and the ambient temperature, T_A. The maximum allowable power dissipation at any ambient temperature is calculated using:

$$P(MAX) = \frac{T_J(MAX) - T_A}{\theta_{J-A}}$$

The value of θ_{J-A} for the WSON (NGT) and SO PowerPAD (DDA) packages are specifically dependent on PCB trace area, trace material, and the number of layers and thermal vias. If a four layer board is used with maximum vias from the IC center to the heat dissipating copper layers, values of θ_{J-A} which can be obtained are approximately 60°C/W for the SO PowerPAD-8 and 40°C/W for the WSON-8 package. For improved thermal resistance and power dissipation for the WSON package, refer to Application Note AN-1187. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown.
(5) If used in a dual-supply system where the regulator load is returned to a negative supply, the LP3878-ADJ output must be diode-clamped to ground.
(6) The output PNP structure contains a diode between the V_{IN} and V_{OUT} terminals that is normally reverse-biased. Forcing the output above the input will turn on this diode and may induce a latch-up mode which can damage the part (see Application Hints).

Electrical Characteristics

Limits in standard typeface are for T_J = 25°C, and limits in **boldface type** apply over the temperature range of -40°C to 125°C. Limits are specified through design, testing, or correlation. The limits are used to calculate TI's Average Outgoing Quality Level (AOQL). Unless otherwise specified: V_{IN} = 3.0V, V_{OUT} = 1V, I_L = 1 mA, C_{OUT} = 10 µF, C_{IN} = 4.7 µF, $V_{S/D}$ = 2V, C_{BYPASS} = 10 nF.

Symbol	Parameter	Conditions	Min	Typical	Max	Units
V_{ADJ}	Adjust Pin Voltage		0.99	1.00	1.01	V
		1 mA ≤ I_L ≤ 800 mA 3.0V ≤ V_{IN} ≤ 6V	0.98 **0.97**	1.00	1.02 **1.03**	
$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	Output Voltage Line Regulation	3.0V ≤ V_{IN} ≤ 16V		0.007	0.014 **0.032**	%/V
V_{IN} (min)	Minimum Input Voltage Required To Maintain Output Regulation	I_L = 800 mA, V_{OUT} ≥ $V_{OUT(NOM)}$ - 1%		2.5	**3.1**	V
		I_L = 800 mA V_{OUT} ≥ $V_{OUT(NOM)}$ - 1% 0 ≤ T_J ≤ 125°C		2.5	**2.8**	
		I_L = 750 mA, V_{OUT} ≥ $V_{OUT(NOM)}$ - 1%		2.5	**3.0**	
V_{DO}	Dropout Voltage(1) V_{OUT} = 3.8V	I_L = 100 µA		1	2 **3**	mV
		I_L = 200 mA		150	200 **300**	
		I_L = 800 mA		475	600 **1100**	
I_{GND}	Ground Pin Current	I_L = 100 µA		180	200 **225**	µA
		I_L = 200 mA		1.5	2 **3.5**	mA
		I_L = 800 mA		5.5	8.5 **15**	
I_O(PK)	Peak Output Current	V_{OUT} ≥ $V_{OUT(NOM)}$ − 5%		1200		mA
I_O(MAX)	Short Circuit Current	R_L = 0 (Steady State)		1300		
e_n	Output Noise Voltage (RMS)	BW = 100 Hz to 100 kHz C_{BYPASS} = 10 nF		18		µV(RMS)
$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	Ripple Rejection	f = 1 kHz		60		dB
I_{ADJ}	ADJ Pin Bias Current (Sourcing)	I_L = 800 mA		200		nA
SHUTDOWN INPUT						
$V_{S/D}$	S/D Input Voltage	V_H = Output ON		1.4	**1.6**	V
		V_L = Output OFF, I_{IN} ≤ 10 µA	**0.04**	0.20		
		V_{OUT} ≤ 10 mV, I_{IN} ≤ 50 µA		0.6		
$I_{S/D}$	S/D Input Current	$V_{S/D}$ = 0		0.02	**−1**	µA
		$V_{S/D}$ = 5V		5	**15**	

(1) Dropout voltage spec applies only if V_{IN} is sufficient so that it does not limit regulator operation.

Typical Performance Characteristics

Unless otherwise specified: V_{IN} = 3.3V, V_{OUT} = 1V, I_L = 1 mA, C_{IN} = 4.7 µF, C_{OUT} = 10 µF, $V_{S/D}$ = 2V, C_{BYP} = 10 nF, T_J = 25°C.

I_{GND} vs Temperature

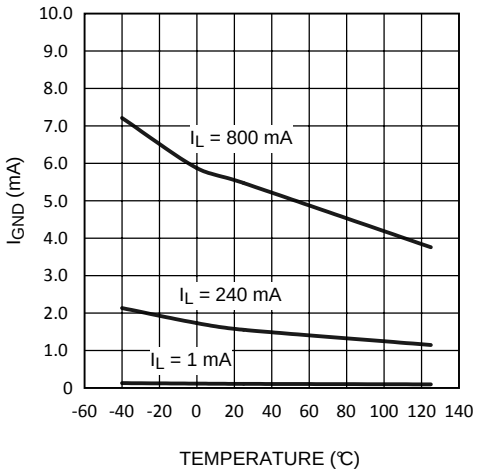


Figure 3.

Minimum V_{IN} Over Temperature

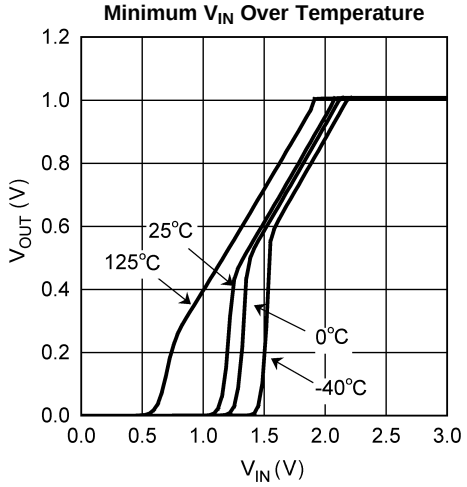


Figure 4.

I_{GND} vs I_{Load}

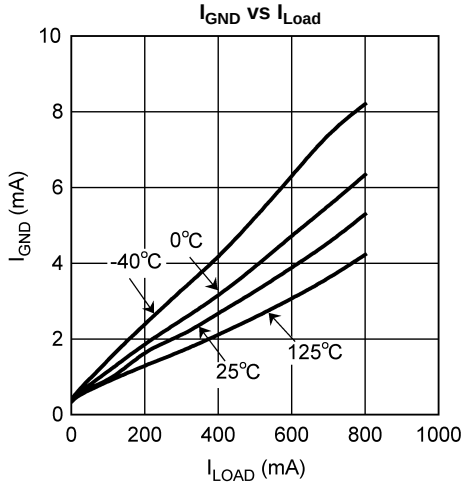


Figure 5.

V_{OUT} vs Temperature

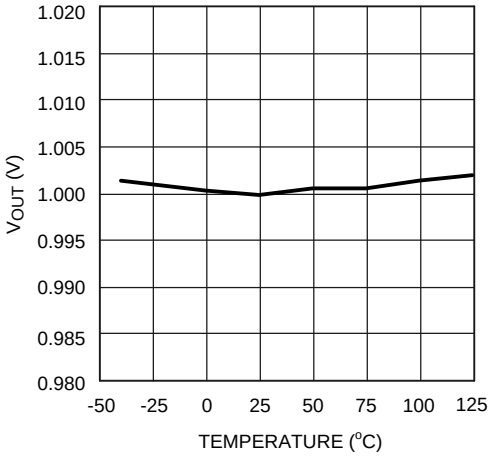


Figure 6.

Minimum V_{IN} vs V_{OUT}

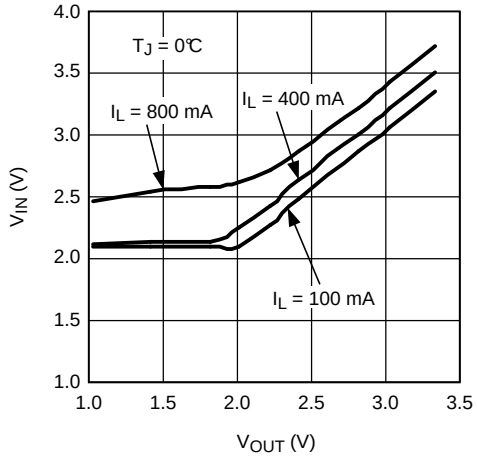


Figure 7.

Minimum V_{IN} vs V_{OUT}

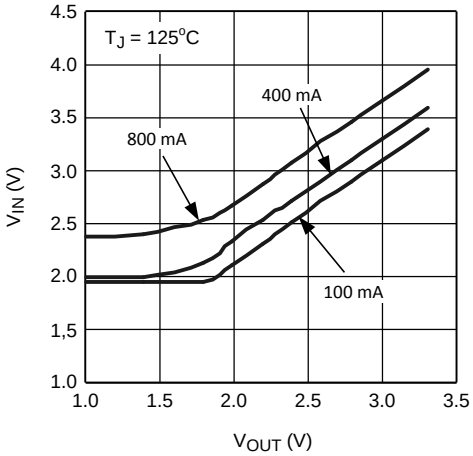


Figure 8.

Typical Performance Characteristics (continued)

Unless otherwise specified: V_{IN} = 3.3V, V_{OUT} = 1V, I_L = 1 mA, C_{IN} = 4.7 µF, C_{OUT} = 10 µF, $V_{S/D}$ = 2V, C_{BYP} = 10 nF, T_J = 25°C.

Minimum V_{IN} vs V_{OUT}

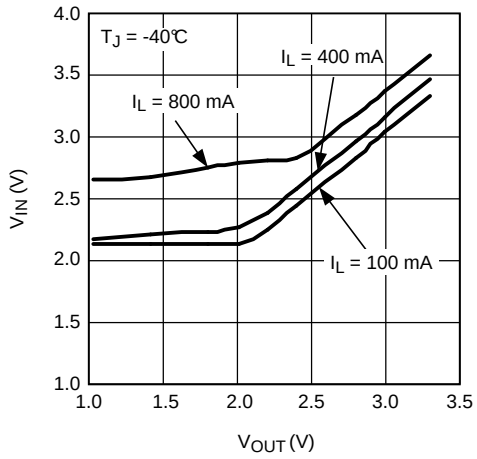


Figure 9.

Ripple Rejection

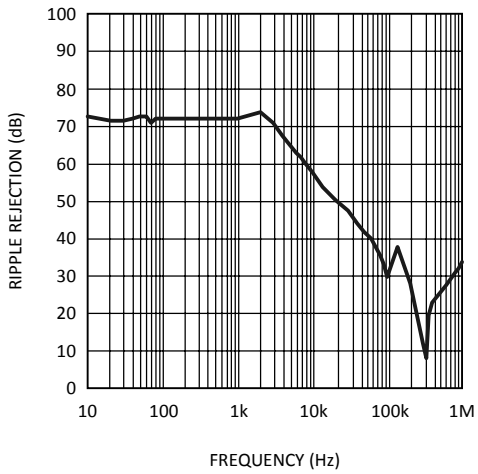


Figure 10.

Ripple Rejection

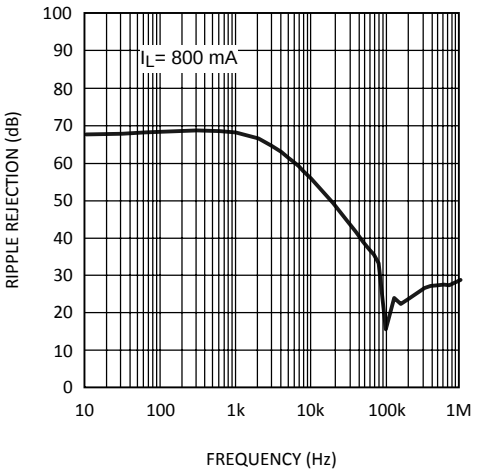


Figure 11.

Output Noise Spectral Density

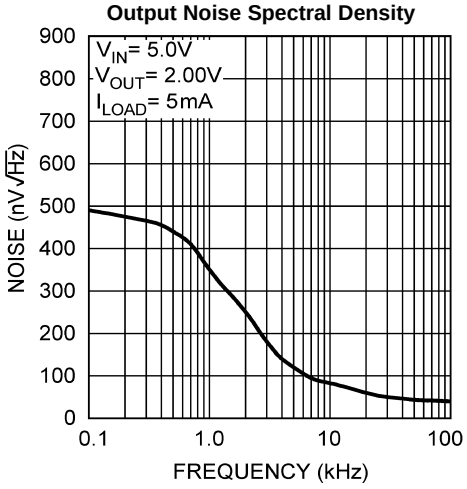


Figure 12.

Output Noise Spectral Density

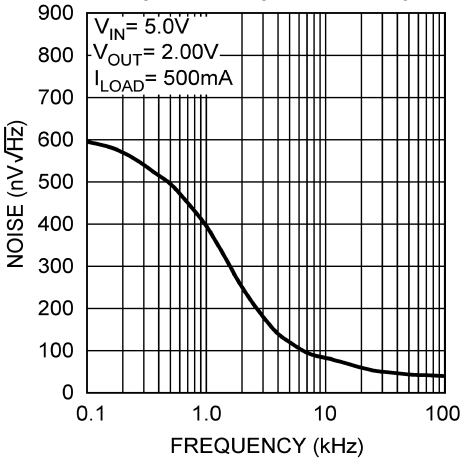


Figure 13.

Line Transient Response

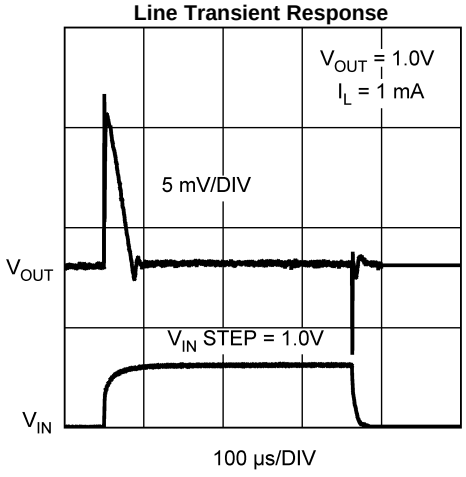
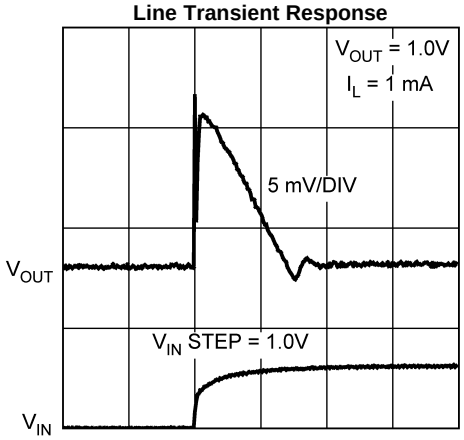


Figure 14.

Typical Performance Characteristics (continued)

Unless otherwise specified: V_{IN} = 3.3V, V_{OUT} = 1V, I_L = 1 mA, C_{IN} = 4.7 µF, C_{OUT} = 10 µF, $V_{S/D}$ = 2V, C_{BYP} = 10 nF, T_J = 25°C.

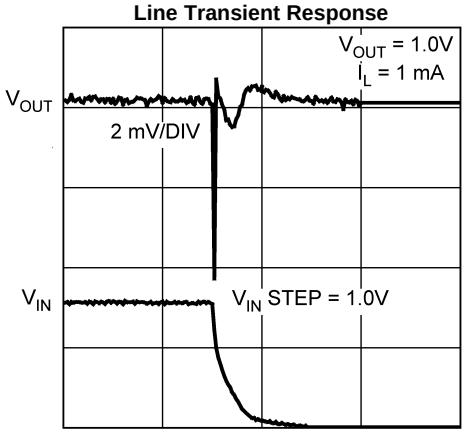
Line Transient Response



25 µs/DIV

Figure 15.

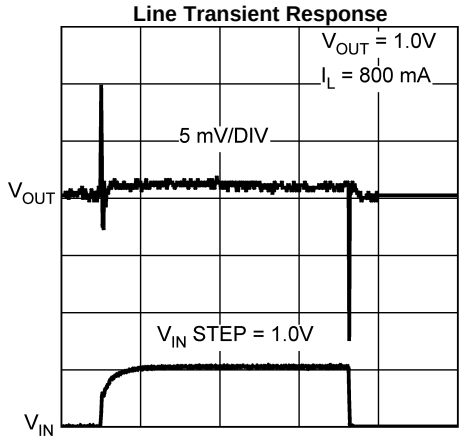
Line Transient Response



25 µs/DIV

Figure 16.

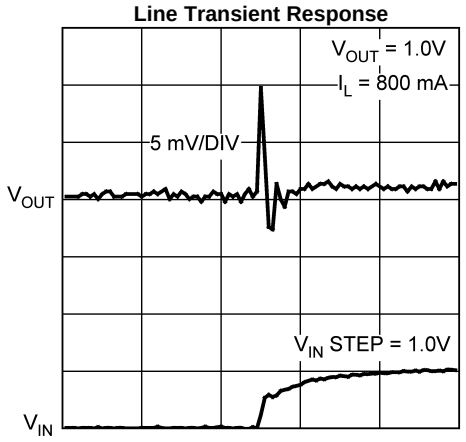
Line Transient Response



100 µs/DIV

Figure 17.

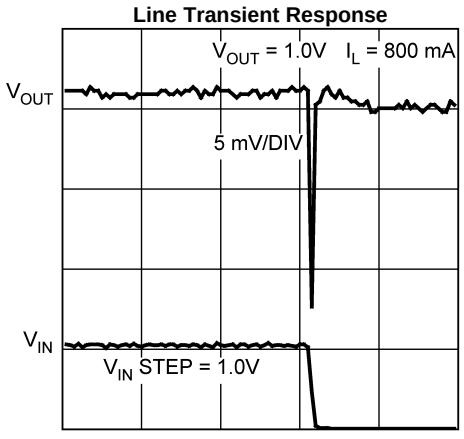
Line Transient Response



20 µs/DIV

Figure 18.

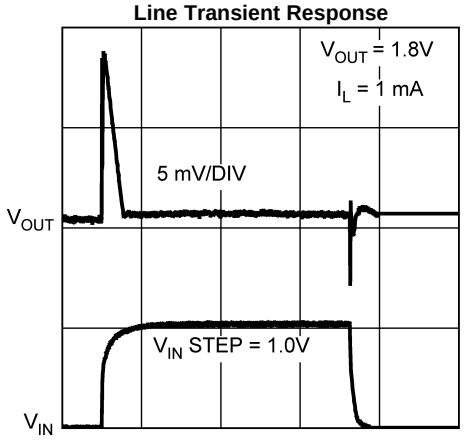
Line Transient Response



20 µs/DIV

Figure 19.

Line Transient Response



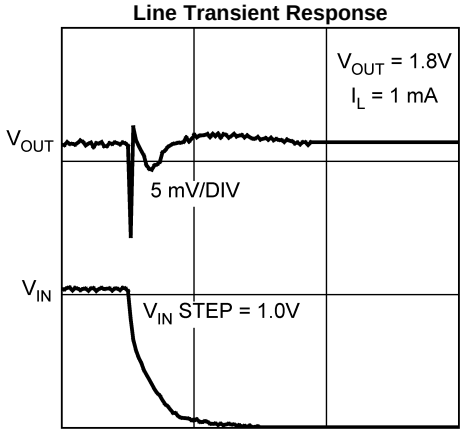
100 µs/DIV

Figure 20.

Typical Performance Characteristics (continued)

Unless otherwise specified: V_{IN} = 3.3V, V_{OUT} = 1V, I_L = 1 mA, C_{IN} = 4.7 µF, C_{OUT} = 10 µF, $V_{S/D}$ = 2V, C_{BYP} = 10 nF, T_J = 25°C.

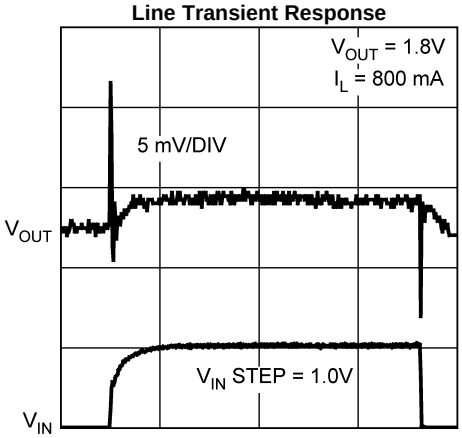
Line Transient Response



25 µs/DIV

Figure 21.

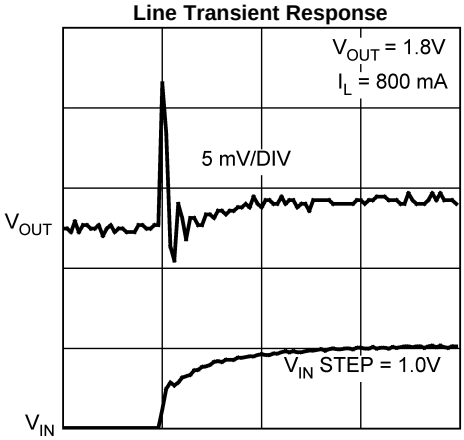
Line Transient Response



100 µs/DIV

Figure 22.

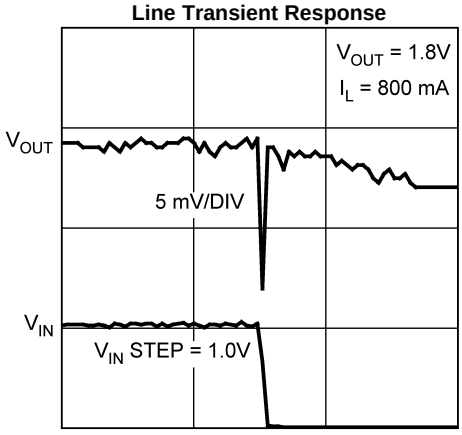
Line Transient Response



25 µs/DIV

Figure 23.

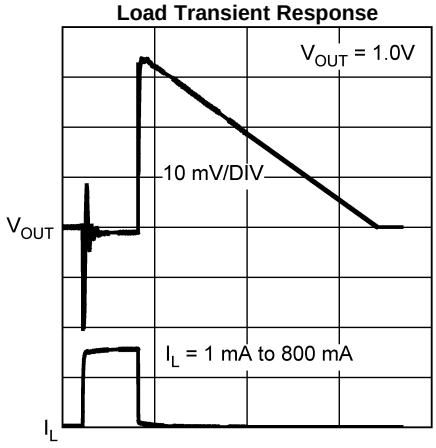
Line Transient Response



25 µs/DIV

Figure 24.

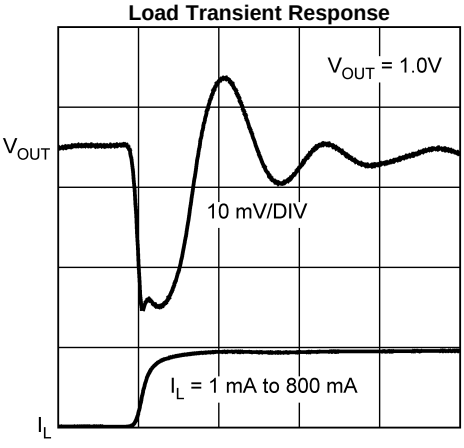
Load Transient Response



50 µs/DIV

Figure 25.

Load Transient Response



2 µs/DIV

Figure 26.

Typical Performance Characteristics (continued)

Unless otherwise specified: V_{IN} = 3.3V, V_{OUT} = 1V, I_L = 1 mA, C_{IN} = 4.7 µF, C_{OUT} = 10 µF, $V_{S/D}$ = 2V, C_{BYP} = 10 nF, T_J = 25°C.

Load Transient Response

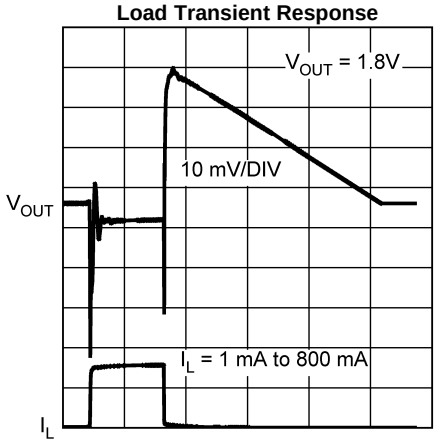


Figure 27.

Load Transient Response

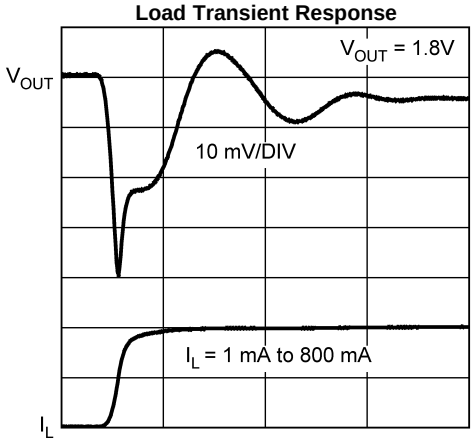


Figure 28.

Turn-On Characteristics

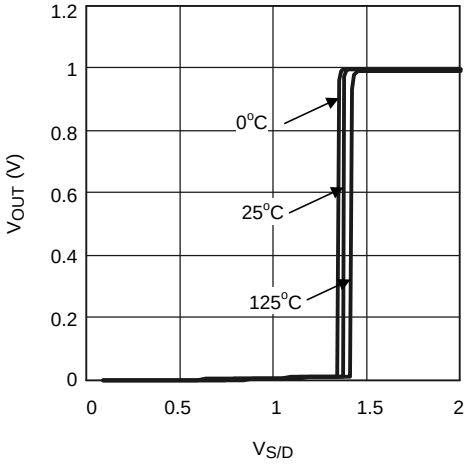


Figure 29.

Turn-Off Characteristics

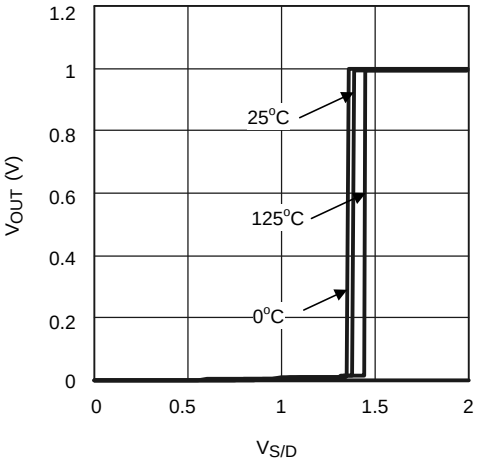
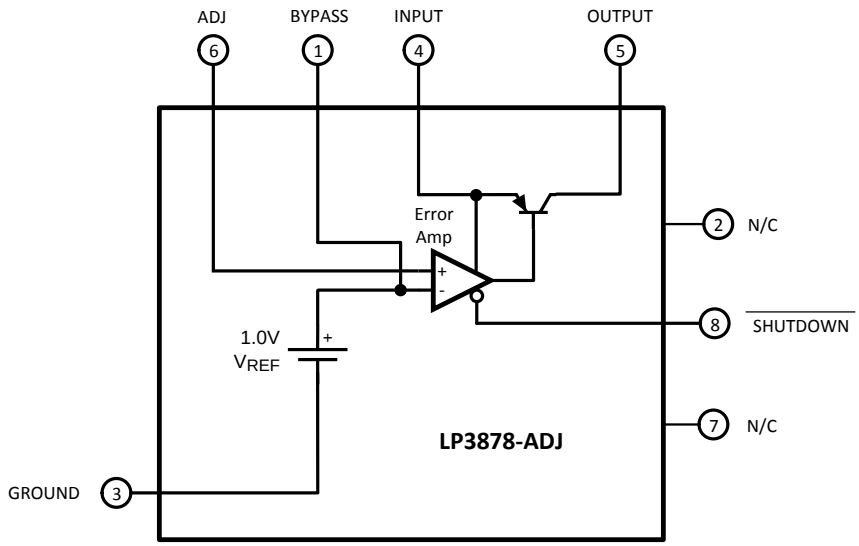


Figure 30.

Block Diagram



APPLICATION INFORMATION

PACKAGE INFORMATION

The LP3878-ADJ is offered in the 8 lead SO PowerPAD or WSON surface mount packages to allow for increased power dissipation compared to the SO-8 and Mini SO-8. For details on thermal performance as well as mounting and soldering specifications, refer to Application Note AN-1187.

EXTERNAL CAPACITORS

Like any low-dropout regulator, the LP3878-ADJ requires external capacitors for regulator stability. These capacitors must be correctly selected for good performance.

INPUT CAPACITOR:

A capacitor whose value is at least 4.7 µF (±20%) is required between the LP3878-ADJ input and ground. A good quality X5R / X7R ceramic capacitor should be used.

Capacitor tolerance and temperature variation must be considered when selecting a capacitor (see CAPACITOR CHARACTERISTICS section) to assure the minimum requirement of input capacitance is met over all operating conditions.

The input capacitor must be located not more than 0.5" from the input pin and returned to a clean analog ground. Any good quality ceramic or tantalum capacitor may be used, assuming the minimum input capacitance requirement is met.

OUTPUT CAPACITOR:

The LP3878-ADJ requires a ceramic output capacitor whose size is at least 10 µF (±20%). A good quality X5R / X7R ceramic capacitor should be used. Capacitance tolerance and temperature characteristics must be considered when selecting an output capacitor.

The LP3878-ADJ is designed specifically to work with ceramic output capacitors, utilizing circuitry which allows the regulator to be stable across the entire range of output current with an ultra low ESR output capacitor.

The output capacitor selected must meet the requirement for minimum amount of capacitance and also have an ESR (equivalent series resistance) value which is within the stable range. A curve is provided which shows the stable ESR range as a function of load current (see Figure 31).

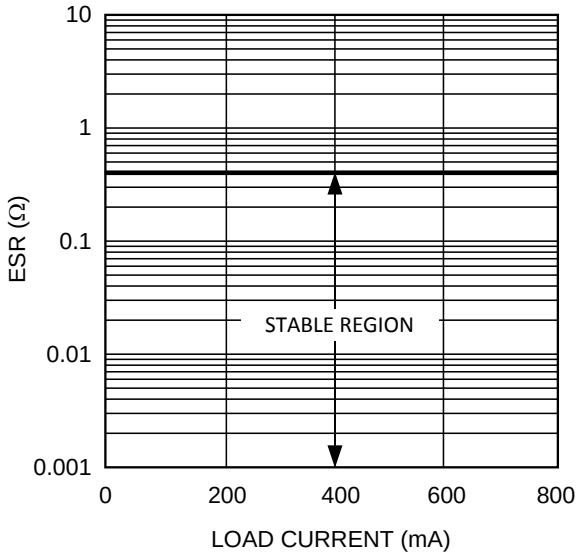


Figure 31. Stable Region For Output Capacitor ESR

NOTE

Important: The output capacitor must maintain its ESR within the stable region *over the full operating temperature range of the application* to assure stability.

The output capacitor ESR forms a zero which is required to add phase lead near the loop gain crossover frequency, typically in the range of 50kHz to 200 kHz. The ESR at lower frequencies is of no importance. Some capacitor manufacturers list ESR at low frequencies only, and some give a formula for Dissipation Factor which can be used to calculate a value for a term referred to as ESR. However, since the DF formula is usually at a much lower frequency than the range listed above, it will give an unrealistically high value. If good quality X5R or X7R ceramic capacitors are used, the actual ESR in the 50 kHz to 200 kHz range will not exceed 25 milli Ohms. If these are used as output capacitors for the LP3878-ADJ, the regulator stability requirements are satisfied.

It is important to remember that capacitor tolerance and variation with temperature must be taken into consideration when selecting an output capacitor so that the minimum required amount of output capacitance is provided over the full operating temperature range. (See CAPACITOR CHARACTERISTICS).

The output capacitor must be located not more than 0.5" from the output pin and returned to a clean analog ground.

NOISE BYPASS CAPACITOR:

The 10 nF capacitor on the Bypass pin significantly reduces noise on the regulator output and is required for loop stability. However, the capacitor is connected directly to a high-impedance circuit in the bandgap reference.

Because this circuit has only a few microamperes flowing in it, any significant loading on this node will cause a change in the regulated output voltage. For this reason, DC leakage current through the noise bypass capacitor must never exceed 100 nA, and should be kept as low as possible for best output voltage accuracy.

The types of capacitors best suited for the noise bypass capacitor are ceramic and film. High-quality ceramic capacitors with either NPO or COG dielectric typically have very low leakage. 10 nF polypropolene and polycarbonate film capacitors are available in small surface-mount packages and typically have extremely low leakage current.

FEEDFORWARD CAPACITOR

The feedforward capacitor designated C_{FF} in the Basic Application circuit is required to increase phase margin and assure loop stability. Improved phase margin also gives better transient response to changes in load or input voltage, and faster settling time on the output voltage when transients occur. C_{FF} forms both a pole and zero in the loop gain, the zero providing beneficial phase lead (which increases phase margin) and the pole adding undesirable phase lag (which should be minimized). The zero frequency is determined both by the value of C_{FF} and R1:

$$fz = 1 / (2 \times \pi \times C_{FF} \times R1) \quad (1)$$

The pole frequency resulting from C_{FF} is determined by the value of C_{FF} and the parallel combination of R1 and R2:

$$fp = 1 / (2 \times \pi \times C_{FF} \times (R1 // R2)) \quad (2)$$

At higher output voltages where R1 is much greater than R2, the value of R2 primarily determines the value of the parallel combination of R1 // R2. This puts the pole at a much higher frequency than the zero. As the regulated output voltage is reduced (and the value of R1 decreases), the parallel effect of R2 diminishes and the two equations become equal (at which point the pole and zero cancel out). Because the pole frequency gets closer to the zero at lower output voltages, the beneficial effects of C_{FF} are increased if the frequency range of the zero is shifted slightly higher for applications with low Vout (because then the pole adds less phase lag at the loop's crossover frequency).

C_{FF} should be selected to place the pole zero pair at a frequency where the net phase lead added to the loop at the crossover frequency is maximized. The following design guidelines were obtained from bench testing to optimize phase margin, transient response, and settling time:

For Vout ≤ 2.5V: C_{FF} should be selected to set the zero frequency in the range of about 50 kHz to 200 kHz.

For Vout > 2.5V: C_{FF} should be selected to set the zero frequency in the range of about 20 kHz to 100 kHz.

CAPACITOR CHARACTERISTICS

CERAMIC:

The LP3878-ADJ was designed to work with ceramic capacitors on the output to take advantage of the benefits they offer: for capacitance values in the 10 µF range, ceramics are the least expensive and also have the lowest ESR values (which makes them best for eliminating high-frequency noise). The ESR of a typical 10 µF ceramic capacitor is in the range of 5 mΩ to 10 mΩ, which meets the ESR limits required for stability by the LP3878-ADJ.

One disadvantage of ceramic capacitors is that their capacitance can vary with temperature. Many large value ceramic capacitors (≥ 2.2 µF) are manufactured with the Z5U or Y5V temperature characteristic, which results in the capacitance dropping by more than 50% as the temperature goes from 25°C to 85°C.

Another significant problem with Z5U and Y5V dielectric devices is that the capacitance drops severely with applied voltage. A typical Z5U or Y5V capacitor can lose 60% of its rated capacitance with half of the rated voltage applied to it.

For these reasons, X7R and X5R type ceramic capacitors must be used on the input and output of the LP3878-ADJ.

SHUTDOWN INPUT OPERATION

The LP3878-ADJ is shut off by pulling the Shutdown input low, and turned on by pulling it high. If this feature is not to be used, the Shutdown input should be tied to V_{IN} to keep the regulator output on at all times.

To assure proper operation, the signal source used to drive the Shutdown input must be able to swing above and below the specified turn-on/turn-off voltage thresholds listed in the Electrical Characteristics section under $V_{ON/OFF}$.

REVERSE INPUT-OUTPUT VOLTAGE

The PNP power transistor used as the pass element in the LP3878-ADJ has an inherent diode connected between the regulator output and input.

During normal operation (where the input voltage is higher than the output) this diode is reverse-biased.

However, if the output is pulled above the input, this diode will turn ON and current will flow into the regulator output.

In such cases, a parasitic SCR can latch which will allow a high current to flow into V_{IN} (and out the ground pin), which can damage the part.

In any application where the output may be pulled above the input, an external Schottky diode must be connected from V_{IN} to V_{OUT} (cathode on V_{IN}, anode on V_{OUT}), to limit the reverse voltage across the LP3878-ADJ to 0.3V (see Absolute Maximum Ratings).

SETTING THE OUTPUT VOLTAGE

The output voltage is set using resistors R1 and R2 (see Basic Application Circuit).

The formula for output voltage is:

$$V_{OUT} = V_{ADJ} \times (1 + (R_1 / R_2)) \quad (3)$$

R2 must be less than 5 kΩ to ensure loop stability.

To prevent voltage errors, R1 and R2 must be located near the LP3878-ADJ and connected via traces with no other currents flowing in them (Kelvin connect). The bottom of the R1/R2 divider must be connected directly to the LP3878-ADJ ground pin.

REVISION HISTORY

Changes from Revision A (April 2013) to Revision B	Page
• Changed layout of National Data Sheet to TI format	13

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP3878MR-ADJ	NRND	SO PowerPAD	DDA	8	95	TBD	Call TI	Call TI		3878 MRADJ	
LP3878MR-ADJ/NOPB	ACTIVE	SO PowerPAD	DDA	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR		3878 MRADJ	Samples
LP3878MRX-ADJ/NOPB	ACTIVE	SO PowerPAD	DDA	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR		3878 MRADJ	Samples
LP3878SD-ADJ/NOPB	ACTIVE	WSON	NGT	8	1000	Green (RoHS & no Sb/Br)	SN | Call TI	Level-1-260C-UNLIM		3878ADJ	Samples
LP3878SDX-ADJ/NOPB	ACTIVE	WSON	NGT	8	4500	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM		3878ADJ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

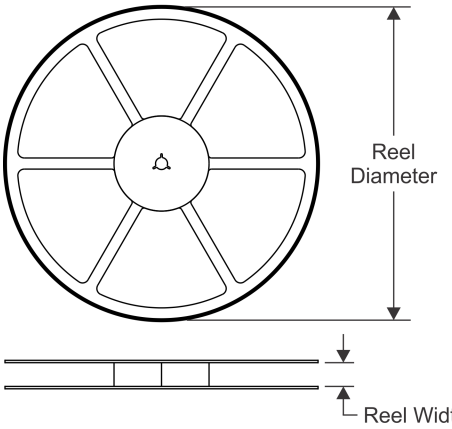
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

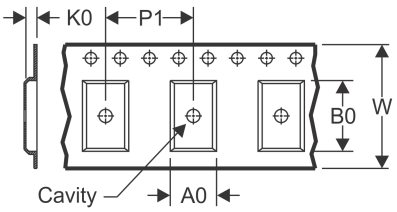
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

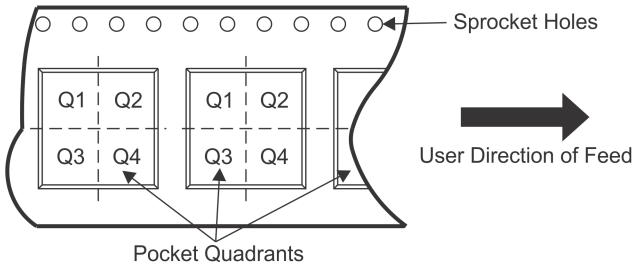


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

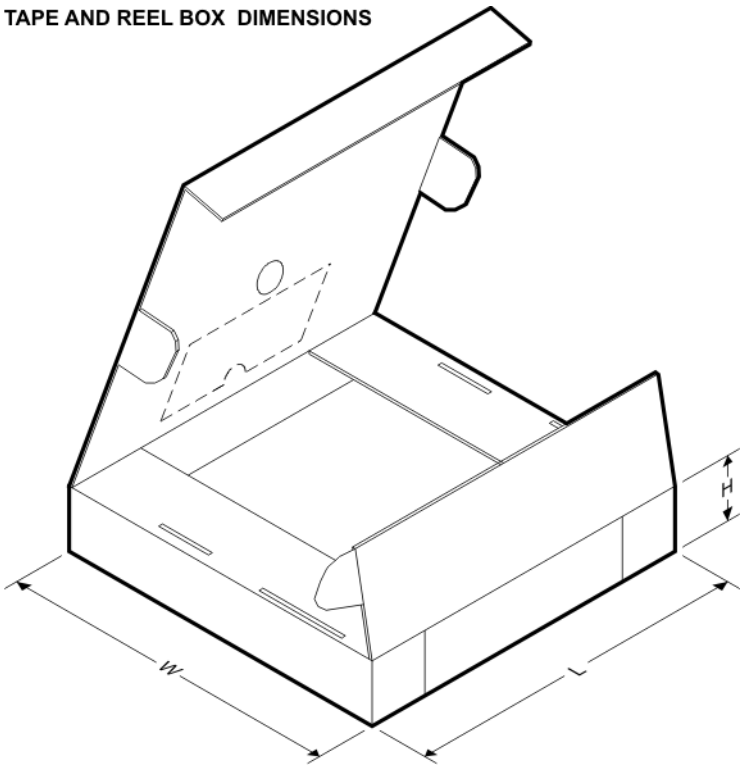
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP3878MRX-ADJ/NOPB	SO Power PAD	DDA	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LP3878SD-ADJ/NOPB	WSON	NGT	8	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LP3878SDX-ADJ/NOPB	WSON	NGT	8	4500	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1

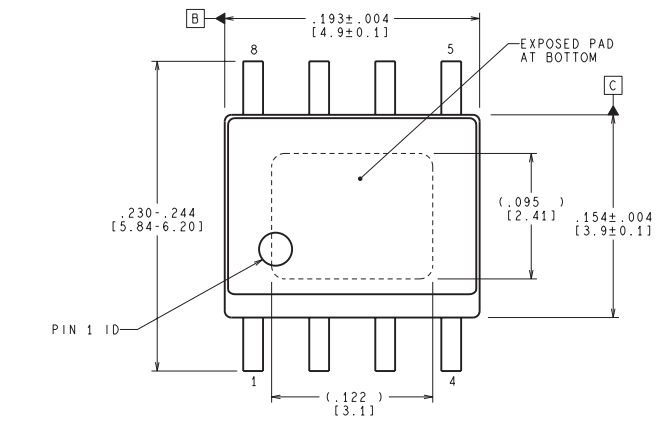
TAPE AND REEL BOX DIMENSIONS

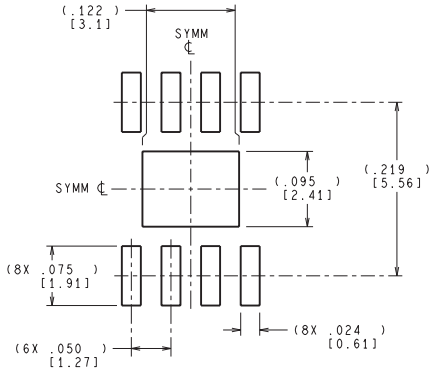


*All dimensions are nominal

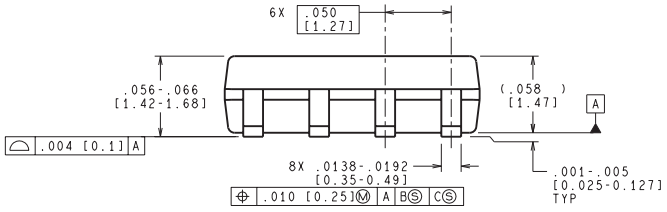
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP3878MRX-ADJ/NOPB	SO PowerPAD	DDA	8	2500	367.0	367.0	35.0
LP3878SD-ADJ/NOPB	WSON	NGT	8	1000	210.0	185.0	35.0
LP3878SDX-ADJ/NOPB	WSON	NGT	8	4500	367.0	367.0	35.0

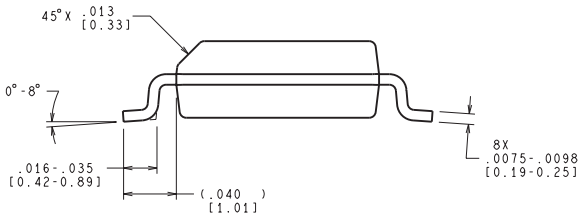
DDA0008B





RECOMMENDED LAND PATTERN





CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS
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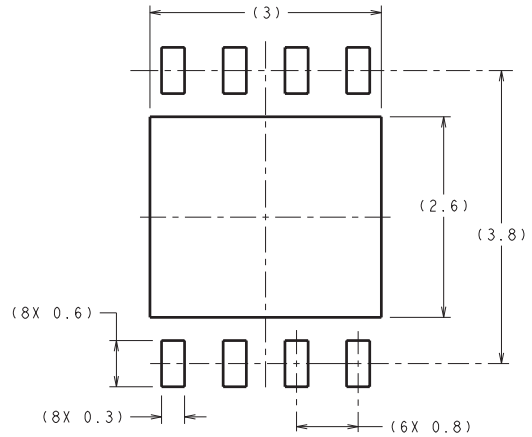

DIMENSIONS ARE IN MILLIMETERS
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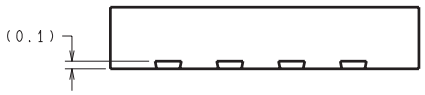
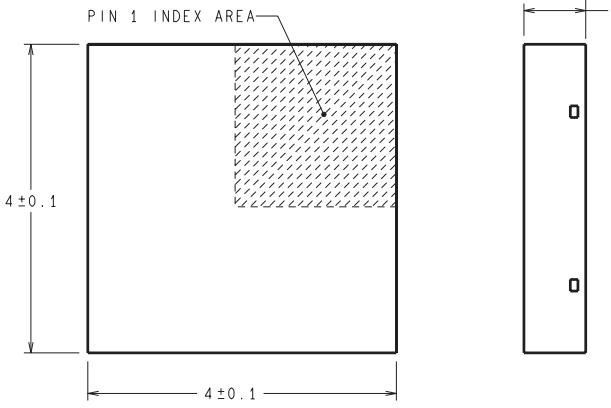
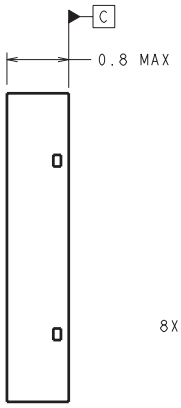
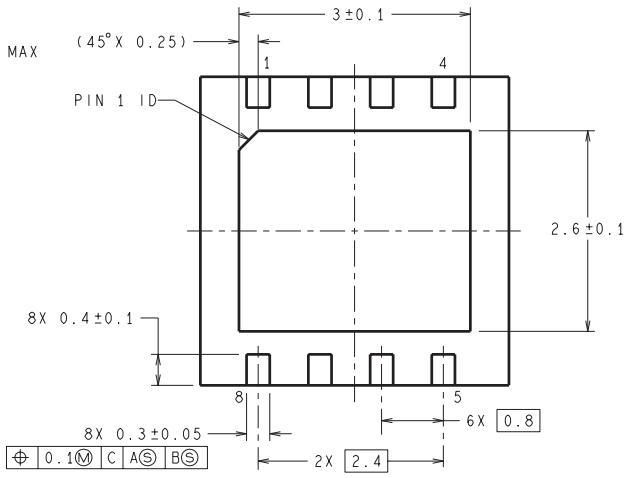


RECOMMENDED LAND PATTERN







SDC08A (Rev A)

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