LM4550 AC '97 Rev 2.1 Multi-Channel Audio Codec with Stereo Headphone Amplifier, Sample Rate Conversion and National 3D Sound

Check for Samples: LM4550

FEATURES

- **AC '97 Rev 2.1 Compliant**
- **High Quality Sample Rate Conversion From 4 kHz to 48 kHz in 1 Hz Increments**
- **Supports up to 6 DAC Channel Systems With Multiple LM4550s or With Other National LM45xx Codecs**
- **Unique National Chaining Function Shares a Single Controller SDATA_IN Pin Among Multiple Codecs**
- **Stereo Headphone Amp With Separate Hain Control**
- **National's 3D Sound Stereo Enhancement Circuitry**
- **Advanced Power Management Support**
- **External Amplifier Power Down (EAPD) Control**
- **PC Beep Passthrough to Line Out during Initialization or Cold Reset**
- **Digital 3.3V and 5V Supply Options**
- **Extended Temperature: $-40°C \leq T_A \leq 85°C$**

APPLICATIONS

- **Desktop PC Audio Systems on PCI Cards, AMR Cards, or With Motherboard Chips Sets Featuring AC Link**
- **Portable PC Systems as on MDC Cards, or With a Chipset or Accelerator Featuring AC Link**
- **General Audio Frequency Systems Requiring 2, 4 or 6 DAC Channels and/or up to 8 ADC Channels**

KEY SPECIFICATIONS

- **Analog Mixer Dynamic Range: 97 dB (typ)**
- **DAC Dynamic Range: 89 dB (typ)**
- **ADC Dynamic Range: 90 dB (typ)**
- **Headphone Amp THD+N at 50 mW: 0.02% (typ) into 32Ω**

DESCRIPTION

The LM4550 is an audio codec for PC systems which is fully PC99 compliant and performs the analog intensive functions of the AC '97 Rev 2.1 architecture. Using 18-bit Sigma-Delta ADCs and DACs, the LM4550 provides 90 dB of Dynamic Range.

The LM4550 was designed specifically to provide a high quality audio path and provide all analog functionality in a PC audio system. It features full duplex stereo ADCs and DACs and analog mixers with access to 4 stereo and 4 mono inputs. Each mixer input has separate gain, attenuation and mute control and the mixers drive 1 mono and 2 stereo outputs, each with attenuation and mute control. The LM4550 provides a stereo headphone amplifier as one of its stereo outputs and also supports National's 3D Sound stereo enhancement and a comprehensive sample rate conversion capability. The sample rate for the ADCs and DACs can be programmed separately with a resolution of 1 Hz to convert any rate in the range 4 kHz – 48 kHz. Sample timing from the ADCs and sample request timing for the DACs are completely deterministic to ease task scheduling and application software development. These features together with an extended temperature range also make the LM4550 suitable for non-PC codec applications.

The LM4550 features the ability to connect several codecs together in a system to provide up to 6 simultaneous channels of streaming data on Output Frames (Controller to Codec) for surround sound applications. Such systems can also support up to 8 simultaneous channels of streaming data on Input Frames (Codec to Controller). Multiple codec systems can be built either using the standard AC Link configuration (*i.e.* of one serial data signal to the Controller per codec) or using a unique National Semiconductor feature for chaining codecs together. This chain feature shares only a single data signal to the controller among multiple codecs.

The AC '97 architecture separates the analog and digital functions of the PC audio system allowing both for system design flexibility and increased performance.

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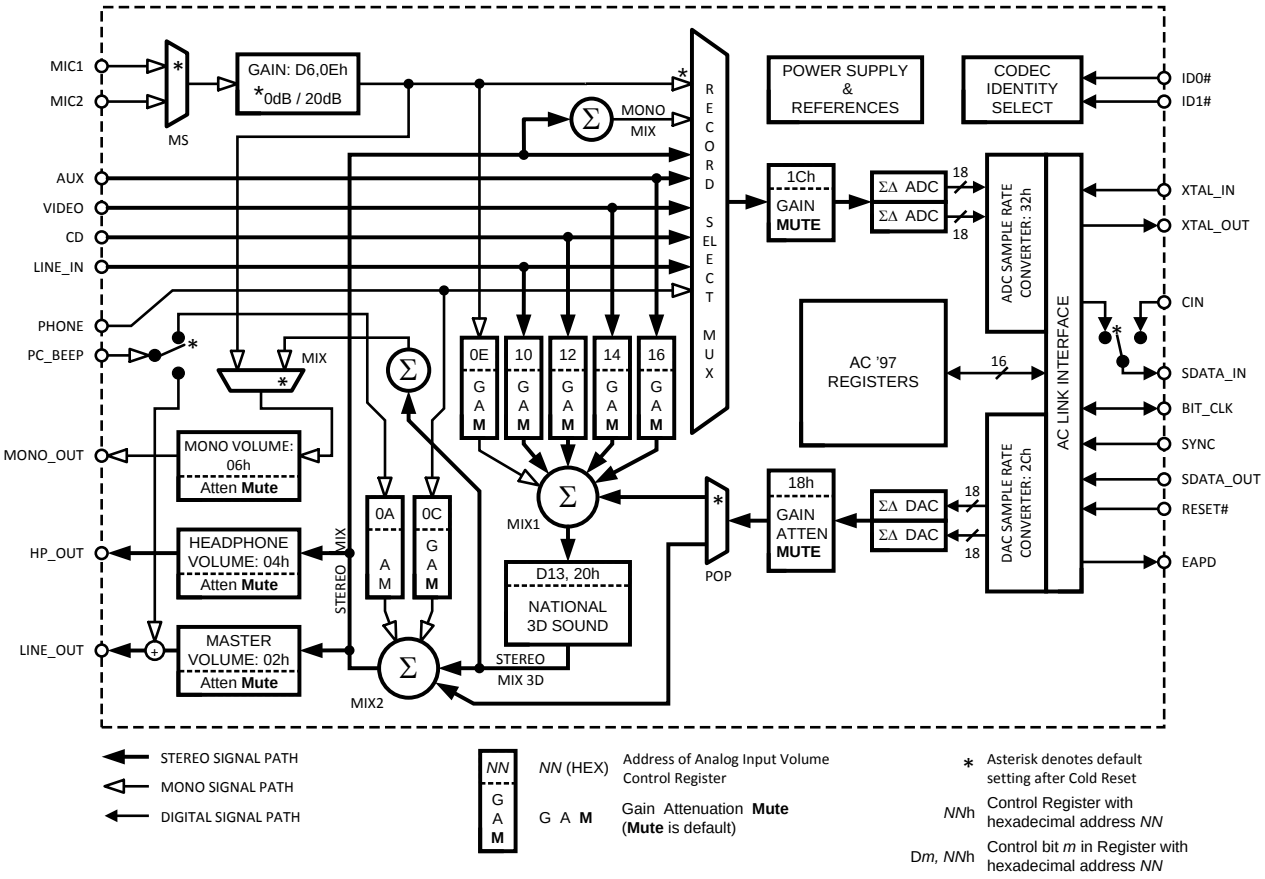
Block Diagram



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

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Absolute Maximum Ratings(1)

Supply Voltage	6.0V
Storage Temperature	−65°C to +150°C
Input Voltage	−0.3V to V_{DD} +0.3V
ESD Susceptibility(2)	2000V
pin 3	750V
ESD Susceptibility(3)	200V
pin 3	100V
Junction Temperature	150°C
Soldering Information	
LQFP Package	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C
θ_{JA} (typ) – PT	74°C/W

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not ensured for parameters where no limit is given, however, the typical value is a good indication of device performance.
(2) Human body model, 100 pF discharged through a 1.5 kΩ resistor.
(3) Machine Model, 220 pF – 240 pF discharged through all pins.

Operating Ratings

Temperature Range	
$T_{MIN} \le T_A \le T_{MAX}$(1)	−40°C ≤ T_A ≤ 85°C
Analog Supply Range	4.2V ≤ AV_{DD} ≤ 5.5V
Digital Supply Range	3.0V ≤ DV_{DD} ≤ 5.5V

(1) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature T_A. The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX} - T_A)/\theta_{JA}$ or the number given in Absolute Maximum Ratings, whichever is lower. For the LM4550, T_{JMAX} = 150°C. The typical junction-to-ambient thermal resistance is 74°C/W for package number PT.

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Electrical Characteristics

The following specifications apply for AV_{DD} = 5V, DV_{DD} = 5V, Fs = 48 kHz, single codec configuration, unless otherwise noted. Limits apply for T_A= 25°C. The reference for 0 dB is 1 Vrms unless otherwise specified.(1)(2)

Symbol	Parameter	Conditions	LM4550		Units (Limits)
			Typical(3)	Limit(4)	
AV_{DD}	Analog Supply Range			4.2	V (min)
				5.5	V (max)
DV_{DD}	Digital Supply Range			3.0	V (min)
				5.5	V (max)
D_{IDD}	Digital Quiescent Power Supply Current	DV_{DD} = 5 V	43		mA
		DV_{DD} = 3.3 V	20		mA
A_{IDD}	Analog Quiescent Power Supply Current		53		mA
I_{DSD}	Digital Shutdown Current		500		µA
I_{ASD}	Analog Shutdown Current		30		µA
V_{REF}	Reference Voltage		2.23		V
PSRR	Power Supply Rejection Ratio		40		dB
Analog Loopthrough Mode(5)					
	Dynamic Range (6)	CD Input to Line Output, -60 dB Input THD+N, A-Weighted	97	90	dB (min)
THD	Total Harmonic Distortion	V_O = -3 dB, f = 1 kHz, R_L = 10 kΩ	0.01	0.02	% (max)
Analog Input Section					
V_{IN}	Line Input Voltage	LINE_IN, AUX, CD, VIDEO, PC_BEEP, PHONE	1		Vrms
V_{IN}	Mic Input with 20 dB Gain		0.1		Vrms
V_{IN}	Mic Input with 0 dB Gain		1		Vrms
Xtalk	Crosstalk	CD Left to Right	-95		dB
Z_{IN}	Input Impedance(6)	All Analog Inputs	40	10	kΩ (min)
C_{IN}	Input Capacitance		15		pF
	Interchannel Gain Mismatch	CD Left to Right	0.01		dB
Record Gain Amplifier - ADC					
A_S	Step Size	0 dB to 22.5 dB	1.5		dB
A_M	Mute Attenuation(6)		86		dB
Mixer Section					
A_S	Step Size	+12 dB to -34.5 dB	1.5		dB
A_M	Mute Attenuation		86		dB
Analog to Digital Converters					
	Resolution		18		Bits
	Dynamic Range(6)	-60 dB Input THD+N, A-Weighted	90	86	dB (min)
	Frequency Response	-1 dB Bandwidth	20		kHz
Digital to Analog Converters					
	Resolution		18		Bits
	Dynamic Range(6)	-60 dB Input THD+N, A-Weighted	89	85	dB (min)

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not ensured for parameters where no limit is given, however, the typical value is a good indication of device performance.
(2) All voltages are measured with respect to the ground pin, unless otherwise specified.
(3) Typicals are measured at 25°C and represent the parametric norm.
(4) Limits are ensured to AOQL (Average Outgoing Quality Level).
(5) Loopthrough Mode describes a path from an analog input through the analog mixers to an analog output.
(6) These specifications are ensured by design and characterization; they are not production tested.

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Electrical Characteristics (continued)

The following specifications apply for AV_{DD} = 5V, DV_{DD} = 5V, Fs = 48 kHz, single codec configuration, unless otherwise noted. Limits apply for T_A= 25°C. The reference for 0 dB is 1 Vrms unless otherwise specified.(1)(2)

Symbol	Parameter	Conditions	LM4550		Units (Limits)
			Typical(3)	Limit(4)	
THD	Total Harmonic Distortion	V_{IN} = -3 dB, f = 1 kHz, R_L = 10 kΩ	0.01		%
	Frequency Response		20 - 21 k		Hz
	Group Delay(6)			2	ms (max)
	Out of Band Energy(7)		-40		dB
	Stop Band Rejection		70		dB
D_T	Discrete Tones		-96		dB
Analog Output Section					
A_S	Step Size	0 dB to -46.5 dB	1.5		dB
A_M	Mute Attenuation		86		dB
THD+N	Headphone Amplifier Total Harmonic Distortion plus Noise	Loopthrough Mode(5), R_L = 32 Ω, f = 1 kHz, P_{out} = 50 mW	0.02		%
Z_{OUT}	Output Impedance(6)	HP_OUT_L, HP_OUT_R	TBD		Ω
Z_{OUT}	Output Impedance(6)	LINE_OUT_L, LINE_OUT_R, MONO_OUT	TBD		Ω
Digital I/O(6)					
V_{IH}	High level input voltage			0.40 x DV_{DD}	V (min)
V_{IL}	Low level input voltage			0.30 x DV_{DD}	V (max)
V_{OH}	High level output voltage			0.50 x DV_{DD}	V (min)
V_{OL}	Low level output voltage			0.20 x DV_{DD}	V (max)
I_L	Input Leakage Current	AC Link inputs		±10	µA
I_L	Tri state Leakage Current	High impedance AC Link outputs		±10	µA
I_{DR}	Output drive current	AC Link outputs	5		mA
Digital Timing Specifications(8)					
F_{BC}	BIT_CLK frequency		12.288		MHz
T_{BCP}	BIT_CLK period		81.4		ns
T_{CH}	BIT_CLK high	Variation of BIT_CLK duty cycle from 50%		±20	% (max)
F_{SYNC}	SYNC frequency		48		kHz
T_{SP}	SYNC period		20.8		µs
T_{SH}	SYNC high pulse width		1.3		µs
T_{SL}	SYNC low pulse width		19.5		µs
T_{DSETUP}	Setup Time for codec data input	SDATA_OUT to falling edge of BIT_CLK		15	ns (min)
T_{DHOLD}	Hold Time for codec data input	Hold time of SDATA_OUT from falling edge of BIT_CLK		5	ns (min)
T_{SSETUP}	Setup Time for codec SYNC input	SYNC to rising edge of BIT_CLK		TBD	ns (min)
T_{SHOLD}	Hold Time for codec SYNC input	Hold time of SYNC from rising edge of BIT_CLK		TBD	ns (min)
T_{CO}	Output Valid Delay	Output Delay of SDATA_IN from rising edge of BIT_CLK	TBD	15	ns (max)
T_{RISE}	Rise Time	BIT_CLK, SYNC, SDATA_IN or SDATA_OUT		6	ns (max)
T_{FALL}	Fall Time	BIT_CLK, SYNC, SDATA_IN or SDATA_OUT		6	ns (max)

(7) Out of band energy is measured from 28.8 kHz to 100 kHz relative to a 1 Vrms DAC output.
(8) These specifications are ensured by design and characterization; they are not production tested.

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Electrical Characteristics (continued)

The following specifications apply for AV_{DD} = 5V, DV_{DD} = 5V, Fs = 48 kHz, single codec configuration, unless otherwise noted. Limits apply for T_A= 25°C. The reference for 0 dB is 1 Vrms unless otherwise specified.(1)(2)

Symbol	Parameter	Conditions	LM4550		Units (Limits)
			Typical(3)	Limit(4)	
T_{CS}	Chain Propagation Delay	Data Delay from CIN to SDATA_IN when the chain feature is active	TBD	TBD	ns (max)
T_{RST_LOW}	RESET# active low pulse width	For Cold Reset		1.0	µs (min)
$T_{RST2CLK}$	RESET# inactive to BIT_CLK start up	For Cold Reset	TBD	162.8	ns (min)
T_{SH}	SYNC active high pulse width	For Warm Reset	1.3	TBD	µs (min)
$T_{SYNC2CLK}$	SYNC inactive to BIT_CLK start up	For Warm Reset	TBD	162.8	ns (min)
T_{S2_PDOWN}	AC Link Power Down Delay	Delay from end of Slot 2 to BIT_CLK, SDATA_IN low		1	µs (max)
$T_{SUPPLY2RST}$	Power On Reset	Time from minimum valid supply levels to end of Reset		1	µs (min)
T_{SU2RST}	Setup to trailing edge of RESET#	For ATE Test Mode		15	ns (min)
T_{RST2HZ}	Rising edge of RESET# to Hi-Z	For ATE Test Mode		25	ns (max)

Timing Diagrams

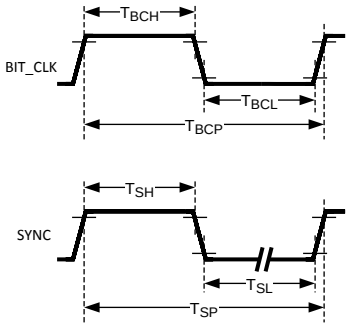

Figure 1. Clocks

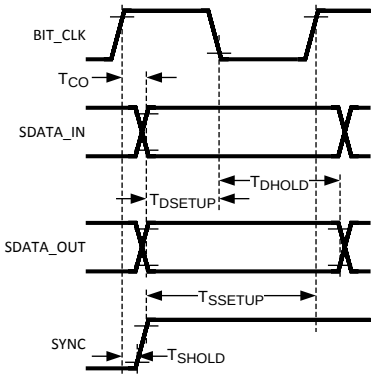

Figure 2. Data Delay, Setup and Hold

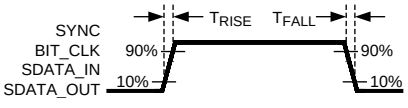

Figure 3. Digital Rise and Fall

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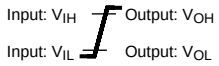

Figure 4. Legend

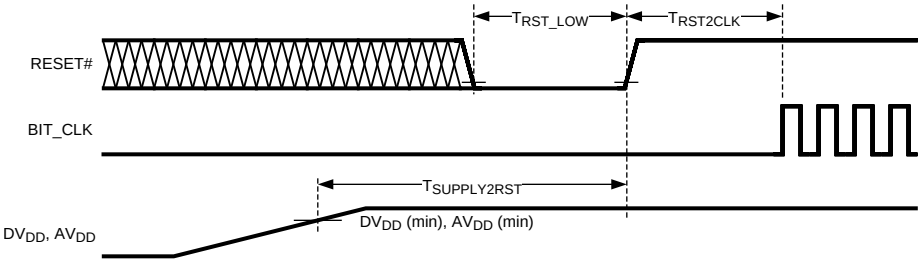

Figure 5. Power On Reset

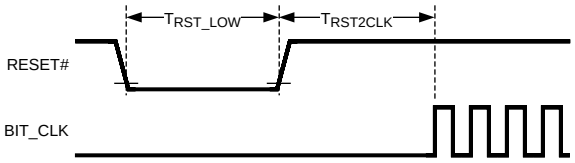

Figure 6. Cold Reset

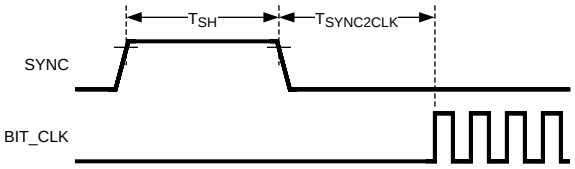

Figure 7. Warm Reset

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Typical Application

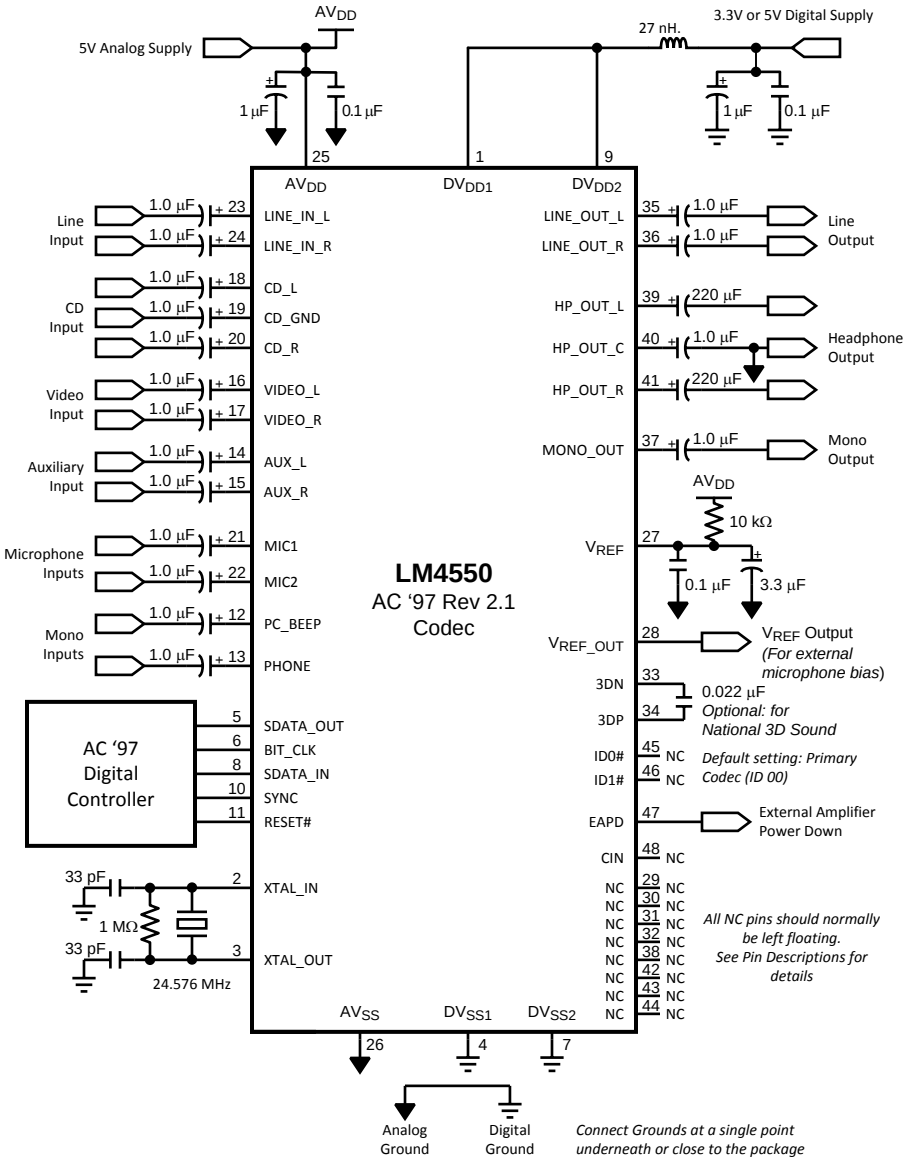

Figure 8. LM4550 Typical Application Circuit, Single Codec, 1 Vrms inputs

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APPLICATION HINTS

- The LM4550 must be initialized by using RESET# to perform a Power On Reset as shown in the Power On Reset Timing Diagram
- V_{REF} must be pulled high to AV_{DD} with a 10 kΩ resistor to ensure correct operation
- Don't leave unused inputs floating. Tie all unused inputs together and connect to Analog Ground through a capacitor (*e.g.* 0.1 µF)
- Do not leave CD_GND floating when using the CD stereo input. CD_GND is the AC signal reference for the CD channels and should be connected to the CD source ground (Analog Ground may also be acceptable) through a 1 µF capacitor
- If using a non-standard AC Link controller take care to keep the SYNC and SDATA_OUT signals low during Cold Reset to avoid accidentally activating the ATE or Vendor test modes
- The PC_Beep input should be explicitly muted if not used since it defaults to 0 dB gain on reset, unlike the mute default of the other analog inputs

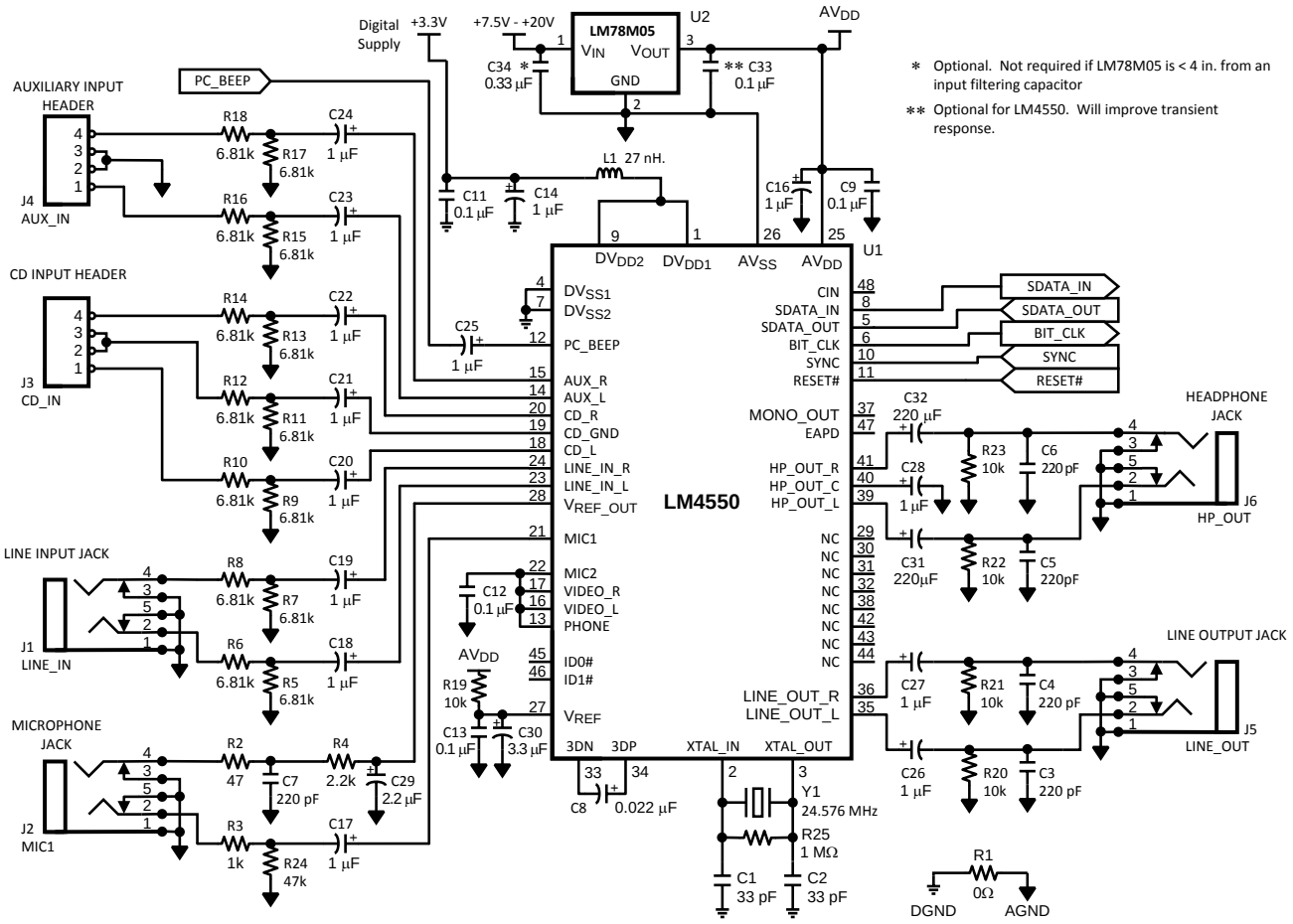

Figure 9. LM4550 Reference Design, Typical Application, Single Codec, 1 Vrms and 2 Vrms inputs, EMC output filters

Connection Diagram

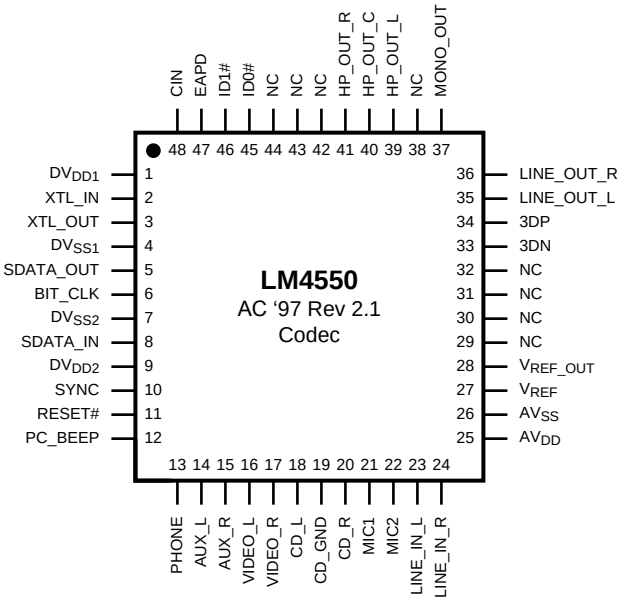

Figure 10. 48 Pin LQFP - Top View
See Package Number PT

Pin Descriptions

Table 1. ANALOG I/O

Name	Pin	I / O	Functional Description
PC_BEEP	12	I	Mono Input This line level (1 Vrms nominal) mono input is mixed equally into both channels of the Stereo Mix signal at MIX2 under the control of the PC_Beep Volume control register, 0Ah. The PC_BEEP level can be muted or adjusted from 0 dB to -45 dB in 3 dB steps. The Stereo Mix signal feeds both the Line Out and Headphone Out analog outputs and is also selectable at the Record Select Mux. During Initialization or Cold Reset, (reset pin held active low), PC_BEEP is switched directly to both channels of the Line Out stereo output, bypassing all volume controls. This allows signals such as PC power-on self-test tones to be heard through the PC's audio system before the codec registers are configured.
PHONE	13	I	Mono Input This line level (1 Vrms nominal) mono input is selectable at the Record Select Mux for conversion by either or both channels of the stereo ADC. It can also be mixed equally into both channels of the Stereo Mix signal at MIX2 under the control of the Phone Volume register, 0Ch. The PHONE level can be muted or adjusted from +12 dB to -34.5 dB in 1.5 dB steps. The Stereo Mix signal feeds both the Line Out and Headphone Out analog stereo outputs and is also selectable at the Record Select Mux.
AUX_L	14	I	Left Stereo Channel Input This line level input (1 Vrms nominal) is selectable at the left channel of the stereo Record Select Mux for conversion by the left channel ADC. It can also be mixed into the left channel of the Stereo Mix 3D signal at MIX1 under the control of the Aux Volume register, 16h. The AUX_L level can be muted (along with AUX_R) or adjusted from +12 dB to -34.5 dB in 1.5 dB steps. Stereo Mix 3D is combined into the Stereo Mix signal at MIX2 for access to the stereo outputs Line Out and Headphone Out.
AUX_R	15	I	Right Stereo Channel Input This line level input (1 Vrms nominal) is selectable at the right channel of the stereo Record Select Mux for conversion by the right channel ADC. It can also be mixed into the right channel of the Stereo Mix 3D signal at MIX1 under the control of the Aux Volume register, 16h. The AUX_R level can be muted (along with AUX_L) or adjusted from +12 dB to -34.5 dB in 1.5 dB steps. Stereo Mix 3D is combined into the Stereo Mix signal at MIX2 for access to the stereo outputs Line Out and Headphone Out.

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Table 1. ANALOG I/O (continued)

Name	Pin	I / O	Functional Description
VIDEO_L	16	I	Left Stereo Channel Input This line level input (1 Vrms nominal) is selectable at the left channel of the stereo Record Select Mux for conversion by the left channel ADC. It can also be mixed into the left channel of the Stereo Mix 3D signal at MIX1 under the control of the Video Volume register, 14h. The VIDEO_L level can be muted (along with VIDEO_R) or adjusted from +12 dB to -34.5 dB in 1.5 dB steps. Stereo Mix 3D is combined into the Stereo Mix signal at MIX2 for access to the stereo outputs Line Out and Headphone Out.
VIDEO_R	17	I	Right Stereo Channel Input This line level input (1 Vrms nominal) is selectable at the right channel of the stereo Record Select Mux for conversion by the right channel ADC. It can also be mixed into the right channel of the Stereo Mix 3D signal at MIX1 under the control of the Video Volume register, 14h. The VIDEO_R level can be muted (along with VIDEO_L) or adjusted from +12 dB to -34.5 dB in 1.5 dB steps. Stereo Mix 3D is combined into the Stereo Mix signal at MIX2 for access to the stereo outputs Line Out and Headphone Out.
CD_L	18	I	Left Stereo Channel Input This line level input (1 Vrms nominal) is selectable at the left channel of the stereo Input Mux for conversion by the left channel ADC. It can also be mixed into the left channel of the Stereo Mix 3D signal at MIX1 under the control of the CD Volume register, 12h. The CD_L level can be muted (along with CD_R) or adjusted from +12 dB to -34.5 dB in 1.5 dB steps. Stereo Mix 3D is mixed into the Stereo Mix signal at MIX2 for access to the stereo outputs Line Out and Headphone Out.
CD_GND	19	I	AC Ground Reference This input is the reference for the signals on both CD_L and CD_R. CD_GND is NOT a DC ground and must be AC-coupled to the stereo source ground common to both CD_L and CD_R. The three inputs CD_GND, CD_L and CD_R act together as a quasi-differential stereo input with CD_GND providing AC common-mode feedback to reject ground noise. This can improve the input SNR for a stereo source with a good common ground but precision resistors may be needed in any external attenuators to achieve the necessary balance between the two channels.
CD_R	20	I	Right Stereo Channel Input This line level input (1 Vrms nominal) is selectable at the right channel of the stereo Input Mux for conversion by the right channel ADC. It can also be mixed into the right channel of the Stereo Mix 3D signal at MIX1 under the control of the CD Volume register, 12h. The CD_R level can be muted (along with CD_L) or adjusted from +12 dB to -34.5 dB in 1.5 dB steps. Stereo Mix 3D is combined into the Stereo Mix signal at MIX2 for access to the stereo outputs Line Out and Headphone Out.
MIC1	21	I	Mono microphone input Either MIC1 or MIC2 can be muxed to a programmable boost amplifier with selection by the MS bit (bit D8) in the General Purpose register, 20h. The boost amplifier gain (0 dB or 20 dB) is set by the 20dB bit (D6) in the Mic Volume register, 0Eh. Nominal input levels at the two gain settings are 1 Vrms and 0.1 Vrms respectively. The amplifier output is selectable (Record Select register, 1Ah) by either the right or left channels of the Record Select Mux for conversion on either or both channels of the stereo ADC. The amplifier output can also be accessed at the stereo mixer MIX1 (muting and mixing adjustments via Mic Volume register, 0Eh) where it is mixed equally into both left and right channels of Stereo Mix 3D for access to the stereo outputs Line Out and Headphone Out. Access to the Mono analog output is selected by a mux controlled by the MIX bit (D9) in General Purpose register, 20h.
MIC2	22	I	Mono microphone input Either MIC1 or MIC2 can be muxed to a programmable boost amplifier with selection by the MS bit (bit D8) in the General Purpose register, 20h. The boost amplifier gain (0 dB or 20 dB) is set by the 20dB bit (D6) in the Mic Volume register, 0Eh. Nominal input levels at the two gain settings are 1 Vrms and 0.1 Vrms respectively. The amplifier output is selectable (Record Select register, 1Ah) by either the right or left channels of the Record Select Mux for conversion on either or both channels of the stereo ADC. The amplifier output can also be accessed at the stereo mixer MIX1 (muting and mixing adjustments via Mic Volume register, 0Eh) where it is mixed equally into both left and right channels of Stereo Mix 3D for access to the stereo outputs Line Out and Headphone Out. Access to the Mono analog output is selected by a mux controlled by the MIX bit (D9) in General Purpose register, 20h.
LINE_IN_L	23	I	Left Stereo Channel Input This line level input (1 Vrms nominal) is selectable at the left channel of the stereo Record Select Mux for conversion by the left channel ADC. It can also be mixed into the left channel of the Stereo Mix 3D signal at MIX1 under the control of the Line In Volume register, 10h. The LINE_IN_L level can be muted (along with LINE_IN_R) or adjusted from +12 dB to -34.5 dB in 1.5 dB steps. Stereo Mix 3D is combined into the Stereo Mix signal at MIX2 for access to the stereo outputs Line Out and Headphone Out.

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Table 1. ANALOG I/O (continued)

Name	Pin	I / O	Functional Description
LINE_IN_R	24	I	Right Stereo Channel Input This line level input (1 Vrms nominal) is selectable at the right channel of the stereo Input Mux for conversion by the right channel ADC. It can also be mixed into the right channel of the Stereo Mix 3D signal at MIX1 under the control of the Line In Volume register, 10h. The LINE_IN_R level can be muted (along with LINE_IN_L) or adjusted from +12 dB to -34.5 dB in 1.5 dB steps. Stereo Mix 3D is combined into the Stereo Mix signal at MIX2 for access to the stereo outputs Line Out and Headphone Out.
LINE_OUT_L	35	O	Left Stereo Channel Output This line level output (1 Vrms nominal) is fed from the left channel of the Stereo Mix signal from MIX2 via the Master Volume register, 02h. The LINE_OUT_L amplitude can be muted (along with LINE_OUT_R) or adjusted from 0 dB to -46.5 dB in 1.5 dB steps.
LINE_OUT_R	36	O	Right Stereo Channel Output This line level output (1 Vrms nominal) is fed from the right channel of the Stereo Mix signal from MIX2 via the Master Volume register, 02h. The LINE_OUT_R amplitude can be muted (along with LINE_OUT_L) or adjusted from 0 dB to -46.5 dB in 1.5 dB steps.
MONO_OUT	37	O	Mono Output This mono line level output (1 Vrms nominal) is fed from either a microphone input (MIC1 or MIC2, after boost amplifier) or from the mono sum of the left and right Stereo Mix 3D channels from MIX1. The optional National 3D Sound enhancement can be disabled (default) by the 3D bit (bit D13) in the General Purpose register, 20h. Choice of input is by the MIX bit (D9) in the same register. MIX=0 selects a microphone input. Output level can be muted or adjusted from 0 dB to -46.5 dB in 1.5 dB steps via the Mono Volume register, 06h.
HP_OUT_L	39	O	Left Stereo Channel Output This line level output (1 Vrms nominal) is fed from the left channel of the Stereo Mix signal from MIX2 via the Headphone Volume register, 04h. The HP_OUT_L amplitude can be muted (along with HP_OUT_R) or adjusted from 0 dB to - 46.5 dB in 1.5 dB steps
HP_OUT_C	40	I	AC Ground Reference In normal use, this input is the AC ground reference for HP_OUT_L and HP_OUT_R. It must be capacitively coupled to analog ground with short traces to maximize performance. It is NOT a DC ground. For non-stereo applications it may also be used to provide common-mode feedback with HP_OUT configured as one differential output rather than as outputs for two single-ended stereo channels.
HP_OUT_R	41	O	Right Stereo Channel Output This line level output (1 Vrms nominal) is fed from the right channel of the Stereo Mix signal from MIX2 via the Headphone Volume register, 04h. The HP_OUT_R amplitude can be muted (along with HP_OUT_L) or adjusted from 0 dB to - 46.5 dB in 1.5 dB steps

Table 2. DIGITAL I/O AND CLOCKING

Name	Pin	I / O	Functional Description
XTL_IN	2	I	24.576 MHz crystal or external oscillator input To complete the oscillator circuit use a fundamental mode crystal operating in parallel resonance and connect a 1MΩ resistor across pins 2 and 3. Choose the load capacitors (Figure 9, *C1, C2*) to suit the load capacitance required by the crystal (*e.g.* C1 = C2 = 33 pF for a 20 pF crystal. Assumes that each 'Input + trace' capacitance is 7 pF). This pin may also be used as the input for an external oscillator (24.576 MHz nominal) at standard logic levels (V_{IH}, V_{IL}). This pin is only used when the codec is in Primary mode. It may be left open (NC) for any Secondary mode.
XTL_OUT	3	O	24.576 MHz crystal output Used with XTAL_IN to configure a crystal oscillator. When the codec is used with an external oscillator this pin should be left open (NC). When the codec is configured in a Secondary mode this pin is not used and may be left open (NC).
SDATA_OUT	5	I	Input to codec This is the input for AC Link Output Frames from an AC '97 Digital Audio Controller to the LM4550 codec. These frames can contain both control data and DAC PCM audio data. This input is sampled by the LM4550 on the falling edge of BIT_CLK.
BIT_CLK	6	I/O	AC Link clock An OUTPUT when in Primary Codec mode. This pin provides a 12.288 MHz clock for the AC Link. The clock is derived (internally divided by two) from the 24.576 MHz signal at the crystal input (XTL_IN). This pin is an INPUT when the codec is configured in any of the Secondary Codec modes and would normally use the AC Link clock generated by a Primary Codec.

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Table 2. DIGITAL I/O AND CLOCKING (continued)

Name	Pin	I / O	Functional Description
SDATA_IN	8	O	Output from codec This is the output for AC Link Input Frames from the LM4550 codec to an AC '97 Digital Audio Controller. These frames can contain both codec status data and PCM audio data from the ADCs. The LM4550 clocks data from this output on the rising edge of BIT_CLK.
SYNC	10	I	AC Link frame marker and Warm Reset This input defines the boundaries of AC Link frames. Each frame lasts 256 periods of BIT_CLK. In normal operation SYNC is a 48 kHz positive pulse with a duty cycle of 6.25% (16/256). SYNC is sampled on the rising edge of BIT_CLK and the codec takes the first positive sample of SYNC as defining the start of a new AC Link frame. If a subsequent SYNC pulse occurs within 255 BIT_CLK periods of the frame start it will be ignored. SYNC is also used as an active high input to perform an (asynchronous) Warm Reset. Warm Reset is used to clear a power down state on the codec AC Link interface.
RESET#	11	I	Cold Reset This active low signal causes a hardware reset which returns the control registers and all internal circuits to their default conditions. RESET# must be used to initialize the LM4550 after Power On when the supplies have stabilized. Cold Reset also clears the codec from both ATE and Vendor test modes. In addition, while active, it switches the PC_BEEP mono input directly to both channels of the LINE_OUT stereo output.
ID0#	45	I	Codec Identity ID1# and ID0# determine the Codec Identity for multiple codec use. The Codec Identity configures the codec in either Primary or one of three Secondary Codec modes. These Identity pins are of inverted polarity relative to the Codec Identity bits ID1, ID0 (bits D15, D14) in the read-only Extended Audio ID register, 28h. If the ID0# pin (pin 45) is connected to ground then the ID0 bit (D14, reg 28h) will be set to “1”. Similarly, connection to DV_{DD} will set the ID0 bit to “0”. If left open (NC), ID0# is pulled high by an internal pull-up resistor. The Codec Identity bits are also used in the Chain-In Control register, 74h. See the register description and the CIN pin description for details.
ID1#	46	I	Codec Identity ID1# and ID0# determine the codec address for multiple codec use. The Codec Identity configures the codec in either Primary or one of three Secondary Codec modes. These Identity pins are of inverted polarity relative to the Codec Identity bits ID1, ID0 (bits D15, D14) in the read-only Extended Audio ID register, 28h. If the ID1# pin (pin 46) is connected to ground then the ID1 bit (D15, reg 28h) will be set to “1”. Similarly, connection to DV_{DD} will set the ID1 bit to “0”. If left open (NC), ID1# is pulled high by an internal pull-up resistor. The Codec Identity bits are also used in the Chain-In Control register, 74h. See the register description and the CIN pin description for details.
EAPD	47	O	External Amplifier Power Down control signal This output is set by the EAPD bit (bit D15) in the Powerdown Control/Status register, 26h. As with the other logic outputs, the output voltage is set by DV_{DD}. This pin is intended to be connected to the shutdown pin on an external power amplifier. For normal operation the default value of EAPD=0 will enable the external amplifier allowing an input on PC_BEEP to be heard during Cold Reset.
CIN	48	I	Chain In The codec can be instructed to disconnect its own SDATA_IN signal and instead pass the signal on CIN through to the SDATA_IN output pin. This is achieved by changing the value of the two LSBs of the Chain-In Control register (74h) so that they differ from the Codec Identity bits ID1, ID0. Those two LSBs default to the value of the Codec Identity bits following Cold Reset thereby disabling the Chain In feature. Chain In can also be disabled by reading the Codec Identity from the Extended Audio ID register (28h) and writing the value back into register 74h LSBs. The Codec Identity bits are determined by the input pins ID1#, ID0#. CIN can be left open (NC) provided that the chain feature is disabled. When the chain feature is used, CIN should always be driven. Either connect the SDATA_IN pin from another codec or else ground CIN to prevent the possibility of floating the SDATA_IN signal at the controller.

Table 3. POWER SUPPLIES AND REFERENCES

Name	Pin	I / O	Functional Description
AV_{DD}	25	I	Analog supply
AV_{SS}	26	I	Analog ground
DV_{DD1}	1	I	Digital supply
DV_{DD2}	9	I	Digital supply
DV_{SS1}	4	I	Digital ground
DV_{SS2}	7	I	Digital ground

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Table 3. POWER SUPPLIES AND REFERENCES (continued)

Name	Pin	I / O	Functional Description
V_{REF}	27	O	Nominal 2.2 V internal reference Not intended to sink or source current. Use short traces to bypass (3.3 µF, 0.1 µF) this pin to maximize codec performance. This pin must be tied to AV_{DD} with a 10 kΩ pull-up resistor.
V_{REF_OUT}	28	O	Nominal 2.2 V reference output Can source up to 5 mA of current and can be used to bias a microphone.

Table 4. 3D SOUND AND NO-CONNECTS (NC)

Name	Pin	I / O	Functional Description
3DP, 3DN	33,34	O	These pins are used to complete the National 3D Sound stereo enhancement circuit. Connect a 0.022 µF capacitor between pins 3DP and 3DN. National 3D Sound can be turned on and off via the 3D bit (bit D13) in the General Purpose register, 20h. National 3D Sound uses a fixed-depth type stereo enhancement circuit hence the 3D Control register, 22h is read-only and is not programmable. If National 3D Sound is not needed, these pins should be left open (NC).
NC	29, 30 31, 32 38, 42 43, 44	NC	These pins are not used and should be left open (NC). For second source applications these pins may be connected to a noise-free supply or ground (*e.g.* AV_{DD} or AV_{SS}), either directly or through a capacitor.

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Typical Performance Characteristics

ADC Noise Floor

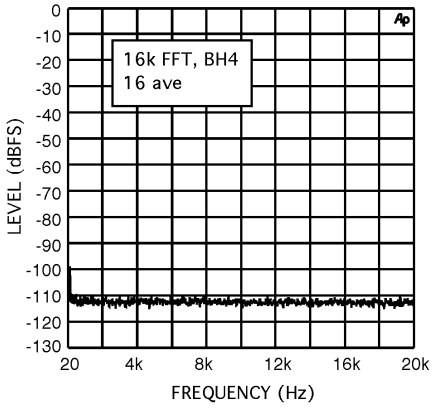

Figure 11.

DAC Noise Floor

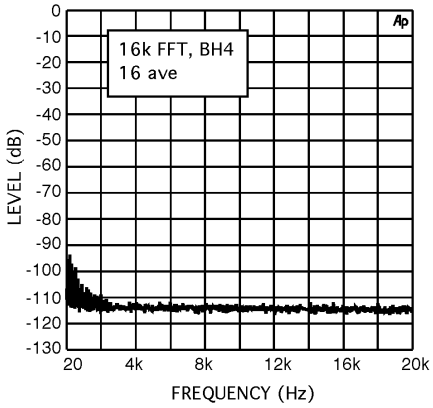

Figure 12.

ADC Frequency Response

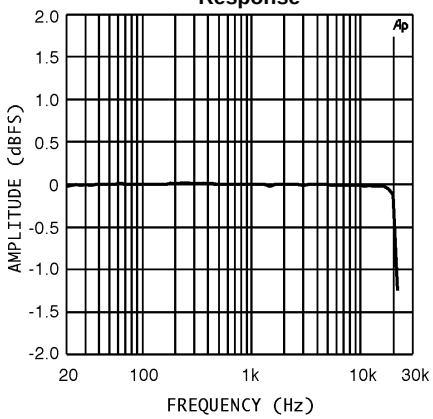

Figure 13.

DAC Frequency Response

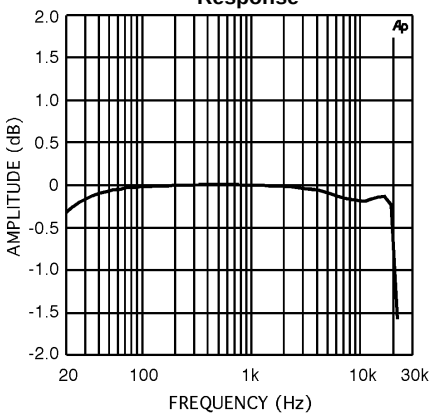

Figure 14.

Line Out Noise Floor (Analog Loopthrough)

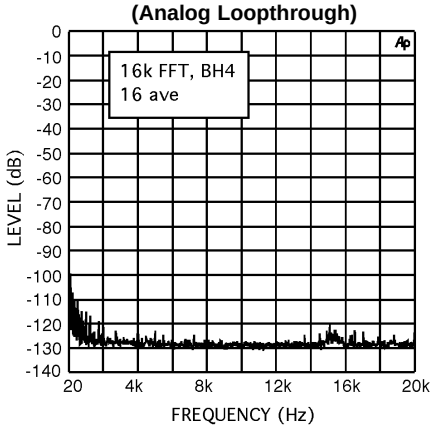

Figure 15.

Headphone Amplifier Noise Floor (Analog Loopthrough)

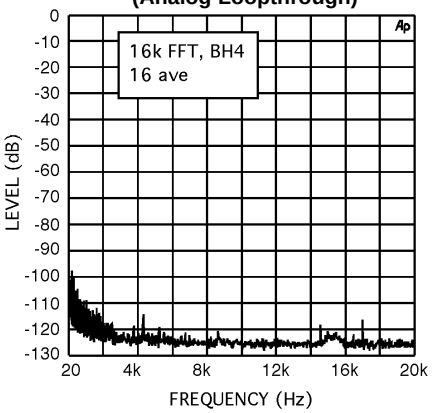

Figure 16.

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Typical Performance Characteristics (continued)

Headphone Amplifier THD+N vs Frequency

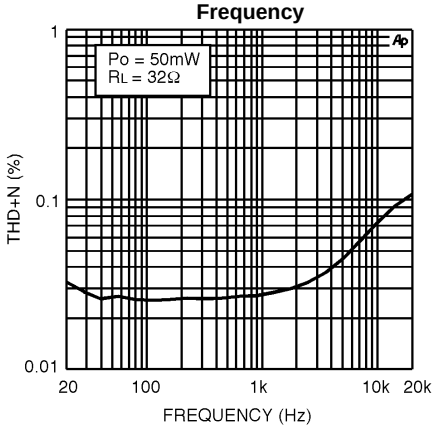

Figure 17.

Headphone Amplifier THD+N vs Output Power

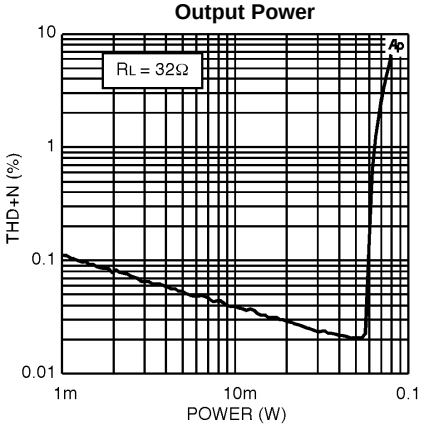

Figure 18.

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Table 5. LM4550 Register Map

	REG	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
	00h	Reset	X	0	0	0	1	1	0	1	0	1	0	1	0	0	0	0	0D50h
Output Volume	02h	Master Volume	Mute	X	X	ML4	ML3	ML2	ML1	ML0	X	X	X	MR4	MR3	MR2	MR1	MR0	8000h
	04h	Headphone Volume	Mute	X	X	ML4	ML3	ML2	ML1	ML0	X	X	X	MR4	MR3	MR2	MR1	MR0	8000h
	06h	Mono Volume	Mute	X	X	X	X	X	X	X	X	X	X	MM4	MM3	MM2	MM1	MM0	8000h
Input Volume	0Ah	PC_Beep Volume	Mute	X	X	X	X	X	X	X	X	X	X	PV3	PV2	PV1	PV0	X	0000h
	0Ch	Phone Volume	Mute	X	X	X	X	X	X	X	X	X	X	GN4	GN3	GN2	GN1	GN0	8008h
	0Eh	Mic Volume	Mute	X	X	X	X	X	X	X	X	20dB	X	GN4	GN3	GN2	GN1	GN0	8008h
	10h	Line In Volume	Mute	X	X	GL4	GL3	GL2	GL1	GL0	X	X	X	GR4	GR3	GR2	GR1	GR0	8808h
	12h	CD Volume	Mute	X	X	GL4	GL3	GL2	GL1	GL0	X	X	X	GR4	GR3	GR2	GR1	GR0	8808h
	14h	Video Volume	Mute	X	X	GL4	GL3	GL2	GL1	GL0	X	X	X	GR4	GR3	GR2	GR1	GR0	8808h
	16h	Aux Volume	Mute	X	X	GL4	GL3	GL2	GL1	GL0	X	X	X	GR4	GR3	GR2	GR1	GR0	8808h
	18h	PCM Out Volume	Mute	X	X	GL4	GL3	GL2	GL1	GL0	X	X	X	GR4	GR3	GR2	GR1	GR0	8808h
ADC Sources	1Ah	Record Select	X	X	X	X	X	SL2	SL1	SL0	X	X	X	X	X	SR2	SR1	SR0	0000h
	1Ch	Record Gain	Mute	X	X	X	GL3	GL2	GL1	GL0	X	X	X	X	GR3	GR2	GR1	GR0	8000h
	20h	General Purpose	POP	X	3D	X	X	X	MIX	MS	LPBK	X	X	X	X	X	X	X	0000h
	22h	3D Control (Read Only)	X	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0101h
X	24h	Reserved	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0000h
	26h	Powerdown Ctrl/Stat	EAPD	PR6	PR5	PR4	PR3	PR2	PR1	PR0	X	X	X	X	REF	ANL	DAC	ADC	000Xh
	28h	Extended Audio ID	ID1	ID0	X	X	X	X	AMAP	0	0	0	X	X	0	X	0	VRA	X201h
	2Ah	Extended Audio Control/Status	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	VRA	0000h
	2Ch	PCM DAC Rate	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	BB80h
	32h	PCM ADC Rate	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	BB80h
X	5Ah	Vendor Reserved 1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0000h
	74h	Chain-In Control	X	X	X	X	X	X	X	X	X	X	X	X	X	X	ID1	ID0	000Xh
X	7Ah	Vendor Reserved 2	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0000h
	7Ch	Vendor ID1	0	1	0	0	1	1	1	0	0	1	0	1	0	0	1	1	4E53h
	7Eh	Vendor ID2	0	1	0	0	0	0	1	1	0	1	0	1	0	0	0	0	4350h

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Functional Description

GENERAL

The LM4550 codec can mix, process and convert among analog (stereo and mono) and digital (AC Link format) inputs and outputs. There are four stereo and four mono analog inputs and two stereo and one mono analog outputs. A single codec supports data streaming on two input and two output channels of the AC Link digital interface simultaneously.

ADC INPUTS AND OUTPUTS

All four of the stereo analog inputs and three of the mono analog inputs can be selected for conversion by the 18-bit stereo ADC. Digital output from the left and right channel ADCs is always located in AC Link Input Frame slots 3 and 4 respectively. Input level to either ADC channel can be muted or adjusted from the Record Gain register, 1Ch. Adjustments are in 1.5 dB steps over a gain range of 0 dB to +22.5 dB and both channels mute together (D15). Input selection for the ADC is through the Record Select Mux controlled from the Record Select register, 1Ah, together with microphone selection controlled by the MS bit (D8) in the General Purpose register, 20h. One of the stereo inputs, CD_IN, uses a quasi-differential 3-pin interface where both stereo channel inputs are referenced to the third pin, CD_GND. CD_GND should be AC coupled to the source ground and provides common-mode feedback to cancel ground noise. It is not a DC ground. The other three stereo inputs, LINE_IN, AUX and VIDEO are 2-pin interfaces, single-ended for each stereo channel, with analog ground (AV_{SS}) as the signal reference. Either of the two mono microphone inputs can be muxed to a programmable boost amplifier before selection for either channel of the ADC. The Microphone Mux is controlled by the Microphone Selection (MS) bit (D8) in the General Purpose register (20h) and the 20 dB programmable boost is enabled by the 20dB bit (D6) in register 0Eh. The mono PHONE input may also be selected for either ADC channel.

ANALOG MIXING: MIX1

Five analog inputs are available for mixing at the stereo mixer, MIX1 – all four stereo and one mono, namely the microphone input selected by MS (D8, reg 20h). Digital input to the codec can be directed to either MIX1 or to MIX2 after conversion by the 18-bit stereo DAC and level adjustment by the PCM Out Volume control register (18h). Each input to MIX1 may be muted or level adjusted using the appropriate Mixer Input Volume Register: Mic Volume (0Eh), Line_In Volume (10h), CD Volume (12h), Video Volume (14h), Aux Volume (16h) and PCM Out Volume (18h). The mono microphone input is mixed equally into left and right stereo channels but stereo mixing is orthogonal, *i.e.* left channels are only mixed with other left channels and right with right. The left and right amplitudes of any stereo input may be adjusted independently however mute for a stereo input acts on both left and right channels.

DAC MIXING AND 3D PROCESSING

Control of routing the DAC output to MIX1 or MIX2 is by the POP bit (D15) in the General Purpose register, 20h. If MIX1 is selected (default, POP=0) then the DAC output is available for processing by the National 3D Sound circuitry. If MIX2 is selected, the DAC output will bypass the 3D processing. This allows analog inputs to be enhanced by the analog 3D Sound circuitry prior to mixing with digital audio. The digital audio may then use alternative digital 3D enhancements. National 3D Sound circuitry is enabled by the 3D bit (D13) in the General Purpose register, 20h, and is a fixed depth implementation. The 3D Control register, 22h, is therefore not programmable (read-only). The 3D Sound circuitry defaults to disabled after reset.

ANALOG MIXING: MIX2

MIX2 combines the output of MIX1 (Stereo Mix 3D) with the two mono analog inputs, PHONE and PC_BEEP, these each level-adjusted by the input control registers Phone Volume (0Ch) and PC_Beep Volume (0Ah) respectively. If selected by the POP bit (D15, reg 20h), the DAC output is also summed into MIX2.

STEREO MIX

The output of MIX2 is the signal, Stereo Mix. Stereo Mix is used to drive both the Headphone output (HP_OUT) and the Line output (LINE_OUT) and can also be selected as the input to the ADC at the Record Select Mux. In addition, the two channels of Stereo Mix are summed to form a mono signal (Mono Mix) also selectable at the Record Select Mux as an input to either channel of the ADC.

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STEREO OUTPUTS

The output volume from LINE_OUT and HP_OUT can be muted or adjusted by 0 dB to 45 dB in nominal 3 dB steps under the control of the output volume registers Master Volume (02h) and Headphone Volume (04h) respectively. As with the input volume registers, adjustments to the levels of the two stereo channels can be made independently but both left and right channels share a mute bit (D15).

MONO OUTPUT

The mono output (MONO_OUT) is driven by one of two signals selected by the MIX bit (D9) in the General Purpose register, 20h. The signal selected by default (MIX = 0) is the mono summation of the two channels of Stereo Mix 3D, the stereo output of the mixer MIX1. Setting the control bit MIX = 1, selects a microphone input, MIC1 or MIC2. The choice of microphone is controlled by the Microphone Select (MS) bit (D8) also in the General Purpose register, 20h.

ANALOG LOOPTHROUGH AND DIGITAL LOOPBACK

Analog Loopthrough refers to an all-analog signal path from an analog input through the mixers to an analog output. Digital Loopback refers to a mixed-mode analog and digital signal path from an analog input through the ADC, looped-back (LPBK bit – D7, 20h) through the DAC and mixers to an analog output.

RESETS

COLD RESET is performed when RESET# (pin 11) is pulled low for > 1 µs. It is a complete reset. All registers and internal circuits are reset to their default state. It is the only reset which clears the ATE and Vendor Test Modes.

WARM RESET is performed when SYNC (pin 10) is held high for > 1 µs and the codec AC Link digital interface is in powerdown (PR4 = 1, Powerdown Control / Status register, 26h). It is used to clear PR4 and power up the AC Link digital interface but otherwise does not change the contents of any registers nor reset any internal circuitry.

REGISTER RESET is performed when any value is written to the RESET register, 00h. It resets all registers to their default state and will modify circuit configurations accordingly but does not reset any other internal circuits.

AC Link Serial Interface Protocol

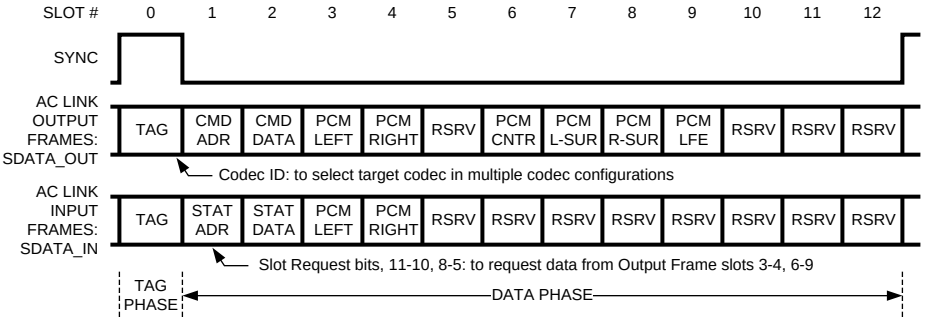

Figure 19. AC Link Bidirectional Audio Frame

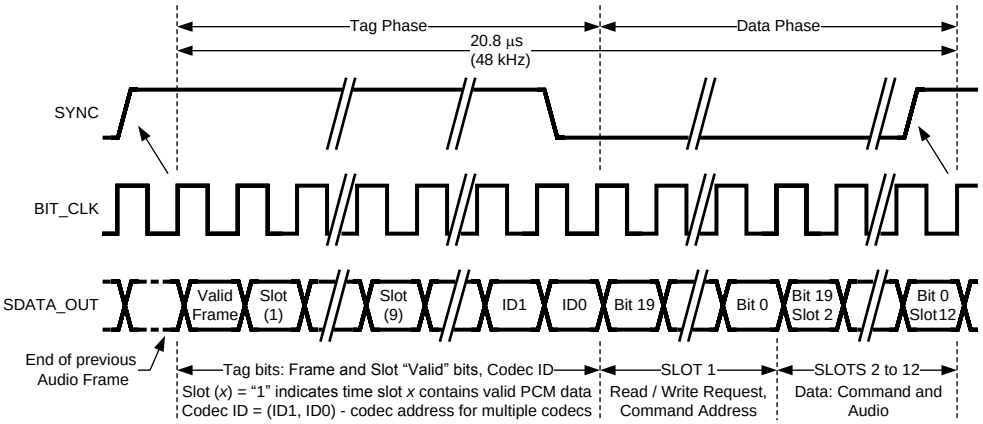

Figure 20. AC Link Output Frame

AC LINK OUTPUT FRAME: SDATA_OUT, CONTROLLER OUTPUT TO LM4550 INPUT

The AC Link Output Frame carries control and PCM data to the LM4550 control registers and stereo DAC. Output Frames are carried on the SDATA_OUT signal which is an output from the AC '97 Digital Controller and an input to the LM4550 codec. As shown in Figure 19, Output Frames are constructed from thirteen time slots: one Tag Slot followed by twelve Data Slots. Each Frame consists of 256 bits with each of the twelve Data Slots containing 20 bits. Input and Output Frames are aligned to the same SYNC transition. Note that the LM4550 only accepts data in eight of the twelve Data Slots and, since it is a two channel codec only in 4 simultaneously – 2 for control, one each for PCM data to the left and right channel DACs. Data-Slot to DAC mappings are tied to the codec mode selected by the Identity pins ID1#, ID0# and are given in Table 19.

A new Output Frame is signaled with a low-to-high transition of SYNC. SYNC should be clocked from the controller on a rising edge of BIT_CLK and, as shown in Figure 20 and Figure 21, the first tag bit in the Frame ("Valid Frame") should be clocked from the controller by the next rising edge of BIT_CLK and sampled by the LM4550 on the following falling edge. The AC '97 Controller should always clock data to SDATA_OUT on a rising edge of BIT_CLK and the LM4550 always samples SDATA_OUT on the next falling edge. SYNC is sampled with the rising edge of BIT_CLK.

The LM4550 checks each Frame to ensure 256 bits are received. If a new Frame is detected (a low-to-high transition on SYNC) before 256 bits are received from the old Frame then the new Frame is ignored *i.e.* the data on SDATA_OUT is discarded until a valid new Frame is detected.

The LM4550 expects to receive data MSB first, in an MSB justified format.

SDATA_OUT: Slot 0 – Tag Phase

The first bit of Slot 0 is designated the "Valid Frame" bit. If this bit is 1, it indicates that the current Output Frame contains at least one slot of valid data and the LM4550 will check further tag bits for valid data in the expected Data Slots. With the codec in Primary mode, a controller will indicate valid data in a slot by setting the associated tag bit equal to 1. Since it is a two channel codec the LM4550 can only receive data from four slots in a given frame and so only checks the valid-data bits for 4 slots. In Primary mode these tag bits are for: slot 1 (Command Address), slot 2 (Command Data), slot 3 (PCM data for left DAC) and slot 4 (PCM data for right DAC).

The last two bits in the Tag contain the Codec ID used to select the target codec to receive the frame in multiple codec systems. When the frame is being sent to a codec in one of the Secondary modes the controller does not use bits 14 and 13 to indicate valid Command Address and Data in slots 1 and 2. Instead, this role is performed by the Codec ID bits – operation of the Extended AC Link assumes that the controller would not access a secondary codec unless it was providing valid Command Address and/or Data. When in one of the secondary modes the LM4550 only checks the tag bits for the Codec ID and for valid data in the two audio data slots: slots 3 & 4 for Secondary mode 1, slots 7 & 8 for mode 2 and slots 6 & 9 for mode 3.

When sending an Output Frame to a Secondary mode codec, a controller should set tag bits 14 and 13 to zero.

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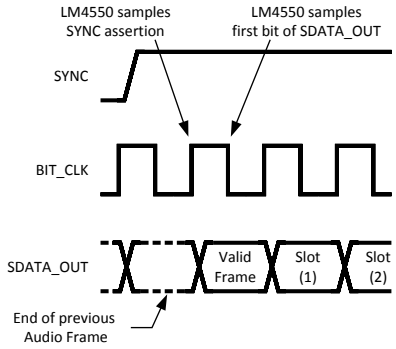

Figure 21. Start of AC Link Output Frame

Table 6. SLOT 0, OUTPUT FRAME

Bit	Description	Comment	
15	Valid Frame	1 =	Valid data in at least one slot.
14	Control register address	1 =	Valid Control Address in Slot 1 (Primary codec only)
13	Control register data	1 =	Valid Control Data in Slot 2 (Primary codec only)
12	Left DAC data in Slot 3	1 =	Valid PCM Data in Slot 3 (Primary & Secondary 1 modes; Left Channel audio)
11	Right DAC data in Slot 4	1 =	Valid PCM Data in Slot 4 (Primary & Secondary 1 modes; Right Channel audio)
10	Not Used	Controller should stuff this slot with “0”s	
9	Left DAC data in Slot 6	1 =	Valid PCM Data in Slot 6 (Secondary 3 mode; Center Channel audio)
8	Left DAC data in Slot 7	1 =	Valid PCM Data in Slot 7 (Secondary 2 mode; Left Surround Channel audio)
7	Right DAC data in Slot 8	1 =	Valid PCM Data in Slot 8 (Secondary 2 mode; Right Surround Channel audio)
6	Right DAC data in Slot 9	1 =	Valid PCM Data in Slot 9 (Secondary 3 mode; LFE Channel audio)
5:2	Not Used	Controller should stuff these slots with “0”s	
1,0	Codec ID (ID1, ID0)	The Codec ID (Table 19) selects the target codec in a multi-codec system to receive the control address and data carried in the Output Frame	

SDATA_OUT: Slot 1 – Read/Write, Control Address

Slot 1 is used by a controller to indicate both the address of a target register in the LM4550 and whether the access operation is a register read or register write. The MSB of slot 1 (bit 19) is set to 1 to indicate that the current access operation is 'read'. Bits 18 through 12 are used to specify the 7-bit register address of the read or write operation. The least significant twelve bits are reserved and should be stuffed with zeros by the AC '97 controller.

Table 7. SLOT 1, OUTPUT FRAME

Bits	Description	Comment
19	Read/Write	1 = Read 0 = Write
18:12	Register Address	Identifies the Status/Command register for read/write
11:0	Reserved	Controller should set to "0"

SDATA_OUT: Slot 2 – Control Data

Slot 2 is used to transmit 16-bit control data to the LM4550 when the access operation is 'write'. The least significant four bits should be stuffed with zeros by the AC '97 controller. If the access operation is a register read, the entire slot, bits 19 through 0 should be stuffed with zeros.

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Table 8. SLOT 2, OUTPUT FRAME

Bits	Description	Comment
19:4	Control Register Write Data	Controller should stuff with zeros if operation is “read”
3:0	Reserved	Set to "0"

SDATA_OUT: Slots 3 & 4 – PCM Playback Left/Right Channels

Slots 3 and 4 are 20-bit fields used to transmit PCM data to the left and right channels of the stereo DAC when the codec is in Primary mode or Secondary mode 1. Any unused bits should be stuffed with zeros. The LM4550 DACs have 18-bit resolution and will therefore use the 18 MSBs of the 20-bit PCM data (MSB justified). The AC '97 Rev 2.1 specification allocates the Left channel of 5.1 Audio to slot 3 and the Right channel to slot 4.

Table 9. SLOTS 3 & 4, OUTPUT FRAME

Bits	Description	Comment
19:0	PCM Audio Data (Left /Right Channels)	Slots used to stream data to DAC when codec is in Primary or Secondary 1 modes. Set unused bits to "0"

SDATA_OUT: Slots 7 & 8 – PCM Playback Left/Right Surround

Slots 7 and 8 are 20-bit fields used to transmit PCM data to the left and right channels of the stereo DAC when the codec is in Secondary mode 2. Any unused bits should be stuffed with zeros. The LM4550 DACs have 18-bit resolution and will therefore use the 18 MSBs of the 20-bit PCM data (MSB justified). The AC '97 Rev 2.1 specification allocates the Left Surround channel of 5.1 Audio to slot 7 and the Right Surround channel to slot 8.

Table 10. SLOTS 7 & 8, OUTPUT FRAME

Bits	Description	Comment
19:0	PCM Audio Data (Left/Right Surround)	Slots used to stream data to DAC when codec is in Secondary 2 mode. Set unused bits to "0"

SDATA_OUT: Slots 6 & 9 – PCM Playback (Center/LFE)

Slots 6 and 9 are 20-bit fields used to transmit PCM data to the left and right channels of the stereo DAC when the codec is in Secondary mode 3. Any unused bits should be stuffed with zeros. The LM4550 DACs have 18-bit resolution and will therefore use the 18 MSBs of the 20-bit PCM data (MSB justified). The AC '97 Rev 2.1 specification allocates the Center channel of 5.1 Audio to slot 6 and the LFE (Low Frequency Enhancement) channel to slot 9.

Table 11. SLOTS 6 & 9, OUTPUT FRAME

Bits	Description	Comment
19:0	PCM Audio Data (Center/ LFE Surround)	Slots used to stream data to DAC when codec is in Secondary 3 mode. Set unused bits to "0"

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SDATA_OUT: Slots 5, 10, 11, 12 – Reserved

These slots are not used by the LM4550 and should all be stuffed with zeros by the AC '97 Controller.

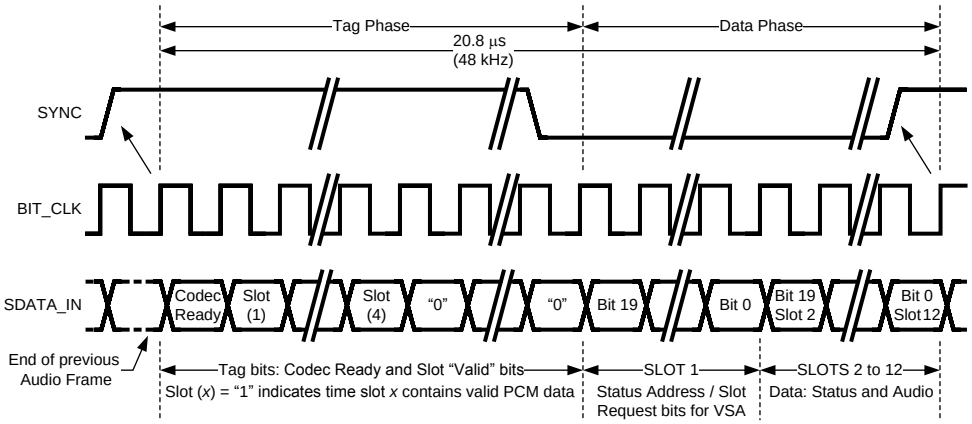

Figure 22. AC Link Input Frame

AC LINK INPUT FRAME: SDATA_IN, CONTROLLER INPUT FROM LM4550 OUTPUT

The AC Link Input Frame contains status and PCM data from the LM4550 control registers and stereo ADC. Input Frames are carried on the SDATA_IN signal which is an input to the AC '97 Digital Audio Controller and an output from the LM4550 codec. As shown in Figure 19, Input Frames are constructed from thirteen time slots: one Tag Slot followed by twelve Data Slots. The Tag Slot, Slot 0, contains 16 bits of which 5 are used by the LM4550. One is used to indicate that the AC Link interface is fully operational and the other 4 to indicate the validity of the data in the four of the twelve following Data Slots that are used by the LM4550. Each Frame consists of 256 bits with each of the twelve data slots containing 20 bits.

A new Input Frame is signaled with a low-to-high transition of SYNC. SYNC should be clocked from the controller on a rising edge of BIT_CLK and, as shown in Figure 22 and Figure 23, the first tag bit in the Frame ("Codec Ready") is clocked from the LM4550 by the next rising edge of BIT_CLK. The LM4550 always clocks data to SDATA_IN on a rising edge of BIT_CLK and the controller is expected to sample SDATA_IN on the next falling edge. The LM4550 samples SYNC on the rising edge of BIT_CLK.

Input and Output Frames are aligned to the same SYNC transition.

The LM4550 checks each Frame to ensure 256 bits are received. If a new Frame is detected (a low-to-high transition on SYNC) before 256 bits are received from an old Frame then the new Frame is ignored *i.e.* no valid data is sent on SDATA_IN until a valid new Frame is detected.

The LM4550 transmits data MSB first, in an MSB justified format. All reserved bits and slots are stuffed with "0"s by the LM4550.

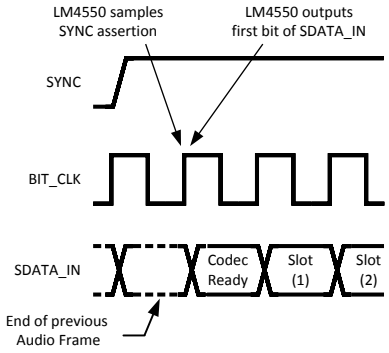

Figure 23. Start of AC Link Input Frame

SDATA_IN: Slot 0 – Codec/Slot Status Bits

The first bit (bit 15, “Codec Ready”) of slot 0 in the AC Link Input Frame indicates when the codec's AC Link digital interface and its status/control registers are fully operational. The digital controller is then able to read the LSBs from the Powerdown Control/Stat register (26h) to determine the status of the four main analog subsections. It is important to check the status of these subsections after Initialization, Cold Reset or the use of the powerdown modes in order to minimize the risk of distorting analog signals passed before the subsections are ready.

The 4 bits 14, 13, 12 and 11 indicate that the data in slots 1, 2, 3 and 4, respectively, are valid.

Table 12. SLOT 0, INPUT FRAME

Bit	Description	Comment	
15	Codec Ready Bit	1 =	AC Link Interface Ready
14	Slot 1 data valid	1 =	Valid Status Address or Slot Request
13	Slot 2 data valid	1 =	Valid Status Data
12	Slot 3 data valid	1 =	Valid PCM Data (Left ADC)
11	Slot 4 data valid	1 =	Valid PCM Data (Right ADC)

SDATA_IN: Slot 1 – Status Address / Slot Request Bits

This slot echoes (in bits 18 – 12) the 7-bit address of the codec control/status register received from the controller as part of a read-request in the previous frame. If no read-request was received, the codec stuffs these bits with zeros.

The 6 bits 11, 10, 8 – 5 are Slot Request bits that support the Variable Rate Audio (VRA) capabilities of the LM4550. Only two are used simultaneously. If the codec is in Primary mode or Secondary mode 1, then the left and right channels of the DAC take PCM data from slots 3 and 4 in the Output Frame respectively (see Table 19). The codec uses bits 11 and 10 to request DAC data from these two slots. If bits 11 and 10 are set to 0, the controller should respond with valid PCM data in slots 3 and 4 of the next Output Frame. If bits 11 and 10 are set to 1, the controller should not send data. Similarly, if the codec is in Secondary mode 2, bits 7 and 6 are used to request data from slots 7 and 8 in the Output Frame. If in Secondary mode 3, bits 8 and 5 request data from slots 6 and 9.

The codec has full control of the slot request bits. By default, data is requested in every frame, corresponding to a sample rate equal to the frame rate (SYNC frequency) – 48 kHz when XTAL_IN = 24.576 MHz. To send samples at a rate below the frame rate, a controller should set VRA = 1 (bit 0 in the Extended Audio Control/Status register, 2Ah) and program the desired rate into the PCM DAC Rate register, 2Ch. Both DAC channels operate at the same sample rate. Values for common sample rates are given in the Register Description section (Sample Rate Control Registers, 2Ch, 32h) but any rate between 4 kHz and 48 kHz (to a resolution of 1 Hz) is supported. Slot Requests from the LM4550 are issued completely deterministically. For example if a sample rate of 8000 Hz is programmed into 2Ch then the LM4550 will always issue a slot request in every sixth frame. A frequency of 9600 Hz will result in a request every fifth frame while a frequency of 8800 Hz will cause slot requests to be spaced alternately five and six frames apart. This determinism makes it easy to plan task scheduling on a system controller and simplifies application software development.

The LM4550 will ignore data in Output Frame slots that do not follow an Input Frame with a Slot Request. For example, if the LM4550 is expecting data at a 8000 Hz rate yet the AC '97 Digital Audio Controller continues to send data at 48000 Hz, then only those one-in-six audio samples that follow a Slot Request will be used by the DAC. The rest will be discarded.

Bits 9, 4, 3, and 2 are request bits for slots not used by the LM4550 and are stuffed with zeros. Bits 1 and 0 are reserved and are also stuffed with zeros.

Table 13. SLOT 1, INPUT FRAME

Bits	Description	Comment
19	Reserved	Stuffed with "0" by LM4550
18:12	Status Register Index	Echo of the requested Status Register address.

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Table 13. SLOT 1, INPUT FRAME (continued)

Bits	Description	Comment	
11	Slot 3 Request bit (PCM Left Audio)	0 =	Controller should send valid data in Slot 3 of the next Output Frame.
		1 =	Controller should not send Slot 3 data.
10	Slot 4 Request bit (PCM Right Audio)	0 =	Controller should send valid data in Slot 4 of the next Output Frame.
		1 =	Controller should not send Slot 4 data.
9	Slot 5 Request bit	Unused - set to "0" by LM4550	
8	Slot 6 Request bit (PCM Center)	0 =	Controller should send valid data in Slot 6 of the next Output Frame.
		1 =	Controller should not send Slot 6 data.
7	Slot 7 Request bit (PCM Left Surround)	0 =	Controller should send valid Slot 7 data in the next Output Frame.
		1 =	Controller should not send Slot 7 data.
6	Slot 8 Request bit (PCM Right Surround)	0 =	Controller should send valid data in Slot 8 of next Output Frame.
		1 =	Controller should not send Slot 8 data.
5	Slot 9 Request bit (PCM LFE)	0 =	Controller should send valid data in Slot 9 of next Output Frame.
		1 =	Controller should not send Slot 9 data.
4:2	Unused Slot Request bits	Stuffed with "0"s by LM4550	
1,0	Reserved	Stuffed with "0"s by LM4550	

SDATA_IN: Slot 2 – Status Data

This slot returns 16-bit status data read from a codec control/status register. The codec sends the data in the frame following a read-request by the controller (bit 15, slot 1 of the Output Frame). If no read-request was made in the previous frame the codec will stuff this slot with zeros.

Table 14. SLOT 2, INPUT FRAME

Bits	Description	Comment
19:4	Status Data	Data read from a codec control/status register. Stuffed with “0”s if no read-request in previous frame.
3:0	Reserved	Stuffed with "0"s by LM4550

SDATA_IN: Slot 3 – PCM Record Left Channel

This slot contains sampled data from the left channel of the stereo ADC. The signal to be digitized is selected using the Record Select register (1Ah) and subsequently routed through the Record Select Mux and the Record Gain amplifier to the ADC.

This is a 20-bit slot and the digitized 18-bit PCM data is transmitted in an MSB justified format. The remaining 2 LSBs are stuffed with zeros.

Table 15. SLOT 3, INPUT FRAME

Bits	Description	Comment
19:2	PCM Record Left Channel data	18-bit PCM audio sample from left ADC
1:0	Reserved	Stuffed with "0"s by LM4550

SDATA_IN: Slot 4 – PCM Record Right Channel

This slot contains sampled data from the right channel of the stereo ADC. The signal to be digitized is selected using the Record Select register (1Ah) and subsequently routed through the Record Select Mux and the Record Gain amplifier to the ADC.

This is a 20-bit slot and the digitized 18-bit PCM data is transmitted in an MSB justified format. The remaining 2 LSBs are stuffed with zeros.

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Table 16. SLOT 4, INPUT FRAME

Bits	Description	Comment
19:2	PCM Record Right Channel data	18-bit PCM audio sample from right ADC
1:0	Reserved	Stuffed with "0"s by LM4550

SDATA_IN: Slots 5 to 12 – Reserved

Slots 5 – 12 of the AC Link Input Frame are not used for data by the LM4550 and are always stuffed with zeros.

Register Descriptions

Default settings are indicated by *.

RESET REGISTER (00h)

Writing any value to this register causes a Register Reset which changes all registers back to their default values. If a read is performed on this register, the LM4550 will return a value of 0D50h. This value can be interpreted in accordance with the AC '97 specification to indicate that National 3D Sound is implemented, 18-bit data is supported for both the ADCs and DACs, and that headphone output is supported.

MASTER VOLUME REGISTER (02h)

This output register allows the output level from either channel of the stereo LINE_OUT to be muted or attenuated over the range 0 dB – 46.5 dB in nominal 1.5 dB steps. There are 5 bits of volume control for each channel and both stereo channels can be individually attenuated. The mute bit (D15) acts simultaneously on both stereo channels of LINE_OUT.

Mute	Mx4:Mx0	Function
0	0 0000	0dB attenuation
0	1 1111	46.5dB attenuation
1	X XXXX	*mute
Default: 8000h		

HEADPHONE VOLUME REGISTER (04h)

This output register allows the level from both channels of HP_OUT to be muted or individually attenuated over the range 0 dB – 46.5 dB in nominal 1.5 dB steps. There are 5 bits of volume control for each channel plus one mute bit. The mute bit (D15) acts on both channels. Operation of this register and HP_OUT matches that of the Master Volume register and the LINE_OUT output.

MONO VOLUME REGISTER (06h)

This output register allows the level from MONO_OUT to be muted or attenuated over the range 0 dB – 46.5 dB in nominal 1.5 dB steps. There are 5 bits of volume control and one mute bit (D15).

Mute	MM4:MM0	Function
0	0 0000	0dB attenuation
0	1 1111	46.5dB attenuation
1	X XXXX	*mute
Default: 8000h		

PC BEEP VOLUME REGISTER (0Ah)

This input register adjusts the level of the mono PC_BEEP input to the stereo mixer MIX2 where it is summed equally into both channels of the Stereo Mix signal. PC_BEEP can be both muted and attenuated over a range of 0 dB to 45 dB in nominal 3 dB steps. Note that the default setting for the PC_Beep Volume register is 0 dB attenuation rather than mute.

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Mute	PV3:PV0	Function
0	0000	*0dB attenuation
0	1111	45dB attenuation
1	XXXX	mute
Default: 0000h		

MIXER INPUT VOLUME REGISTERS (Index 0Ch – 18h)

These input registers adjust the volume levels into the stereo mixers MIX1 and MIX2. Each channel may be adjusted over a range of +12dB gain to 34.5dB attenuation in 1.5dB steps. For stereo ports, volumes of the left and right channels can be independently adjusted. Muting a given port is accomplished by setting the MSB to 1. Setting the MSB to 1 for stereo ports mutes both the left and right channels. The Mic Volume register (0Eh) controls an additional 20dB boost for the selected microphone input by setting the 20dB bit (bit D6).

Mute	Gx4:Gx0	Function
0	0 0000	+12dB gain
0	0 1000	0dB gain
0	1 1111	34.5dB attenuation
1	X XXXX	*mute
Default:	8008h (mono registers) 8808h (stereo registers)	

RECORD SELECT REGISTER (1Ah)

This register independently controls the sources for the right and left channels of the stereo ADC. The default value of 0000h corresponds to selecting the (mono) Mic input for both channels.

SL2:SL0	Source for Left Channel ADC	
0		*Mic input
1		CD input (L)
2		VIDEO input (L)
3		AUX input (L)
4		LINE_IN input (L)
5		Stereo Mix (L)
6		Mono Mix
7		PHONE input

SR2:SR0	Source for Right Channel ADC	
0		*Mic input
1		CD input (R)
2		VIDEO input (R)
3		AUX input (R)
4		LINE_IN input (R)
5		Stereo Mix (R)
6		Mono Mix
7		PHONE input

Default: 0000h

RECORD GAIN REGISTER (1Ch)

This register controls the input levels for both channels of the stereo ADC. The inputs come from the Record Select Mux and are selected via the Record Select Control register, 1Ah. The gain of each channel can be individually programmed from 0dB to +22.5dB in 1.5dB steps. Both channels can also be muted by setting the MSB to 1.

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Table 17. Record Gain Register (1Ch)

Mute	Gx3:Gx0	Function
0	1111	22.5dB gain
0	0000	0dB gain
1	XXXX	*mute
Default: 8000h		

GENERAL PURPOSE REGISTER (20h)

This register controls many miscellaneous functions implemented on the LM4550. The miscellaneous control bits include POP which allows the DAC output to bypass the National 3D Sound circuitry, 3D which enables or disables the National 3D Sound circuitry, MIX which selects the MONO_OUT source, MS which controls the Microphone Selection mux and LPBK which connects the output of the stereo ADC to the input of the stereo DAC. LPBK provides a mixed-mode analog – digital – analog loopback path between analog inputs and analog outputs.

BIT	Function		
POP	PCM Out Path:	*0 =	3D allowed
		1 =	3D bypassed
3D	National 3D Sound:	*0 =	off
		1 =	on
MIX	Mono output select:	*0 =	Mix
		1 =	Mic
MS	Mic select:	*0 =	MIC1
		1 =	MIC2
LPBK	ADC/DAC Loopback:	*0 =	No Loopback
		1 =	Loopback
Default: 0000h			

3D CONTROL REGISTER (22h)

This read-only (0101h) register indicates, in accordance with the AC '97 Rev 2.1 Specification, the fixed depth and center characteristics of the National 3D Sound stereo enhancement.

POWERDOWN CONTROL / STATUS REGISTER (26h)

This read/write register is used both to monitor subsystem readiness and also to program the LM4550 powerdown states. The 4 LSBs indicate status and the 8 MSBs control powerdown.

The 4 LSBs of this register indicate the status of the 4 audio subsections of the codec: Reference voltage, Analog mixers and amplifiers, DAC section, ADC section. When the "Codec Ready" indicator bit in the AC Link Input Frame (SDATA_IN: slot 0, bit 15) is a "1", it indicates that the AC Link and AC '97 registers are in a fully operational state and that control and status information can be transferred. It does not indicate that the codec is ready to send or receive audio PCM data or to pass signals through the analog I/O and mixers. To determine that readiness, the Controller must check that the 4 LSBs of this register are set to “1” indicating that the appropriate audio subsections are ready.

The powerdown bits PR0 – PR6 control internal subsections of the codec. They are implemented in compliance with AC '97 Rev 2.1 to support the standard device power management states D0 – D3 as defined in the ACPI and PCI Bus Power Management specification.

PR0 controls the powerdown state of the ADC and associated sampling rate conversion circuitry. PR1 controls powerdown for the DAC and the DAC sampling rate conversion circuitry. PR2 powers down the mixer circuits (MIX1, MIX2, National 3D Sound, Mono Out, Line Out). PR3 powers down V_{REF} in addition to all the same mixer circuits as PR2. PR4 powers down the AC Link digital interface – see Figure 24 for signal powerdown timing. PR5 disables internal clocks. PR6 powers down the Headphone amplifier. EAPD controls the External Amplifier PowerDown bit.

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BIT#	BIT	Function: Status	
0	ADC	1 =	ADC section ready to transmit data
1	DAC	1 =	DAC section ready to accept data
2	ANL	1 =	Analog mixers ready
3	REF	1 =	V_{REF} is up to nominal level

BIT#	BIT	Function: Powerdown	
8	PR0	1 =	Powerdown ADCs and Record Select Mux
9	PR1	1 =	Powerdown DACs
10	PR2	1 =	Powerdown Analog Mixer (V_{REF} still on)
11	PR3	1 =	Powerdown Analog Mixer (V_{REF} off)
12	PR4	1 =	Powerdown AC Link digital interface (BIT_CLK off)
13	PR5	1 =	Disable Internal Clock
14	PR6	1 =	Powerdown Headphone Amplifier
15	EAPD	External Amplifier PowerDown	
		*0 =	Set EAPD Pin to 0 (pin 47)

Default: 000Xh

EXTENDED AUDIO ID REGISTER (28h)

This read-only (X201h) register identifies which AC '97 Extended Audio features are supported. The LM4550 features AMAP (Slot/DAC mappings based on Codec Identity), VRA (Variable Rate Audio) and ID1, ID0, the Codec Identity bits used to support multi-codec systems. AMAP is indicated by a "1" in bit 9, VRA is indicated by a "1" in bit 0. The two MSBs, ID1 and ID0, show the current Codec Identity as defined by the Identity pins ID1#, ID0#. Note that the external logic connections to ID1#, ID0# (pins 46 and 45) are inverse in polarity to the value of the Codec Identity (ID1, ID0) held in bits D15, D14. The AMAP Slot/DAC mappings are given in Table 19 in the Multiple Codec section. Codec mode selections are shown in the table below.

Pin 46 (ID1#)	Pin 45 (ID0#)	D15,28h (ID1)	D14,28h (ID0)	Codec Identity Mode
NC/DV_{DD}	NC/DV_{DD}	0	0	Primary
NC/DV_{DD}	GND	0	1	Secondary 1
GND	NC/DV_{DD}	1	0	Secondary 2
GND	GND	1	1	Secondary 3

EXTENDED AUDIO STATUS/CONTROL REGISTER (2Ah)

This read/write register provides status and control of the variable sample rate capabilities in the LM4550. Setting the LSB of this register to "1" enables Variable Rate Audio (VRA) mode and allows DAC and ADC sample rates to be programmed via registers 2Ch and 32h respectively.

BIT	Function	
VRA	*0 =	VRA off (Frame-rate sampling)
	1 =	VRA on
Default: 0000h		

SAMPLE RATE CONTROL REGISTERS (2Ch, 32h)

These read/write registers are used to set the sample rate for the left and right channels of the DAC (PCM DAC Rate, 2Ch) and the ADC (PCM ADC Rate, 32h). When Variable Rate Audio is enabled via bit 0 of the Extended Audio Control/Status register (2Ah), the sample rates can be programmed, in 1 Hz increments, to be any value from 4 kHz to 48 kHz. The value required is the hexadecimal representation of the desired sample rate, *e.g.* 8000_{10} = 1F40h. Below is a list of the most common sample rates and the corresponding register (hex) values.

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Table 18. Common Sample Rates

SR15:SR0	Sample Rate (Hz)
1F40h	8000
2B11h	11025
3E80h	16000
5622h	22050
AC44h	44100
*BB80h	*48000

CHAIN-IN CONTROL REGISTER (74h)

This read/write register is only needed when using the Chain In feature. This feature goes beyond the AC '97 specification and is not required for standard AC Link operation. The two LSBs of this register default to the Codec Identity (ID1, ID0) after reset. This default state corresponds to standard AC Link operation where the output of codec pin 8 (SDATA_IN) carries the AC Link Input Frames back to the controller from the codec.

If the two LSBs differ from the Codec Identity (register 28h describes the Codec Identity), then the signal present at CIN (pin 48) is switched through to the SDATA_IN (pin 8) output. In this fashion, Secondary codecs can be chained together by connecting one codec's SDATA_IN pin to the next codec's CIN pin. This has the end result of only requiring a single SDATA_IN pin at the controller rather than the standard one SDATA_IN pin per codec. Note, however, that the chained codecs time-share the bandwidth of the SDATA_IN signal under allocation from the controller.

The first codec in the chain (nearest the controller) will have access to the full bandwith of SDATA_IN following a system reset (Cold Reset for each codec). To access any other codec in the chain, the controller must write a suitable value (*i.e.* the Identity of the target codec) to the Chain-In Control register (74h) of each intervening codec in the chain.

The last codec in the serial chain (furthest from the controller) should have its CIN pin connected to digital ground. When writing software drivers, care should be taken to avoid any problems that could occur when this last codec in the chain is set to pass a CIN signal when there is none to pass. Different controllers may handle an input of all 0s differently and leaving the CIN pin floating should definitely be avoided.

BIT#	Function	
1,0	*(bit1,bit0) =	(ID1,ID0): Chain-In off
	(bit1,bit0) ≠	(ID1,ID0): Chain-In on

VENDOR ID REGISTERS (7Ch, 7Eh)

These two read-only (4E53h, 4350h) registers contain National's Vendor ID and National's LM45xx codec version designation. The first 24 bits (4Eh, 53h, 43h) represent the three ASCII characters “NSC” which is National's Vendor ID for Microsoft's Plug and Play. The last 8 bits are the two binary coded decimal characters, *5, 0* and identify the codec to be an LM45*50*.

RESERVED REGISTERS

Do not write to reserved registers. In particular, do not write to registers 24h, 5Ah and 7Ah. All registers not listed in the LM4550 Register Map are reserved. Reserved registers will return 0000h if read.

Low Power Modes

The LM4550 provides 7 bits to control the powerdown state of internal analog and digital subsections and clocks. It also provides one bit intended to control an external analog power amplifier. These 8 bits (PR0 – PR6, EAPD) are the 8 MSBs of the Powerdown Control/Status register, 26h. The status of the four main analog subsections is given by the 4 LSBs in the same register, 26h.

The powerdown bits are implemented in compliance with AC '97 Rev 2.1 to support the standard device power management states D0 – D3 as defined in the ACPI and PCI Bus Power Management specification.

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PR0 controls the powerdown state of the ADC and associated sampling rate conversion circuitry. PR1 controls powerdown for the DAC and the DAC sampling rate conversion circuitry. PR2 powers down the mixer circuits (MIX1, MIX2, National 3D Sound, Mono Out, Line Out). PR3 powers down V_{REF} in addition to all the same mixer circuits as PR2. PR4 powers down the AC Link Digital Interface – see Figure 24 for signal powerdown timing. PR5 disables internal clocks but leaves the crystal oscillator and BIT_CLK running (needed for minimum Primary mode powerdown dissipation in multi-codec systems). PR6 powers down the Headphone amplifier. EAPD controls the External Amplifier PowerDown pin (pin 47).

After a subsection has undergone a powerdown cycle, the appropriate status bit(s) in the Powerdown Control/Status register (26h) must be polled to confirm readiness. In particular the startup time of the V_{REF} circuitry depends on the value of the decoupling capacitors on pin 27 (3.3 µF, 0.1 µF in parallel is recommended).

When the AC Link Digital Interface is powered down the codec output signals SDATA_IN and BIT_CLK (Primary mode) are cleared to zero and no control data can be passed between controller and codec(s). This powerdown state can be cleared in two ways: Cold Reset (RESET# = 0) or Warm Reset (SYNC = 1, no BIT_CLK). Cold Reset sets all registers back to their default values (including clearing PR4) whereas Warm Reset only clears the PR4 bit and restarts the AC Link Digital Interface leaving all register contents otherwise unaffected. For Warm Reset (see Timing Diagrams), the SYNC input is used asynchronously. The LM4550 codec allows the AC Link digital interface powerdown state to be cleared immediately so that its duration can essentially be as short as T_{SH}, the Warm Reset pulse width. However for conformance with AC '97 Rev 2.1, Warm Reset should not be applied within 4 frame times of powerdown *i.e.* the AC Link powerdown state should be allowed to last at least 82.8 µs.

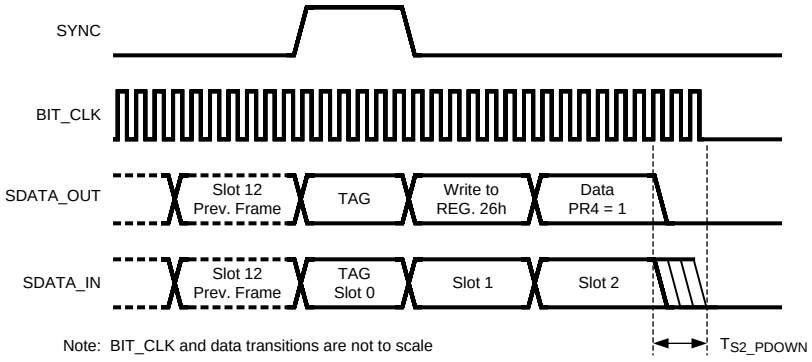

Figure 24. AC Link Powerdown Timing

Improving System Performance

The audio codec is capable of dynamic range performance in excess of 90 db., but the user must pay careful attention to several factors to achieve this. A primary consideration is keeping analog and digital grounds separate, and connecting them together in only one place. Some designers show the connection as a zero ohm resistor, which allows naming the nets separately. Although it is possible to use a two layer board, it is recommended that a minimum of four layers be used, with the two inside layers being analog ground and digital ground. If EMI is a system consideration, then as many as eight layers have been successfully used. The 12 and 25 MHz. clocks can have significant harmonic content depending on the rise and fall times. With the exception of the digital VDD pins, (covered later) bypass capacitors should be very close to the package. The analog VDD pins should be supplied from a separate regulator to reduce noise. By operating the digital portion on 3.3V instead of 5V, an additional 0.5-0.7 db improvement can be obtained.

Depending on power supply layout, routing, and capacitor ESR, a device instability can occur, resulting in increased noise on the outputs. This can be eliminated by adding an inductor in the digital supply line between the supply bypass capacitors and the DVDD pins, which increases the high frequency impedance of the supply as seen by the part. This “current starving” technique slows down internal rise and fall times, which will improve the signal to noise ratio, especially at low temperatures. In addition, the EMI radiated from the board is also reduced.

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Multiple Codecs

EXTENDED AC LINK

Up to four codecs can be supported on the extended AC Link. These multiple codec implementations should run off a common BIT_CLK generated by the Primary Codec. All codecs share the AC '97 Digital Controller output signals, SYNC, SDATA_OUT, and RESET#. Each codec, however, supplies its own SDATA_IN signal back to the controller, with the result that the controller requires one dedicated input pin per codec (Figure 25).

By definition there can be one Primary Codec and up to three Secondary Codecs on an extended AC Link. The Primary Codec has a Codec Identity = (ID1, ID0) = ID = 00 while Secondary Codecs take identities equal to 01, 10 or 11 (see Table 19). The Codec Identity is also used as a chip select function. This allows the Command and Status registers in any of the codecs to be individually addressed although the access mechanism for Secondary Codecs differs slightly from that for a Primary.

The Identity control pins, ID1#, ID0# (pins 46 and 45) are internally pulled up to DV_{DD}. The Codec may therefore be configured as 'Primary' either by leaving ID1#, ID0# open (NC) or by strapping them externally to DV_{DD} (digital supply).

The difference between Primary and Secondary codec modes is: in their timing source; in the AMAP Slot-to-DAC mapping used in Output Frames carried by SDATA_OUT; and in the Tag Bit handling in Output Frames for Command/Status register access. For a timing source, a Primary codec divides down by 2 the frequency of the signal on XTAL_IN and also generates this as the BIT_CLK output for the use of the controller and any Secondary codecs. Secondary codecs use BIT_CLK as an input and as their timing source and do not use XTAL_IN or XTAL_OUT, The AMAP mappings are given in Table 19 and the use of Tag Bits is described below.

SECONDARY CODEC REGISTER ACCESS

For Secondary Codec access, the controller must set the tag bits for Command Address and Data in the Output Frame as invalid (*i.e.* equal to 0). The Command Address and Data tag bits are in slot 0, bits 14 and 13 and Output Frames are those in the SDATA_OUT signal from controller to codec. The controller must also place the non-zero value (01, 10, or 11) corresponding to the Identity (ID1, ID0) of the target Secondary Codec into the Codec ID field (slot 0, bits 1 and 0) in that same Output Frame. The value set in the Codec ID field determines which of the three possible Secondary Codecs is accessed. Unlike a Primary Codec, a Secondary Codec will disregard the Command Address and Data tag bits when there is a match between the 2-bit Codec ID value (slot 0, bits 1 and 0) and the Codec Identity (ID1, ID0). Instead it uses the Codec-ID/Identity match to indicate that the Command Address in slot 1 and (if a “write”) the Command Data in slot 2 are valid.

When reading from a Secondary Codec, the controller must send the correct Codec ID bits (*i.e.* the target Codec Identity in slot 0, bits 1 and 0) along with the read-request bit (slot 1, bit 19) and target register address (slot 1, bits 18 – 12). To write to a Secondary Codec, a controller must send the correct Codec ID bits when slot 1 contains a valid target register address and “write” indicator bit and slot 2 contains valid target register data. A write operation is only valid if the register address and data are both valid and sent within the same frame. When accessing the Primary Codec, the Codec ID bits are cleared and the tag bits 14 and 13 resume their role indicating the validity of Command Address and Data in slots 1 and 2.

The use of the tag bits in Input Frames (carried by the SDATA_IN signal) is the same for Primary and Secondary Codecs.

The Codec Identity is determined by the inverting input pins ID1#, ID0# (pins 46 and 45) and can be read as the value of the ID1, ID0 bits (D15, D14) in the Extended Audio ID register, 28h of the target codec.

In addition to the Codec Identity bits (ID1, ID0), the read-only Extended Audio ID register (28h) contains the AMAP bit (D9). The AMAP bit indicates support for the (optional) AC '97 Rev. 2.1 compliant mappings from slots in AC Link Output Frames to the audio DACs for each of the four Codec Identity modes. AMAP = 1 indicates that the default mapping (as realized after reset) of Slots-to-DACs conforms to Table 19. Slots in AC Link Input Frames are always mapped such that PCM data from the left ADC channel is carried by slot 3 and PCM data from the right ADC channel by slot 4. Output Frames are those carried by the SDATA_OUT signal from the controller to the codec while Input Frames are those carried by the SDATA_IN signal from the codec to the controller.

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SLOT 0: TAG bits in Output Frames (controller to codec)

Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Valid Frame	Slot 1 Valid	Slot 2 Valid	Slot 3 Valid	Slot 4 Valid	X	Slot 6 Valid	Slot 7 Valid	Slot 8 Valid	Slot 9 Valid	X	X	X	X	ID1	ID0

Extended Audio ID register (28h): Support for Multiple Codecs

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
28h	Extended Audio ID	ID1	ID0	X	X	X	X	AMAP	X	X	X	X	X	X	X	X	VRA	X201h

Table 19. AMAP Slot-to-DAC Audio MAPping

Codec Identity Mode	ID1 (D15, 28h)	ID0 (D14, 28h)	Left DAC data		Right DAC data	
			From Slot #	5.1 Audio channel (1)	From Slot #	5.1 Audio channel (1)
Primary	0	0	3	Left	4	Right
Secondary 1	0	1	3	Left	4	Right
Secondary 2	1	0	7	Left Surround	8	Right Surround
Secondary 3	1	1	6	Center	9	LFE

(1) AC '97 Rev 2.1 specifies this allocation of 5.1 Audio channels to these slots in the AC Link Output Frame

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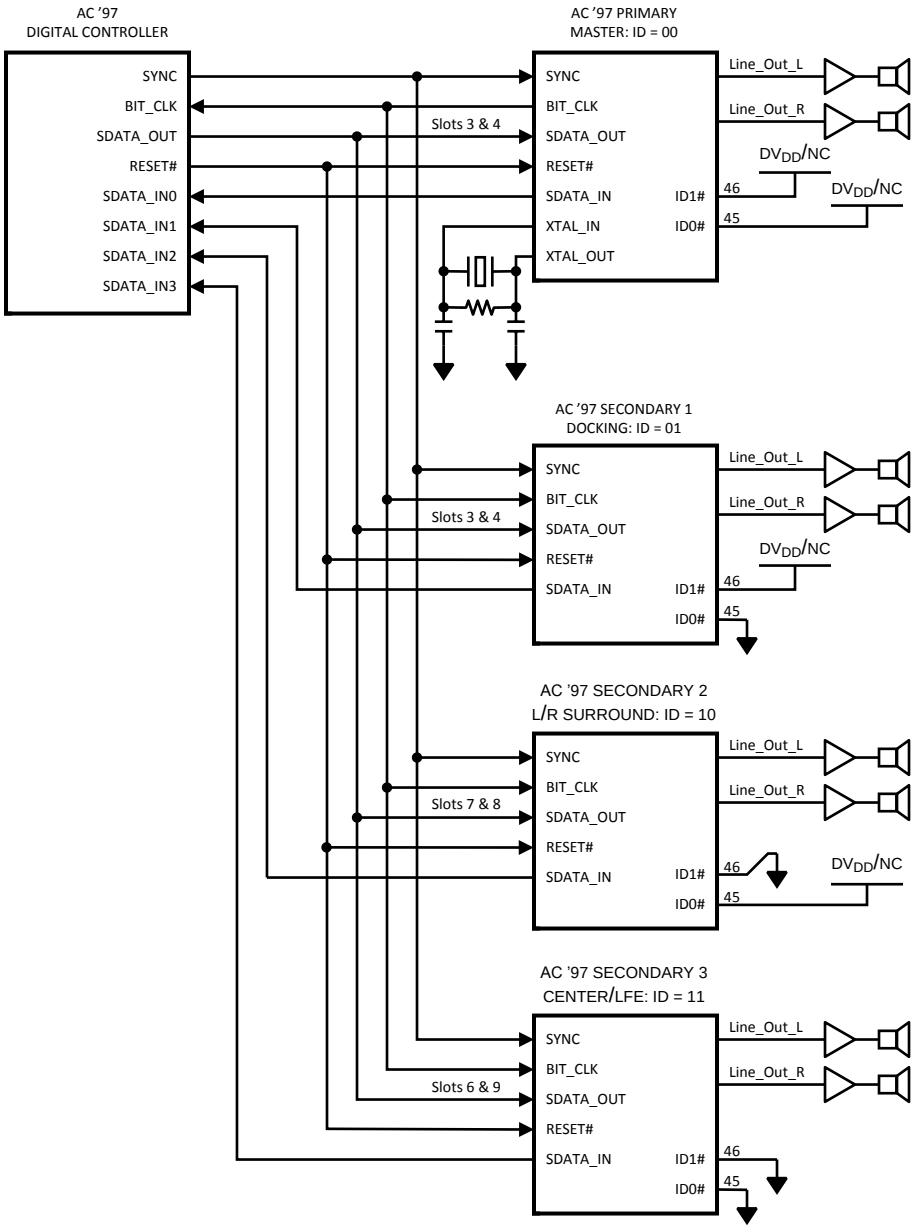

Figure 25. Multiple Codecs using Extended AC Link

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CODEC CHAINING

Using National Semiconductor's unique feature for chaining together codecs, a multiple codec system can be built using fewer interface pins. This Chain feature allows two, three or four codecs to share a single signal input pin at the controller. By setting the two LSBs of the Chain-In Control register (74h) to a value other than the Codec Identity, a controller can instruct a codec to disconnect its own SDATA_IN signal and discard its own Input Frame and instead switch the signal connected to the CIN pin through to the SDATA_IN output pin allowing passage of an SDATA_IN signal carrying the Input Frame from a codec further down the chain. The Chain-In Control register (74h) is updated at the rising edge of SYNC therefore an instruction to enable or disable the Chain feature takes effect in the next frame.

When the Chain feature is used the CIN pin should always be driven. Connect CIN to either the SDATA_IN pin from another codec or else ground CIN to prevent the possibility of floating the SDATA_IN signal at the controller.

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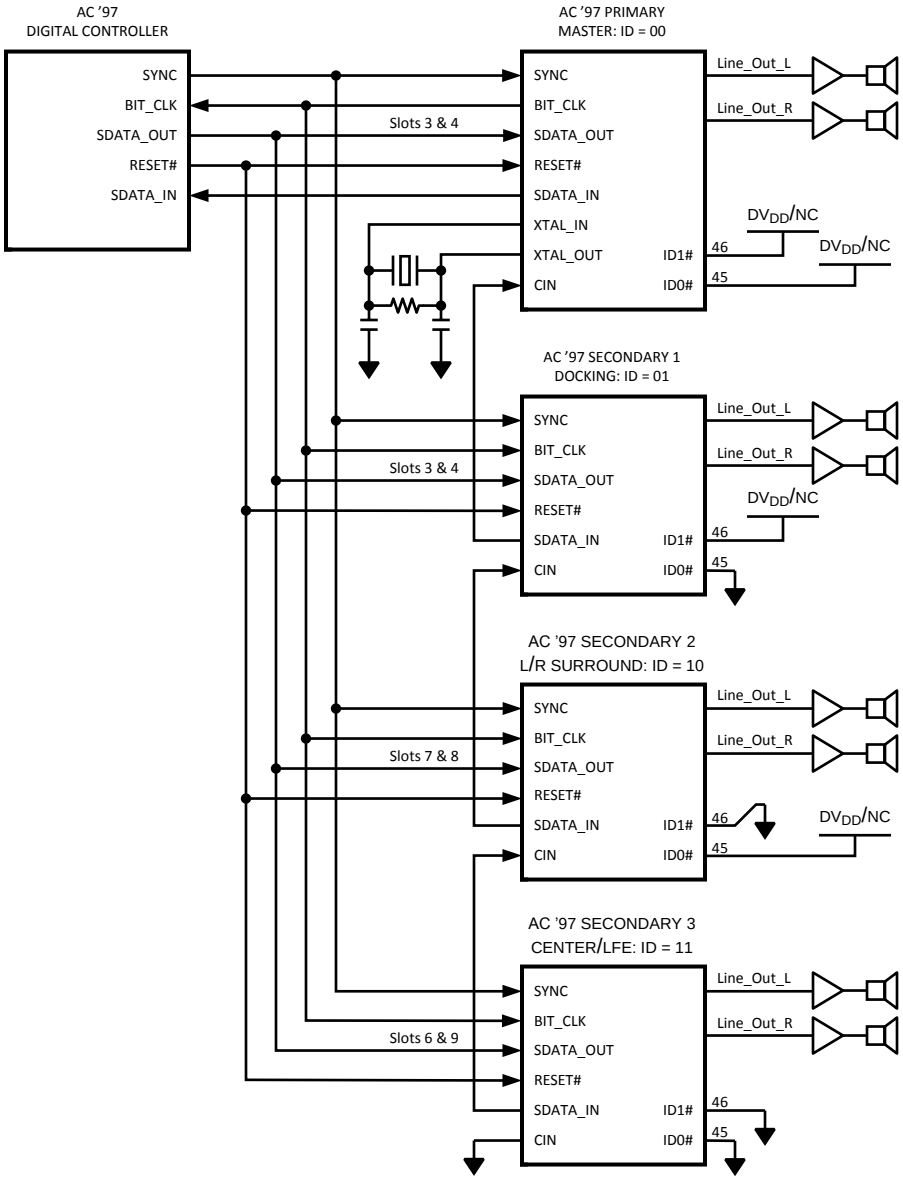

Figure 26. Multiple Codecs in a Chain

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Test Modes

AC '97 Rev 2.1 defines two test modes: ATE test mode and Vendor test mode. Cold Reset is the only way to exit either of them. The ATE test mode is activated if SDATA_OUT is sampled high by the trailing edge (zero-to-one transition) of RESET#. In ATE test mode the codec AC Link outputs SDATA_IN and BIT_CLK are configured to a high impedance state to allow tester control of the AC Link interface for controller testing. ATE test mode timing parameters are given in the Electrical Characteristics table. The Vendor test mode is entered if SYNC is sampled high by the zero-to-one transition of RESET#. Neither of these entry conditions can occur in normal AC Link operation but care must be taken to avoid mistaken activation of the test modes when using non standard controllers.

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REVISION HISTORY

Changes from Revision E (April 2013) to Revision F	Page
• Changed layout of National Data Sheet to TI format	37

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