

LM2611 1.4MHz Cuk Converter

Check for Samples: [LM2611](#)

FEATURES

- 1.4MHz switching frequency
- Low $R_{DS(ON)}$ DMOS FET
- 1mVp-p output ripple
- -5V at 300mA from 5V input
- Better regulation than a charge pump
- Uses tiny capacitors and inductors
- Wide input range: 2.7V to 14V
- Low shutdown current: $<1\mu A$
- 5-lead SOT-23 package

APPLICATIONS

- MR Head Bias
- Digital camera CCD bias
- LCD bias
- GaAs FET bias
- Positive to negative conversion

DESCRIPTION

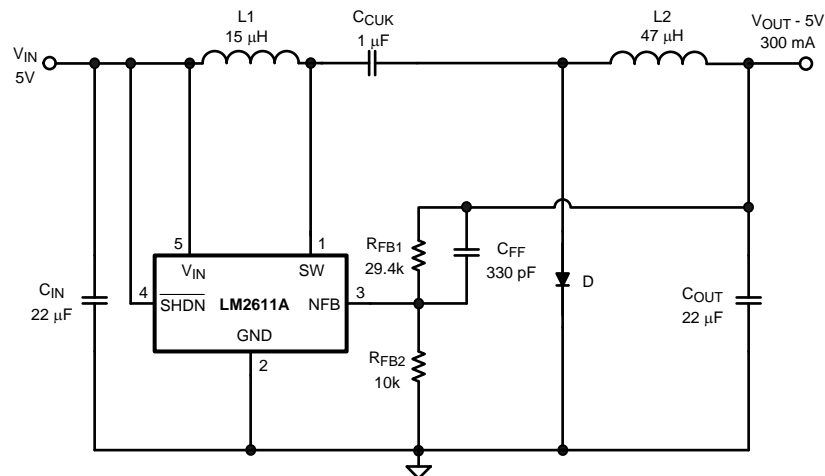
The LM2611 is a current mode, PWM inverting switching regulator. Operating from a 2.7 - 14V supply, it is capable of producing a regulated negative output voltage of up to $-(36-V_{IN(MAX)})$. The LM2611 utilizes an input and output inductor, which enables low voltage ripple and RMS current on both the input and the output. With a switching frequency of 1.4MHz, the inductors and output capacitor can be physically small and low cost. High efficiency is achieved through the use of a low $R_{DS(ON)}$ FET.

The LM2611 features a shutdown pin, which can be activated when the part is not needed to lower the I_q and save battery life. A negative feedback (NFB) pin provides a simple method of setting the output voltage, using just two resistors. Cycle-by-cycle current limiting and internal compensation further simplify the use of the LM2611.

The LM2611 is available in a small SOT23-5 package. It comes in two grades:

	Grade A	Grade B
Current Limit	1.2A	0.9A
$R_{DS(ON)}$	0.5 Ω	0.7 Ω

Typical Application Circuit



C_{IN} : TAIYO YUDEN X5R JMK325BJ226MM
 C_{CUK} : TAIYO YUDEN X5R EMK316BJ105MF
 C_{OUT} : TAIYO YUDEN X5R JMK325BJ226MM
D: ON SEMICONDUCTOR MBR0520
L1: SUMIDA CR32-150
L2: SUMIDA CR32-470



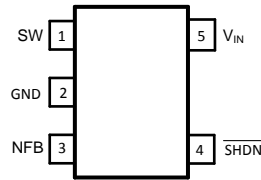
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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

**5-lead SOT-23 Package
Top View**



See Package Number DBV0005A

Pin Description

Pin	Name	Function
1	SW	Drain of internal switch. Connect at the node of the input inductor and Cuk capacitor.
2	GND	Analog and power ground.
3	NFB	Negative feedback. Connect to output via external resistor divider to set output voltage.
4	$\overline{\text{SHDN}}$	Shutdown control input. $V_{\text{IN}} = \text{Device on}$. Ground = Device in shutdown.
5	V_{IN}	Analog and power input. Filter out high frequency noise with a 0.1 μF ceramic capacitor placed close to the pin.

Absolute Maximum Ratings ⁽¹⁾

V_{IN}	14.5V
SW Voltage	-0.4V to 36V
NFB Voltage	+0.4V to -6V
$\overline{\text{SHDN}}$ Voltage	-0.4V to 14.5V
Maximum Junction Temperature	125°C
Power Dissipation ⁽²⁾	Internally Limited
Lead Temperature	300°C
ESD Susceptibility ⁽³⁾	
Human Body Model	2kV
Machine Model	200V

- (1) Absolute maximum ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions for which the device is intended to be functional, but device parameter specifications may not be ensured. For specifications and test conditions, see the Electrical Characteristics.
- (2) The maximum allowable power dissipation is a function of the maximum junction temperature, $T_{\text{J(MAX)}}$, the junction-to-ambient thermal resistance, θ_{JA} , and the ambient temperature, T_{A} . See the Electrical Characteristics table for the thermal resistance of various layouts. The maximum allowable power dissipation at any ambient temperature is calculated using: $P_{\text{D (MAX)}} = (T_{\text{J(MAX)}} - T_{\text{A}})/\theta_{\text{JA}}$. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown.
- (3) The human body model is a 100 pF capacitor discharged through a 1.5k Ω resistor into each pin. The machine model is a 200pF capacitor discharged directly into each pin.

Operating Conditions

Operating Junction Temperature Range	-40°C to +125°C
Storage Temperature	-65°C to +150°C
Supply Voltage	2.7V to 14V
θ_{JA}	256°C/W

Electrical Characteristics

Specifications in standard type face are for $T_J = 25^\circ\text{C}$ and those with **boldface type** apply over the **Temperature Range** $T_J = -40^\circ\text{C}$ to $+85^\circ\text{C}$, unless otherwise specified. $V_{IN} = 5.0\text{V}$ and $I_L = 0\text{A}$, unless otherwise specified.

Symbol	Parameter	Conditions	Min ⁽¹⁾	Typ ⁽²⁾	Max ⁽¹⁾	Units
V_{IN}	Input Voltage		2.7		14	V
I_{SW}	Switch Current Limit	Grade A	1	1.2	2	A
		Grade B	0.7	0.9		
$R_{DS(ON)}$	Switch ON Resistance	Grade A		0.5	0.65	Ω
		Grade B		0.7	0.9	
$SHDN_{TH}$	Shutdown Threshold	Device enabled	1.5			V
		Device disabled			0.50	
I_{SHDN}	Shutdown Pin Bias Current	$V_{SHDN} = 0\text{V}$		0.0		μA
		$V_{SHDN} = 5\text{V}$		0.0	1.0	
NFB	Negative Feedback Reference	$V_{IN} = 3\text{V}$	-1.205	-1.23	-1.255	V
I_{NFB}	NFB Pin Bias Current	$V_{NFB} = -1.23\text{V}$	-2.7	-4.7	-6.7	μA
I_q	Quiescent Current	$V_{SHDN} = 5\text{V}$, Switching		1.8	3.5	mA
		$V_{SHDN} = 5\text{V}$, Not Switching		270	500	μA
		$V_{SHDN} = 0\text{V}$		0.024	1	μA
$\%V_{OUT}/\Delta V_{IN}$	Reference Line Regulation	$2.7\text{V} \leq V_{IN} \leq 14\text{V}$		0.02		$\%/V$
f_S	Switching Frequency		1.0	1.4	1.8	MHz
D_{MAX}	Maximum Duty Cycle		82	88		%
I_L	Switch Leakage	Not Switching $V_{SW} = 5\text{V}$			1	μA

- (1) All limits are specified at room temperature (standard typeface) and at temperature extremes (bold typeface). All room temperature limits are 100% tested through statistical analysis. All limits at temperature extremes via correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).
- (2) Typical numbers are at 25°C and represent the expected value of the parameter.

Typical Performance Characteristics

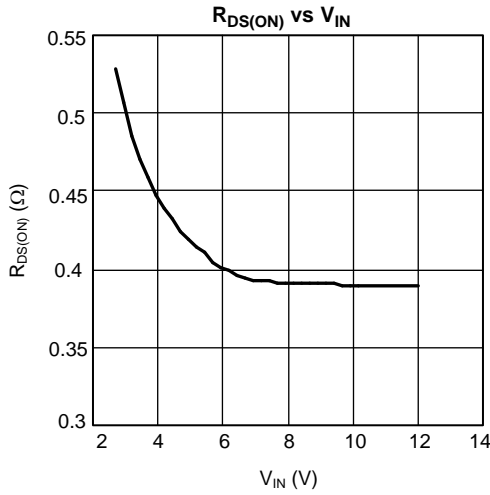


Figure 1.

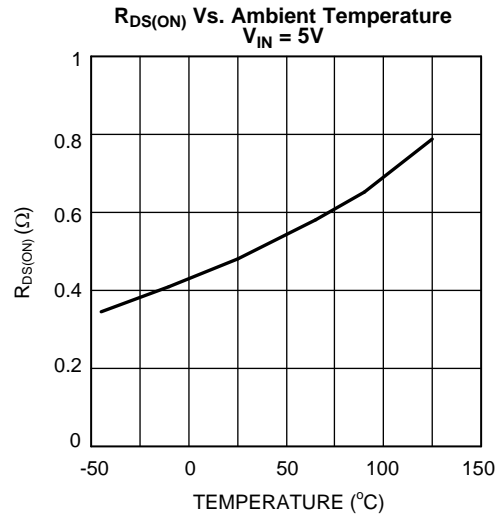


Figure 2.

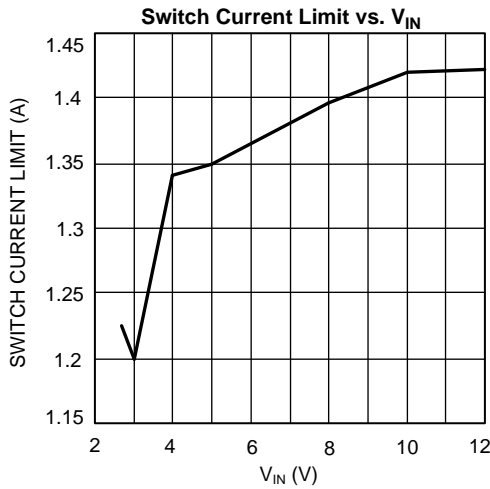


Figure 3.

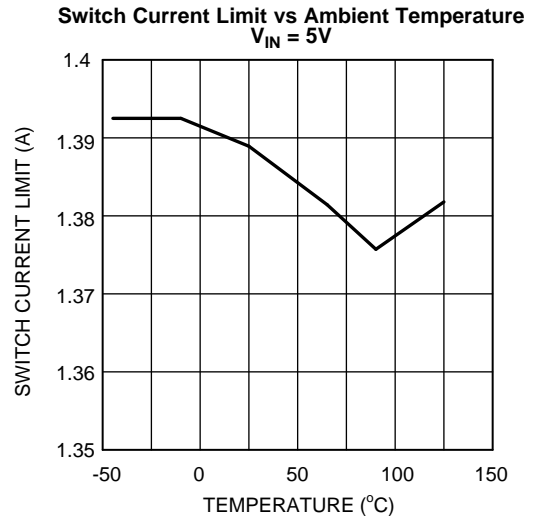


Figure 4.

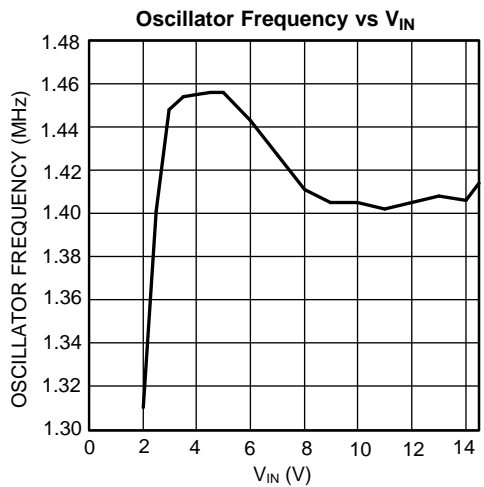


Figure 5.

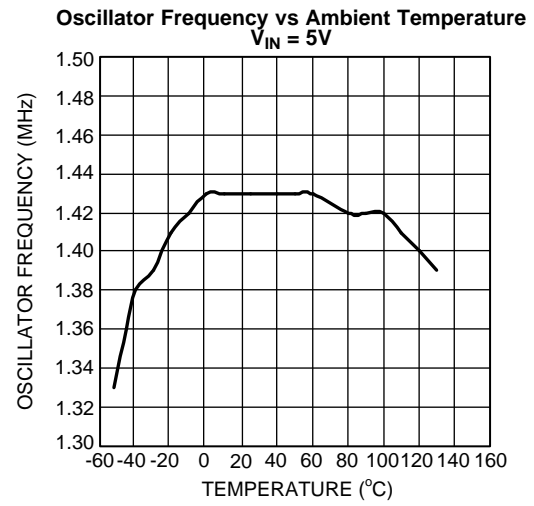


Figure 6.

Typical Performance Characteristics (continued)

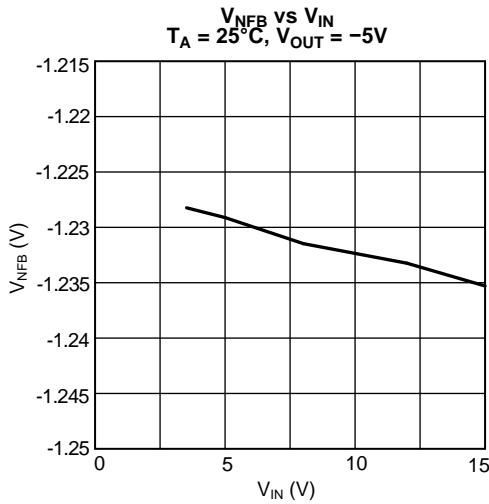


Figure 7.

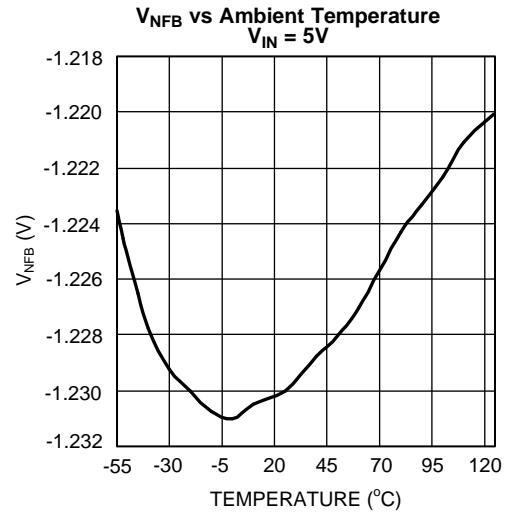


Figure 8.

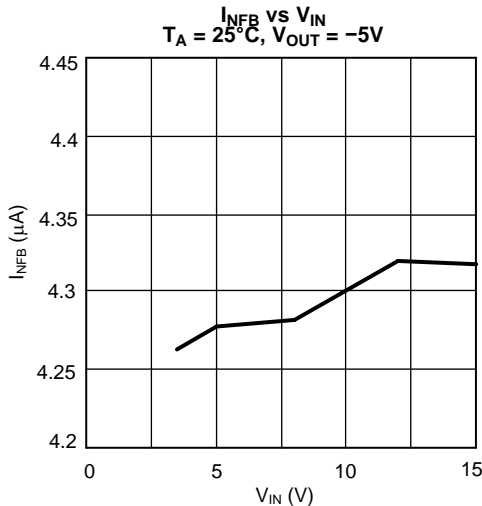


Figure 9.

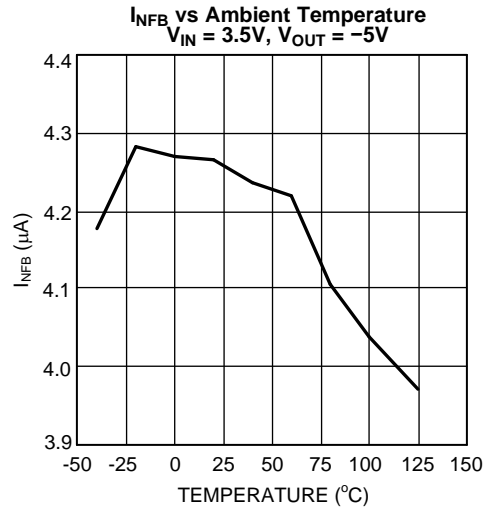


Figure 10.

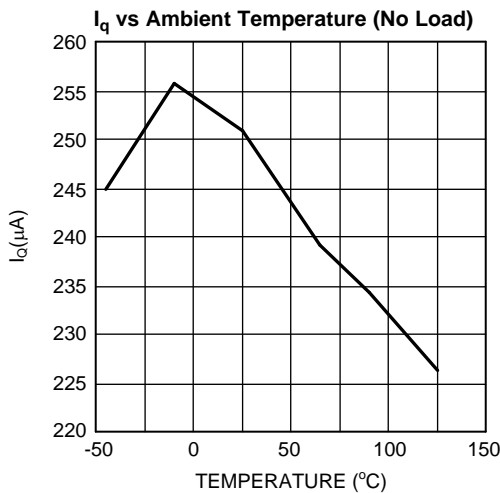


Figure 11.

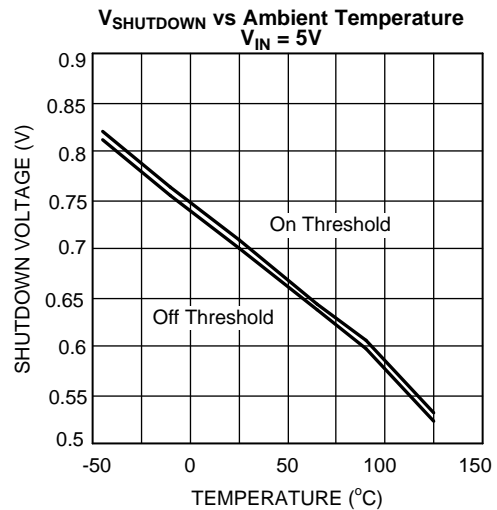
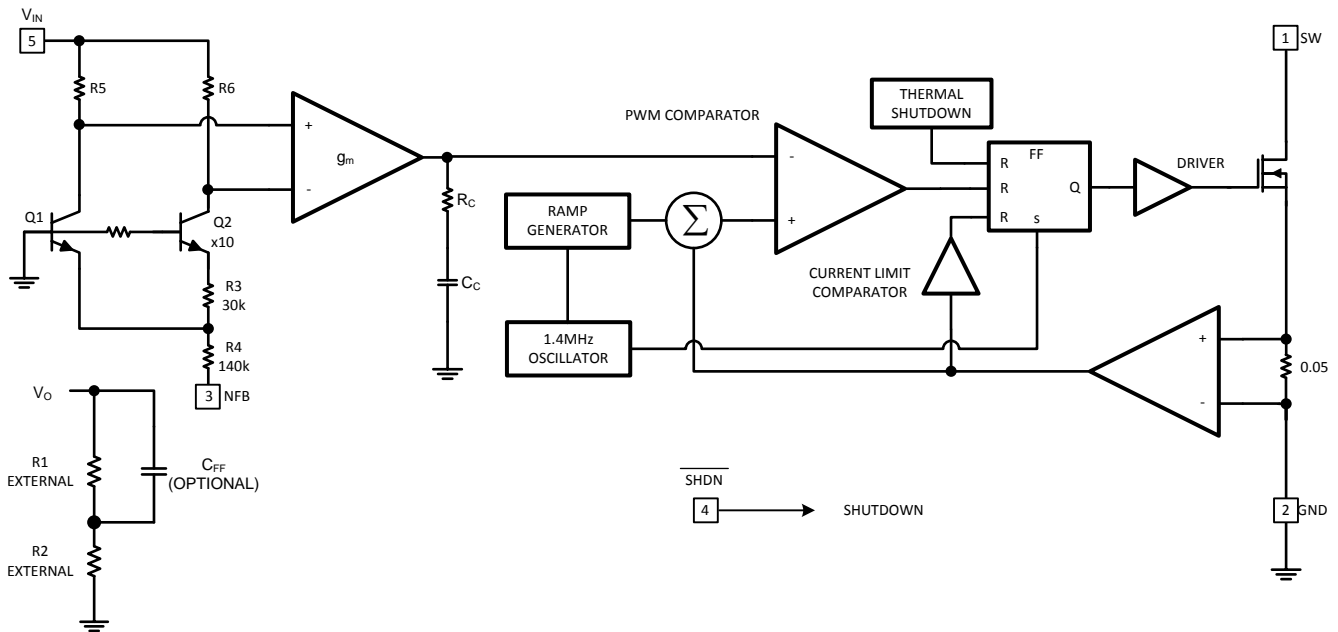


Figure 12.

Block Diagram



Operation

Cuk Converter

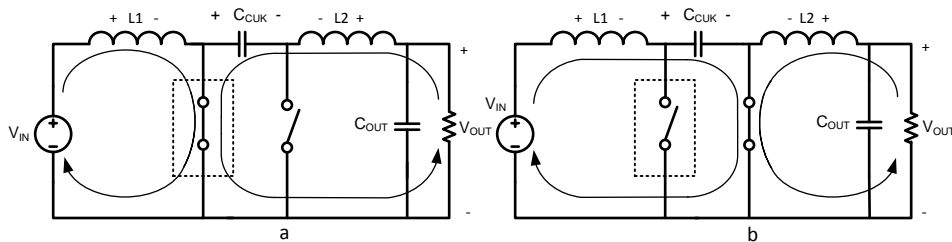


Figure 13. Operating Cycles of a Cuk Converter

The LM2611 is a current mode, fixed frequency PWM switching regulator with a $-1.23V$ reference that makes it ideal for use in a Cuk converter. The Cuk converter inverts the input and can step up or step down the absolute value. Using inductors on both the input and output, the Cuk converter produces very little input and output current ripple. This is a significant advantage over other inverting topologies such as the buck-boost and flyback.

The operating states of the Cuk converter are shown in [Figure 13](#). During the first cycle, the transistor switch is closed and the diode is open. $L1$ is charged by the source and $L2$ is charged by C_{CUK} , while the output current is provided by $L2$. In the second cycle, $L1$ charges C_{CUK} and $L2$ discharges through the load. By applying the volt-second balance to either of the inductors, the relationship of V_{OUT} to the duty cycle (D) is found to be:

$$V_{OUT} = -V_{IN} \frac{D}{1-D} \tag{1}$$

The following sections review the steady-state design of the LM2611 Cuk converter.

Output and Input Inductor

[Figure 14](#) and [Figure 15](#) show the steady-state voltage and current waveforms for $L1$ and $L2$, respectively. Referring to [Figure 13](#) (a), when the switch is closed, V_{IN} is applied across $L1$. In the next cycle, the switch opens and the diode becomes forward biased, and V_{OUT} is applied across $L1$ (the voltage across C_{CUK} is $V_{IN} - V_{OUT}$).

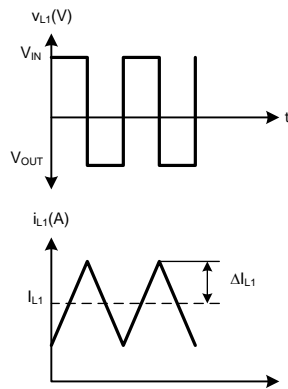


Figure 14. Voltage and Current Waveforms in Inductor L1 of a Cuk Converter

The voltage and current waveforms of inductor L2 are shown in Figure 15. During the first cycle of operation, when the switch is closed, V_{IN} is applied across L2. When the switch opens, V_{OUT} is applied across L2.

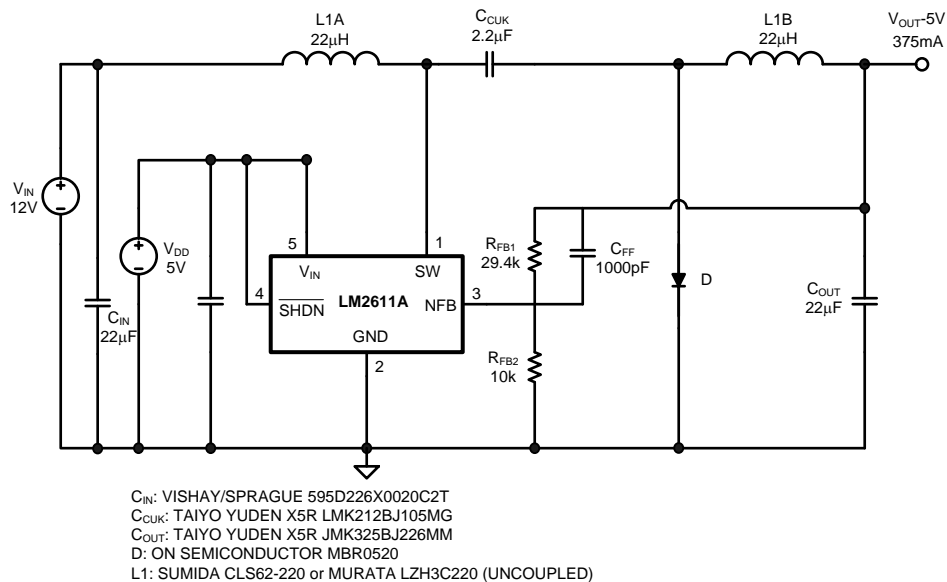


Figure 15. Voltage and Current Waveforms in Inductor L2 of a Cuk Converter

The following equations define values given in Figure 14 and Figure 15:

$$I_{L2} = I_{OUT} \quad (2)$$

$$\Delta I_{L2} = \frac{V_{IN} \times D \times T_S}{2 \times L_2} \quad (3)$$

$$I_{L1} = \frac{D}{1-D} I_{L2} = \frac{D}{1-D} I_{OUT} \quad (4)$$

$$\Delta I_{L1} = \frac{V_{IN} \times D \times T_S}{2 \times L_1} \quad (5)$$

Use these equations to choose correct core sizes for the inductors. The design of the LM2611's internal compensation assumes L1 and L2 are equal to 10 - 22 μ H, thus it is recommended to stay within this range.

Switch Current Limit

The LM2611 incorporates a separate current limit comparator, making current limit independent of any other variables. The current limit comparator measures the switch current versus a reference that represents current limit. If at any time the switch current surpasses the current limit, the switch opens until the next switching period. To determine the maximum load for a given set of conditions, both the input and output inductor currents must be considered. The switch current is equal to $i_{L1} + i_{L2}$, and is drawn in [Figure 16](#). In summary:

$$\begin{aligned}
 i_{SW(PEAK)} &= i_{L1} + i_{L2} = I_{L1} + I_{L2} + \Delta i_{L1} + \Delta i_{L2} \\
 &= I_{OUT} \times \left(1 + \frac{D}{1-D}\right) + \frac{V_{IN} \times D \times T_S}{2} \times \left(\frac{1}{L_1} + \frac{1}{L_2}\right)
 \end{aligned} \tag{6}$$

$i_{SW(PEAK)}$ must be less than the current limit (1.2A typical), but will also be limited by the thermal resistivity of the LM2611's SOT23-5 package ($\theta_{JA} = 265^\circ\text{C/W}$).

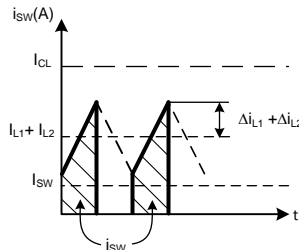


Figure 16. Switch Current Waveform in a Cuk Converter. The peak value is equal to the sum of the average currents through L1 and L2 and the average-to-peak current ripples through L1 and L2.

Input Capacitor

The input current waveform to a Cuk converter is continuous and triangular, as shown in [Figure 14](#). The input inductor insures that the input capacitor sees fairly low ripple currents. However, as the input inductor gets smaller, the input ripple goes up. The RMS current in the input capacitor is given by:

$$I_{CIN(RMS)} = \frac{1}{2\sqrt{3}} \frac{V_{IN}}{f_s L_1 \left(\frac{V_i}{|V_o|} + 1\right)} \tag{7}$$

The input capacitor should be capable of handling the RMS current. Although the input capacitor is not so critical in a Cuk converter, a 10 μF or higher value good quality capacitor prevents any impedance interactions with the input supply. A 0.1 μF or 1 μF ceramic bypass capacitor is also recommended on the V_{IN} pin (pin 5) of the IC. This capacitor must be connected very close to pin 5 (within 0.2 inches).

Output Capacitor

Like the input current, the output current is also continuous, triangular, and has low ripple (see I_{L2} in [Figure 15](#)). The output capacitor must be rated to handle its RMS current:

$$I_{COUT(RMS)} = \frac{\Delta i_{L2}}{\sqrt{3}} = \frac{1}{2\sqrt{3}} \frac{V_{IN}}{f_s L_2 \left(\frac{V_i}{|V_o|} + 1\right)} \tag{8}$$

For example, $I_{COUT(RMS)}$ can range from 30mA to 180mA with $10\mu\text{H} \leq L_{1,2} \leq 22\mu\text{H}$, $-10\text{V} \leq V_{OUT} \leq -3.3\text{V}$, and $2.7\text{V} \leq V_{IN} \leq 30\text{V}$ (V_{IN} may be 30V if using separate power and analog supplies, see Split Supply Operation in the APPLICATIONS section). The worst case conditions are with $L_{1,2}$, $V_{OUT(MAX)}$, and $V_{IN(MAX)}$. Many capacitor technologies will provide this level of RMS current, but ceramic capacitors are ideally suited for the LM2611. Ceramic capacitors provide a good combination of capacitance and equivalent series resistance (ESR) to keep the zero formed by the capacitance and ESR at high frequencies. The ESR zero is calculated as:

$$f_{ESR} = \frac{1}{2\pi C_{OUT} ESR} \text{ (Hz)} \tag{9}$$

A general rule of thumb is to keep $f_{ESR} > 80\text{kHz}$ for LM2611 Cuk designs. Low ESR tantalum capacitors will usually be rated for at least 180mA in a voltage rating of 10V or above. However the ESR in a tantalum capacitor (even in a low ESR tantalum capacitor) is much higher than in a ceramic capacitor and could place f_{ESR} low enough to cause the LM2611 to run unstable.

Improving Transient Response/Compensation

The compensator in the LM2611 is internal. However, a zero-pole pair can be added to the open loop frequency response by inserting a feed forward capacitor, C_{FF} , in parallel to the top feedback resistor (R_{FB1}). Phase margin and bandwidth can be improved with the added zero-pole pair. This in turn will improve the transient response to a step load change (see Figure 17 and Figure 18). The position of the zero-pole pair is a function of the feedback resistors and the capacitor value:

$$\omega_z = \frac{1}{C_{FF}R_{FB1}} \text{ (rad/s)} \tag{10}$$

$$\omega_p = \frac{1}{C_{FF}R_{FB1}} \left(1 + \frac{R_{FB1}}{R_{FB2}}\right) \text{ (rad/s)} \tag{11}$$

The optimal position for this zero-pole pair will vary with circuit parameters such as D , I_{OUT} , C_{OUT} , $L1$, $L2$, and C_{CUK} . For most cases, the value for the zero frequency is between 5 kHz to 20 kHz. Notice how the pole position, ω_p , is dependant on the feedback resistors R_{FB1} and R_{FB2} , and therefore also dependant on the output voltage. As the output voltage becomes closer to -1.26V , the pole moves towards the zero, tending to cancel it out. If the absolute magnitude of the output voltage is less than 3.3V , adding the zero-pole pair will not have much effect on the response.

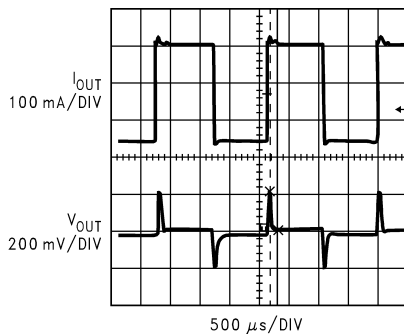


Figure 17. 130mA to 400mA Transient Response of the circuit in 5V to -5V Inverting Converter with $C_{FF} = 1\text{nF}$

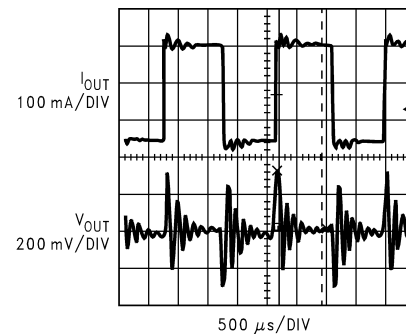


Figure 18. 130mA to 400mA Transient Response of the circuit in 5V to -5V Inverting Converter with C_{FF} disconnected

Hysteretic Mode

As the output current decreases, there will come a point when the energy stored in the Cuk capacitor is more than the energy required by the load. The excess energy is absorbed by the output capacitor, causing the output voltage to increase out of regulation. The LM2611 detects when this happens and enters a pulse skipping, or hysteretic mode. In hysteretic mode, the output voltage ripple will increase, as illustrated in [Figure 19](#) and [Figure 20](#).

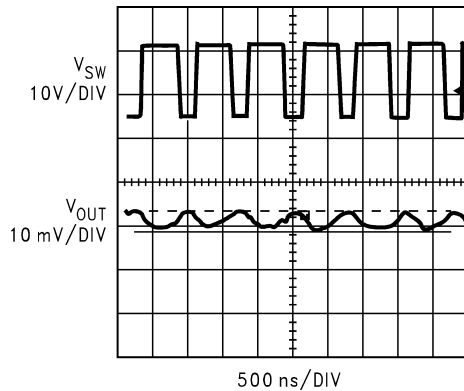


Figure 19. The LM2611 in PWM mode has very low ripple

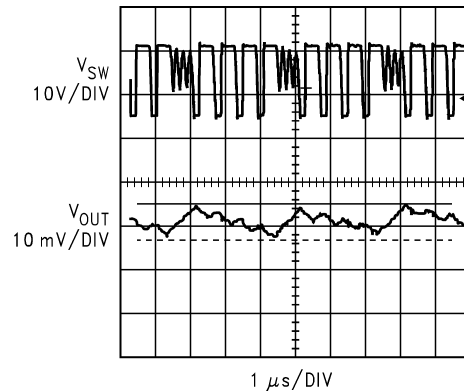


Figure 20. At low loads, the LM2611 enters a pulse-skipping mode. The output ripple slightly increases in this mode.

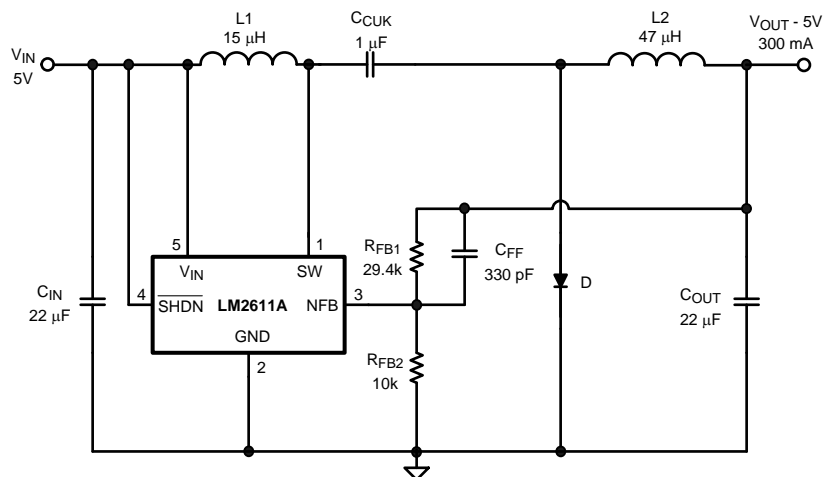
Thermal Shutdown

If the junction temperature of the LM2611 exceeds 163°C, it will enter thermal shutdown. In thermal shutdown, the part deactivates the driver and the switch turns off. The switch remains off until the junction temperature drops to 155°C, at which point the part begins switching again. It will typically take 10ms for the junction temperature to drop from 163°C to 155°C with the switch off.

APPLICATION INFORMATION

Application Circuits

5V to -5V Inverting Converter



C_{IN}: TAIYO YUDEN X5R JMK325BJ226MM
 C_{CUK}: TAIYO YUDEN X5R EMK316BJ105MF
 C_{OUT}: TAIYO YUDEN X5R JMK325BJ226MM
 D: ON SEMICONDUCTOR MBR0520
 L1: SUMIDA CR32-150
 L2: SUMIDA CR32-470

Figure 21. The Maximum Output Current vs Output Voltage (Adjust R_{FB2} to Set a Different Output Voltage) When The Input Voltage is 5V

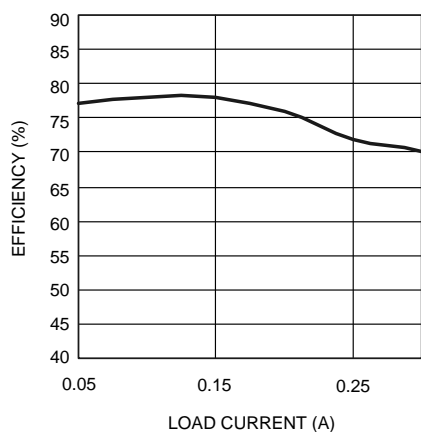


Figure 22. Efficiency vs Load Current

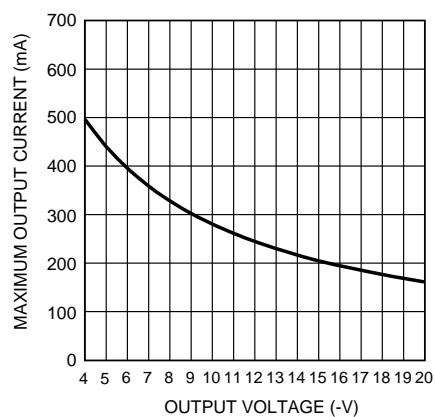
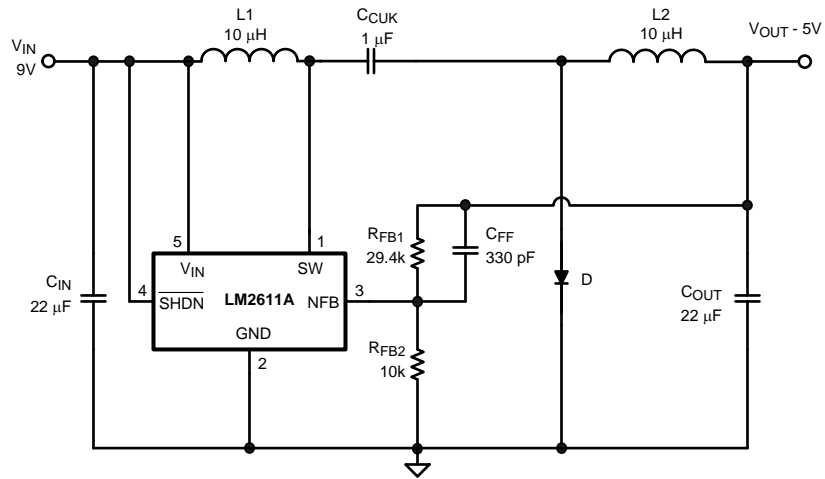


Figure 23. The Maximum Output Current vs Output Voltage (Adjust R_{FB2} to Set a Different Output Voltage) When The Input Voltage is 5V

9V to -5V Inverting Converter



C_{IN}: TAIYO YUDEN X5R JMK325BJ226MM
 C_{CUK}: TAIYO YUDEN X5R EMK316BJ105MF
 C_{OUT}: TAIYO YUDEN X5R JMK325BJ226MM
 D: ON SEMICONDUCTOR MBR0520
 L1: SUMIDA CR32-100
 L2: SUMIDA CR32-100

Figure 24. The Maximum Output Current vs Output Voltage (Adjust R_{FB2} to Set a Different Output Voltage) When The Input Voltage is 9V

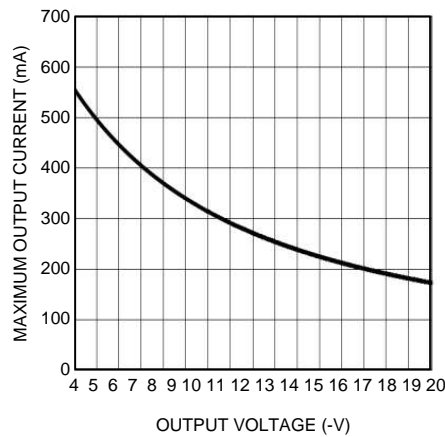
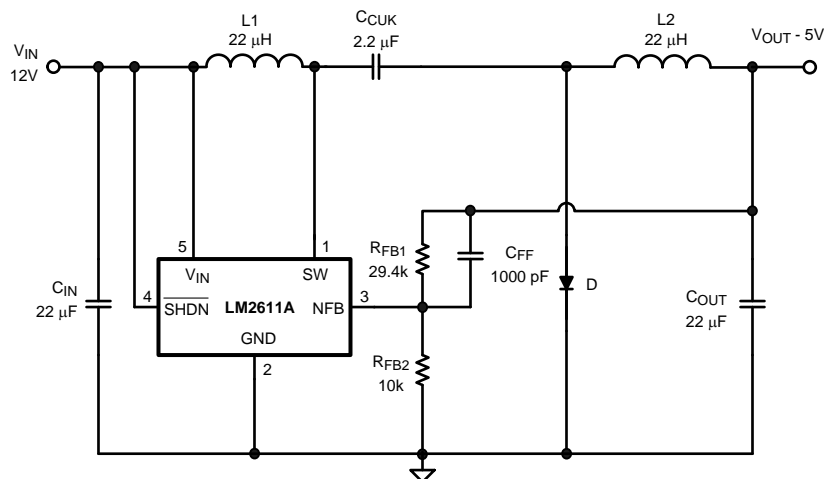


Figure 25. The Maximum Output Current vs Output Voltage (Adjust R_{FB2} to Set a Different Output Voltage) When The Input Voltage is 9V

12V to -5V Inverting Converter



C_{IN}: TAIYO YUDEN X5R JMK325BJ226MM
 C_{CUK}: TAIYO YUDEN X5R EMK316BJ225ML
 C_{OUT}: TAIYO YUDEN X5R JMK325BJ226MM
 D: ON SEMICONDUCTOR MBR0520
 L1: SUMIDA CR32-220
 L2: SUMIDA CR32-220

Figure 26. The Maximum Output Current vs Output Voltage (Adjust R_{FB2} to Set a Different Output Voltage) When The Input Voltage is 12V

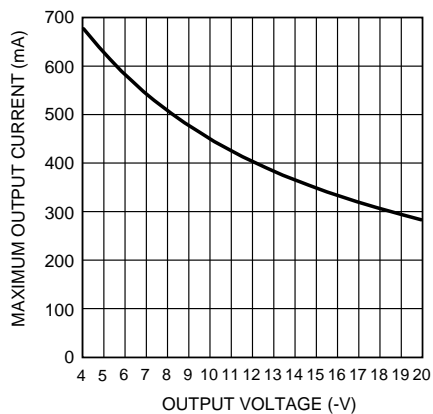
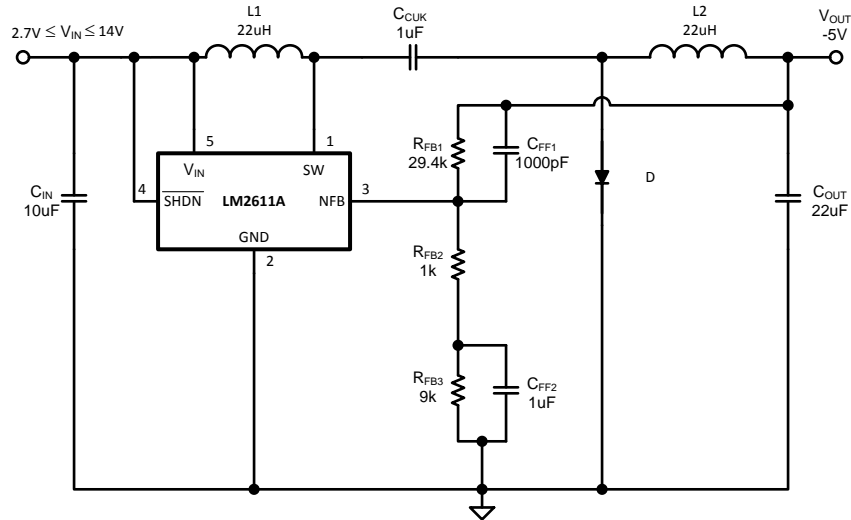


Figure 27. The Maximum Output Current vs Output Voltage (Adjust R_{FB2} to Set a Different Output Voltage) When The Input Voltage is 12V

High Duty Cycle/Load Current Operation

The circuit in [Figure 32](#) is used for high duty cycles ($D > 0.5$) and high load currents. The duty cycle will begin to increase beyond 50% as the input voltage drops below the absolute magnitude of the output voltage. R_{FB3} and C_{FF2} are added to the feedback network to introduce a low frequency lag compensation (pole-zero pair) necessary to stabilize the circuit under the combination of high duty cycle and high load currents.



C_{IN} : TAIYO YUDEN X5R JMK325BJ106MN
 C_{CUK} : TAIYO YUDEN X5R TMK316BJ105ML
 C_{OUT} : TAIYO YUDEN X5R JMK325BJ226MM
 D: ON SEMICONDUCTOR MBR0520
 L1, L2: SUMIDA CDRH6D28-220

Figure 32. LM2611 High Current Schematic

REVISION HISTORY

Changes from Revision H (April 2013) to Revision I	Page
<hr/> <ul style="list-style-type: none">• Changed layout of National Data Sheet to TI format	<hr/> 16

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM2611AMF	NRND	SOT-23	DBV	5	1000	TBD	Call TI	Call TI	-40 to 125	S40A	
LM2611AMF/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	S40A	
LM2611AMFX/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	S40A	
LM2611BMF	NRND	SOT-23	DBV	5	1000	TBD	Call TI	Call TI	-40 to 125	S40B	
LM2611BMF/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	S40B	
LM2611BMFX/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	S40B	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM2611AMF	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM2611AMF/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM2611AMFX/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM2611BMF	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM2611BMF/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM2611BMFX/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

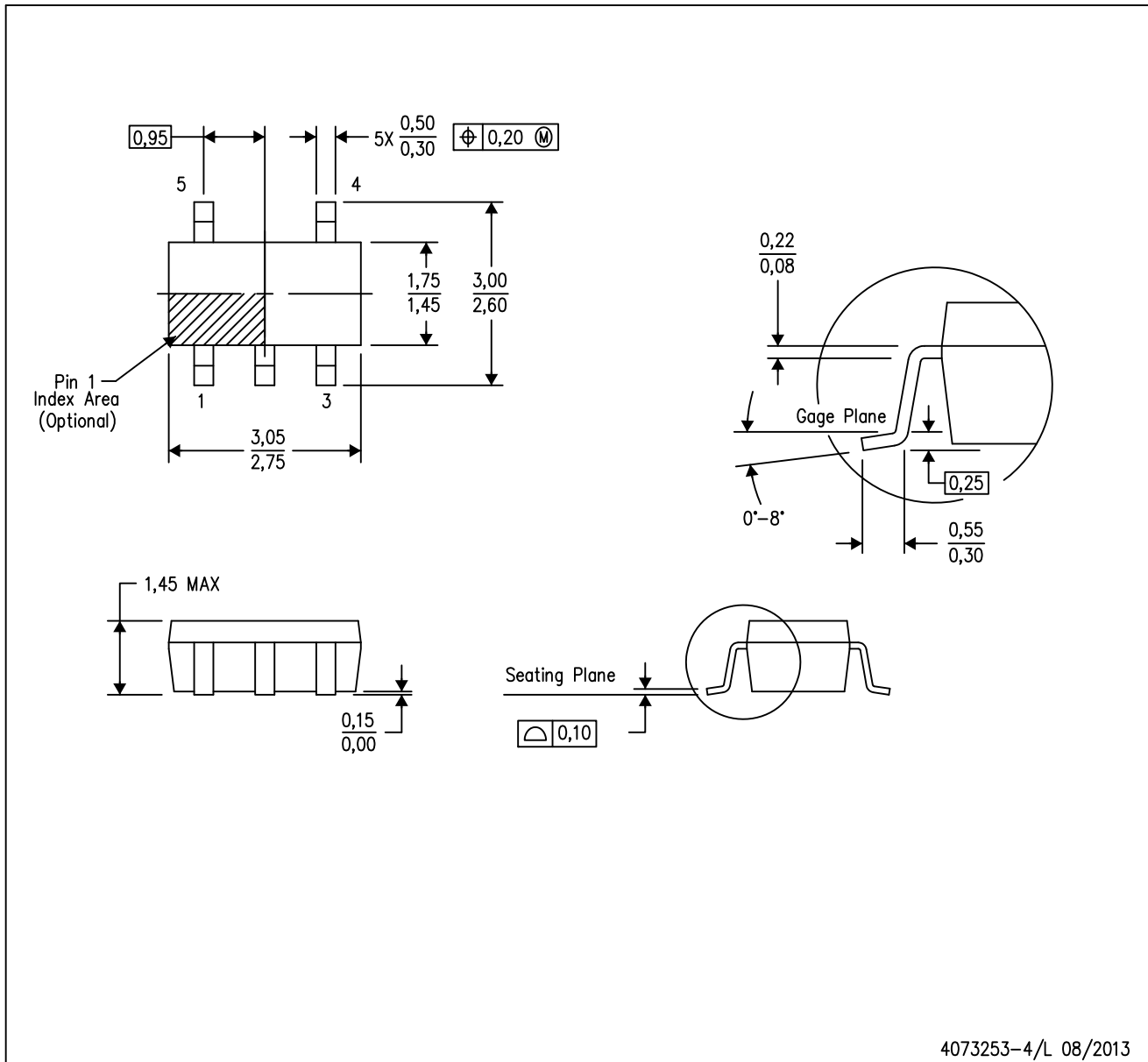
TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM2611AMF	SOT-23	DBV	5	1000	210.0	185.0	35.0
LM2611AMF/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LM2611AMFX/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LM2611BMF	SOT-23	DBV	5	1000	210.0	185.0	35.0
LM2611BMF/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LM2611BMFX/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0

DBV (R-PDSO-G5)

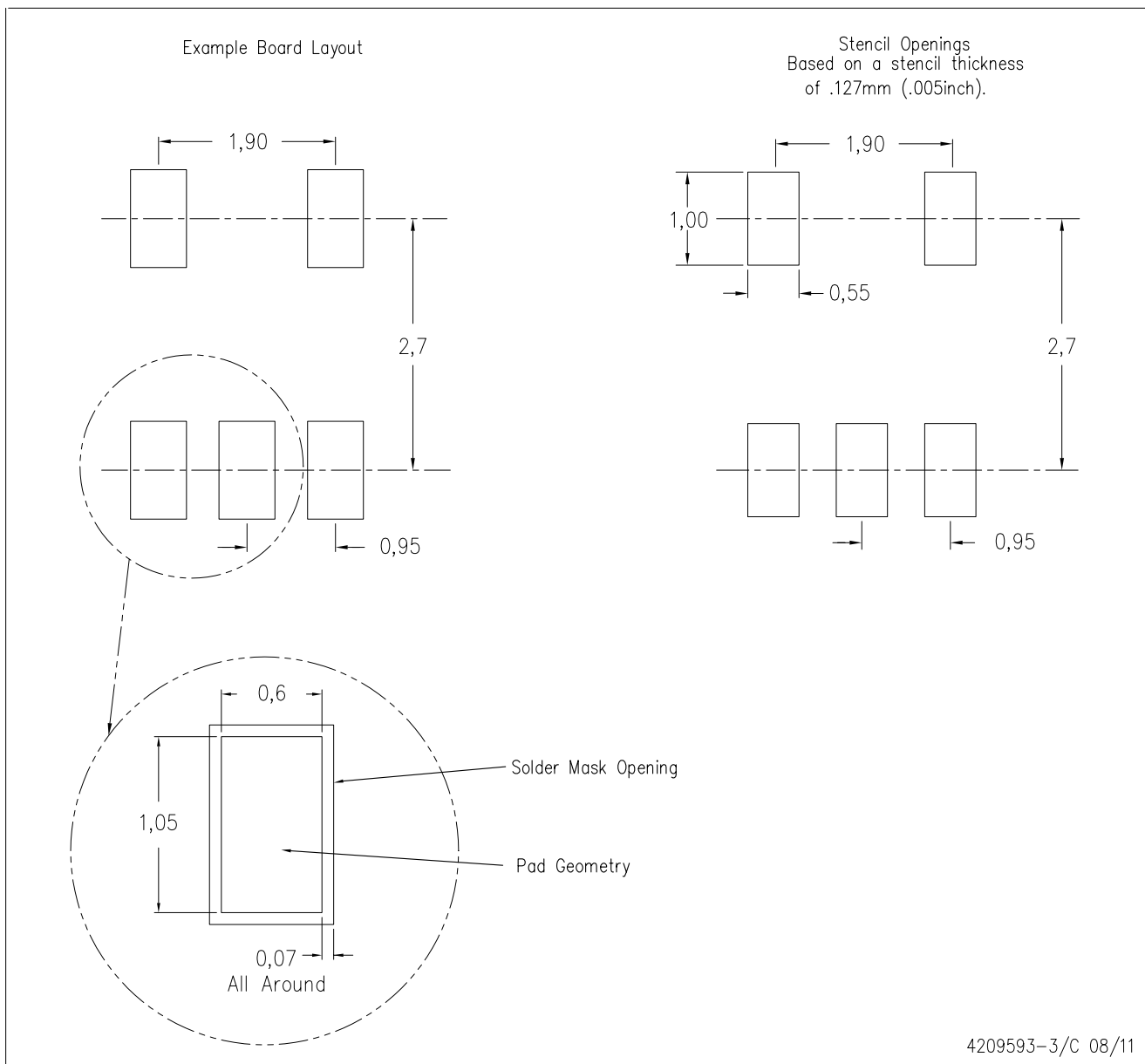
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - D. Falls within JEDEC MO-178 Variation AA.

DBV (R-PDSO-G5)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - D. Publication IPC-7351 is recommended for alternate designs.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

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