PIC24FJ128GA010 Family Silicon Errata and Data Sheet Clarification

The PIC24FJ128GA010 Family devices that you have received conform functionally to the current Device Data Sheet (DS39747**E**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC24F128GA010 family silicon.

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**C2**).

Data Sheet clarifications and corrections start on page 19, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with MPLAB ICD 2 or PICkit™ 3:

1. Using the appropriate interface, connect the device to the MPLAB ICD 2 programmer/debugger or PICkit™ 3.
2. From the main menu in MPLAB IDE, select *Configure>Select Device* and then select the target part number in the dialog box.
3. Select the MPLAB hardware tool (*Debugger>Select Tool*).
4. Perform a "Connect" operation to the device (*Debugger>Connect*). Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note:	If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various PIC24F128GA010 family silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID(1)	Revision ID for Silicon Revision(2)				
		A2	A3	A4	C1	C2
PIC24FJ128GA010	040Dh	02h	03h	07h	43h	44h
PIC24FJ96GA010	040Ch					
PIC24FJ64GA010	040Bh					
PIC24FJ128GA008	040Ah					
PIC24FJ96GA008	0409h					
PIC24FJ64GA008	0408h					
PIC24FJ128GA006	0407h					
PIC24FJ96GA006	0406h					
PIC24FJ64GA006	0405h					

Note 1: The Device IDs (DEVID and DEVREV) are located at the last two implemented addresses in program memory. They are shown in hexadecimal in the format "DEVID DEVREV".

2: Refer to the *"PIC24FJXXXGA0XX Flash Programming Specification"* (DS39768) for detailed information on Device and Revision IDs for your specific device.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions[1]				
				A2	A3	A4	C1	C2
Core	—	1.	SFR write issues in Doze mode.	X	X	X		
I²C™	—	2.	Failure to lock out writes to I2CxTRN.	X				
UART	—	3.	Parity failure with odd values in BRG.	X	X	X		
Resets	—	4.	FSCM clock switch issue.	X				
Timers	—	5.	Special Event Trigger failure (Timer2/3).	X				
SPI	Enhanced mode	6.	Enhanced Buffer modes are unavailable.	X	X	X		
JTAG	Programming	7.	JTAG device programming not compatible with third party solutions.	X	X	X		
A/D	—	8.	High gain error.	X	X	X		
I²C	—	9.	Failure to detect bus collision in Stop or Restart sequences.	X				
UART	—	10.	Erroneous FIFO buffer overflow flag.	X				
SPI	Master mode	11.	Master mode reception errors at fast bit rates.	X	X	X		
CPU	—	12.	Skipped `DISI` instruction under certain circumstances.	X				
PMP	—	13	$\overline{\text{PMRD}}$ signal absent in Master mode under certain conditions.	X	X	X		
PMP	Master mode	14.	Address increment/decrement failure on back-to-back reads in Master mode.	X				
RTCC	—	15.	Missed increments on simultaneous register update.	X				
RTCC	—	16.	Calibration not applied at every interval.	X				
I²C	Slave mode	17.	Failure to Acknowledge write operation in Slave mode.	X				
I²C	—	18.	Receive mode can be enabled outside of Idle state.	X				
UART	—	19.	Change in Sync Break timing.	X	X	X		
UART	—	20.	Reception failures in High-Speed mode.	X	X	X		
UART	—	21.	UTXISEL0 bit always reads as '0'.	X				
UART	—	22.	UTXSEL mode '10' behaves as mode '00'.	X				
UART	HW Flow Control	23.	Hardware flow control unavailable for some devices and some UARTs.	X	X	X		
UART	—	24.	Erroneous baud rate calculations in High-Speed mode.	X	X	X		
UART	Auto-Baud	25.	Insertion of spurious data with auto-baud reception.	X	X	X		
Interrupts	Traps	26.	Failure to exit Doze mode on certain traps.	X	X	X		
Output Compare	—	27.	Single glitch on initialization under certain conditions.	X	X	X		
A/D	INT0 Trigger	28.	Device may not wake when convert on INT0 trigger is selected.	X	X	X		
SPI	Framed modes	29.	Frame Sync unavailable in Master mode under certain conditions.	X	X	X		

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

TABLE 2: SILICON ISSUE SUMMARY (CONTINUED)

Module	Feature	Item Number	Issue Summary	Affected Revisions[1]				
				A2	A3	A4	C1	C2
SPI	Slave mode	30.	Module in Slave mode may ignore $\overline{SSx}$ pin and receive data anyway.	X	X	X		
Oscillator	Two-Speed Start-up	31.	Two-Speed Start-up failure when IESO is enabled.	X	X	X		
Core	Reset	32.	Unimplemented CLKDIV bits reset to '1'.	X	X	X		
Core	Traps	33.	Clock failure trap does not vector as expected.	X	X	X		
Core	Resets	34.	BOR and POR flags are both set on BOR.	X	X	X		
I/O Ports	—	35.	OSCO/CLKO/RC15 driven immediately following POR.	X	X	X		
I^2C	Slave mode	36.	D/$\overline{A}$ bit fails to update in Slave mode transmissions.	X	X	X		
UART	Auto-Baud	37.	Double receive interrupt with auto-baud reception.	X	X	X		
UART	Auto-Baud	38.	Auto-baud calculation errors causing transmit or receive failures.	X	X	X		
UART	—	39.	Erroneous sampling and framing errors when using two Stop bits.	X	X	X	X	X
SPI	—	40.	DISSCK does not disable the SPIx clock.	X	X	X		
Output Compare	PWM mode	41.	Single missed compare events under certain conditions.	X	X	X		
CRC	—	42.	Improper VWORD Reset on FIFO overflow.	X	X	X		
UART	IrDA®	43.	IR baud clock only available during transmit.	X	X			
I^2C	—	44.	Issues with write operations on I2CxSTAT.	X				
I^2C	—	45.	ACKSTAT prematurely cleared in Slave mode.	X	X	X		
RTCC	—	46.	Write errors to ALCFGRPT register.	X	X	X		
Core	Instruction Set	47.	Loop count errors with REPEAT instruction and R-A-W stalls.	X	X	X		
Memory	PSV	48.	False address error traps at lower boundary of PSV space.	X	X	X		
I/O	PORTB	49.	RB5 as an open-drain output stays in high-impedance state.	X	X	X		
RTCC	Alarm	50.	Decrement of alarm repeat counter under certain conditions.	X	X	X	X	X
UART	UERIF Interrupt	51.	No UERIF flag with multiple errors.	X	X	X		
UART	FIFO Error Flags	52.	PERR and FERR not correctly set for all bytes in receive FIFO.	X	X	X		
UART	—	53.	Does not transmit if TxREG is preloaded.	X	X	X		
I^2C	Master mode	54.	Module may respond to its own master transmission as a slave under certain conditions.	X	X	X		
I^2C	Slave mode	55.	Failure to respond correctly to some reserved addresses in 10-bit mode.	X	X	X		

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

TABLE 2: SILICON ISSUE SUMMARY (CONTINUED)

Module	Feature	Item Number	Issue Summary	Affected Revisions[1]				
				A2	A3	A4	C1	C2
I^2C	—	56.	TBF flag error with bus collisions.	X	X	X		
SPI	Master mode	57.	Incorrect status bit timing.	X	X	X		
RTCC	Alarm	58.	Pin toggling error on alarm repeat.		X	X		
I/O Pins	—	59.	Spec change for V_{OL} and V_{OH}.			X		
SPI	Framed modes	60.	Framed SPIx modes are not supported.				X	X
SPI	Enhanced mode	61.	Interrupt flag set early in Enhanced Buffer mode under certain conditions.				X	X
Core	Code Protection	62.	General code protection disables bootloader functionality.				X	
UART	TX Interrupt	63.	A TX interrupt may occur before the data transmission is complete.				X	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

> **Note:** This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**C2**).

1. Module: Core

With Doze mode enabled, DOZEN (CLKDIV<11>) set and the CPU Peripheral Clock Ratio Select bits (CLKDIV<14:12>) configured to any value except '000', writes to SFR locations can not be performed.

Work around

Disable Doze mode or select 1:1 CPU peripheral clock ratio before modifying stated SFR locations, or avoid writing stated locations while Doze mode is enabled and a CPU peripheral clock ratio other than 1:1 is selected. Configure the device prior to entering Doze mode and use the mode only to monitor applications activity.

Affected Silicon Revisions

A2	A3	A4	C1	C2			
X	X	X					

2. Module: I^{2}C™

Writing to I2CxTRN during a Start bit transmission generates a write collision, indicated by the IWCOL (I2CxSTAT<7>) bit being set. In this state, additional writes to the I2CxTRN register should be blocked. However, in this condition, the I2CxTRN register can be written, although transmissions will not occur until the IWCOL bit is cleared in software.

Work around

After each write to the I2CxTRN register, read the IWCOL bit to ensure a collision has not occurred. If the IWCOL bit is set, it must be cleared in software and I2CxTRN must be rewritten.

Affected Silicon Revisions

A2	A3	A4	C1	C2			
X							

3. Module: UART

With the parity option enabled, a parity error, indicated with the PERR bit (UxSTA<3>) being set, may occur if the Baud Rate Generator contains an odd value. This affects both even and odd parity options.

Work around

Load the Baud Rate Generator register, UxBRG, with an even value or disable the peripheral's parity option by loading either '00' or '11' into the Parity and Data Selection bits, PDSEL<1:0> (UxMODE<2:1>).

Affected Silicon Revisions

A2	A3	A4	C1	C2			
X	X	X					

4. Module: Resets

After an oscillator has stopped, with the Fail-Safe Clock Monitor enabled and the FCKSM<1:0> Configuration bits (Flash Configuration Word 2<7:6>) programmed to '00', the system clock source is forced to FRC. After which, the system clock source may not be changed in software by modifying the New Oscillator Selection bits, NOSC<2:0> (OSCCON<10:8>), unless a device Reset occurs.

Work around

Upon detecting an oscillator failure, determined by reading the Clock Fail Detect bit, CF (OSCCON<3>), as set, execute a RESET instruction prior to selecting a new system clock source using the NOSC bits.

Affected Silicon Revisions

A2	A3	A4	C1	C2			
X							

5. Module: Timers

With Timer2 and Timer3 configured in 32-bit mode by setting T2CON<3>, a Special Event Trigger to start an A/D conversion may not occur when the most significant word of the Period register, PR3, is '0'.

Work around

Either write PR3 to a non-zero value or configure Timer3 for 16-bit operation when generating a Special Event Trigger for periodic A/D conversions.

Affected Silicon Revisions

A2	A3	A4	C1	C2			
X							

6. Module: SPI (Enhanced Mode)

The Enhanced SPIx modes, selected by setting the Enhanced Buffer Enable bit, SPIBEN (SPIxCON2<0>), are not available.

Work around

Use Standard SPIx modes by clearing the SPIx Enhanced Buffer Enable bit, SPIBEN.

Affected Silicon Revisions

A2	A3	A4	C1	C2			
X	X	X					

7. Module: JTAG (Programming)

The current JTAG programming implementation is not compatible with third party programmers using SVF (Serial Vector Format) description language. JTAG boundary scan is supported by third party JTAG solutions and is not affected.

Work around

The user can program devices with In-Circuit Serial Programming™. JTAG programming can be accomplished using custom JTAG software. The current implementation may not be supported in future PIC24F revisions. JTAG boundary scan is supported.

Affected Silicon Revisions

A2	A3	A4	C1	C2			
X	X	X					

8. Module: A/D

Gain error may be as high as 5 LSbs for external references ($V_{REF}+$ and $V_{REF}-$) and 6 LSbs for internal reference (AV_{DD} and AV_{SS}).

Work around

Determine gain error from a known reference voltage and compensate the A/D result in software.

Affected Silicon Revisions

A2	A3	A4	C1	C2			
X	X	X					

9. Module: I^{2}C

The I^{2}C module may not detect a bus collision during a Restart or Stop sequence. When this occurs, the Master Bus Collision Detect bit, BCL (I2CxSTAT<10>), may not set. The BCL bit will indicate a bus collision, if it occurs, during a Start sequence. This issue only affects I^{2}C multi-master networks.

Work around

To use the device in an I^{2}C multi-master network, each master device must detect when Start and Stop events occur on the I^{2}C bus. A Start sequence should be initiated only after a Start and a Stop event have been detected to ensure a bus collision can be detected.

Affected Silicon Revisions

A2	A3	A4	C1	C2			
X							

10. Module: UART

The Receive Buffer Overrun Error Status bit, OERR (UxSTA<1>), may set before the UART FIFO has overflowed. After the fourth byte is received by the UART, the FIFO is full. The OERR bit should set after the fifth byte has been received in the UART Shift register. Instead, the OERR bit may set after the fourth received byte with the UART Shift register empty.

Work around

After four bytes have been received by the UART, the UART Receiver Interrupt Flag bit, U1RXIF (IFS0<11>) or U2RXIF (IFS1<14>), will be set, indicating the UART FIFO is full. The OERR bit may also be set. After reading the UART Receive Buffer, UxRXREG, four times to clear the FIFO, clear both the OERR and UxRXIF bits in software.

Affected Silicon Revisions

A2	A3	A4	C1	C2			
X							

11. Module: SPI (Master Mode)

Master mode receptions using the SPI1 and SPI2 modules may not function correctly for bit rates above 8 Mbps if the master has the SMP bit (SPIxCON1<9>) cleared (master samples data at the middle of the serial clock period).

In this case, the data transmitted by the slave is received, shifted right by one bit, by the master. For example, if the data transmitted by the slave was 0xAAAA, the data received by the master would be 0x5555 (0xAAAA shifted right by one bit).

Work around

Users may set up the SPIx module so that the bit rate is 8 Mbps or lower.

Alternatively, the bit rate can be configured higher than 8 Mbps, but the SMP bit (SPIxCON1<9>) of the SPIx master must be set (master samples data at the end of the serial clock period).

Affected Silicon Revisions

A2	A3	A4	C1	C2			
X	X	X					

12. Module: CPU

A `DISI` instruction may be ignored if the command is executed in the same instruction cycle as when the DISICNT register decrements to zero. For example, if a `DISI #5` instruction is performed, the DISICNT will decrement to zero in six instruction cycles (5 instruction cycles for the `DISI` command plus 1 for the instruction execution). If a second `DISI` command executes in the same instruction cycle that DISCNT reaches zero, the second `DISI` instruction will be ignored. In any other instruction cycle, the second `DISI` command will perform as described in the product data sheet.

Work around

To disable interrupts using the `DISI` instruction, execute the instruction twice. For example, to disable interrupts for five instruction cycles, use the following:

`DISI #2` (can be any value except 0)

`DISI #5` (number of instruction cycles `DISI` will be active)

This work around ensures a `DISI` command is not executed in the same instruction cycle as when the DISICNT register decrements to zero.

Affected Silicon Revisions

A2	A3	A4	C1	C2			
X							

13 Module: PMP

In Master mode (MODE<1:0> = `11` or `10`), back-to-back operations may cause the $\overline{\text{PMRD}}$ signal to not be generated. This limitation occurs when the peripheral is configured for zero Wait states (WAITM<3:0> = `0000`).

Work around

The $\overline{\text{PMRD}}$ signal will be generated correctly if a minimum of one instruction cycle delay is inserted between the back-to-back operations. A `NOP` instruction, or any other instruction, is adequate. Selecting a delay other than zero will also permit the $\overline{\text{PMRD}}$ signal to be generated.

Affected Silicon Revisions

A2	A3	A4	C1	C2			
X	X	X					

14. Module: PMP (Master Mode)

With the PMP in Master mode (MODE<1:0> = `11` or `10`) with the increment/decrement feature enabled (INCM<1:0> = `01` or `10`), the address may not automatically change when the PMDINx register is read. This issue may occur when multiple back-to-back reads are performed.

Work around

The PMP address will be generated correctly if a minimum of one instruction cycle delay is inserted between the back-to-back read operations of the PMDINx register. A `NOP` instruction, or any other instruction, is adequate.

Affected Silicon Revisions

A2	A3	A4	C1	C2			
X							

15. Module: RTCC

An RTCC increment may be missed if an RTCC update and an RTCC increment occur at the same time, and updates are disallowed (RTCWREN = `0`). In this condition, the RTCC is not updated since the RTCWREN bit is clear.

Work around

Prior to writing to the RTCVAL registers, verify that the RTCSYNC bit is clear and the RTCWREN bit is set. This ensures that the RTCC will be updated and the update will not occur during an RTCC increment.

Affected Silicon Revisions

A2	A3	A4	C1	C2			
X							

16. Module: RTCC

The RTCC automatic calibration, stored in the CAL<7:0> bits, is intended to be applied every minute on the minute boundary. The calibration is applied after the first minute but may not occur on subsequent minute intervals.

Work around

Read and rewrite the SECONDS (RTCPTR<1:0> = `00`) value after each minute. This reinitializes the calibration circuit and allows the calibration to be applied to the next minute increment.

Affected Silicon Revisions

A2	A3	A4	C1	C2			
X							

17. Module: I²C (Slave Mode)

In I²C Slave mode, the I²C peripheral may not Acknowledge a write operation (R/W = `0`) after a Restart has been received. This sequence is typically used to perform a slave transmit operation in 10-Bit Addressing mode (A10M = `1`). Attempting to perform a write operation after a Restart may cause the peripheral to generate a NACK and end the operation unexpectedly.

Work around

To perform an I²C slave transmit, refer to Figure 24-27 from **Section 24. "Inter-Integrated Circuit™ (I²C™)"** in the *"PIC24F Family Reference Manual"* (DS39702).

Affected Silicon Revisions

A2	A3	A4	C1	C2			
X							

18. Module: I²C

I²C Receive mode should be enabled (i.e., RCEN bit should be set) only when the system is Idle (i.e., when ACKEN, RCEN, PEN, RSEN and SEN all equal zero). It should not be possible to set the RCEN bit when the system is not Idle; however, the RCEN bit can be set under this circumstance.

Work around

Wait for the system to become Idle before setting the RCEN bit. Verify that the following bits are clear:

ACKEN, RCEN, PEN, RSEN and SEN.

Affected Silicon Revisions

A2	A3	A4	C1	C2			
X							

19. Module: UART

The timing for transmitting a Sync Break has changed for this revision of silicon. The Sync Break is transmitted as soon as the UTXBRK bit is set. A dummy write to UxTXREG is still required and must be performed before the Sync Break has finished transmitting. Otherwise, the UxTX may be held in the active state until the write has occurred.

Work around

Set the UTXBRK bit when a Sync Break is required and perform a dummy write to UxTXREG immediately following. This sequence will avoid holding the UxTX pin in the active state.

Affected Silicon Revisions

A2	A3	A4	C1	C2			
X	X	X					

20. Module: UART

When the UART is in High-Speed mode, BRGH (UxMODE<3>) is set, some optimal UxBRG values can cause reception to fail.

Work around

Test UxBRG values in the application to find a UxBRG value that works consistently for more high-speed applications. The user should verify that the UxBRG baud rate error does not exceed the application limits.

Affected Silicon Revisions

A2	A3	A4	C1	C2			
X	X	X					

21. Module: UART

The UTXISEL0 bit (UxSTA<13>) always reads as zero, regardless of the value written to it. The bit can be written to either a '0' or '1', but will always read zero. This will affect read-modify-write operations, such as bit-wise or shift operations. Using a read-modify-write instruction on the UxSTA register will always write the UTXISEL0 bit to zero.

Work around

If a UTXISEL0 value of '1' is needed, avoid using read-modify-write instructions on the UxSTA register. Copy the UxSTA register to a temporary variable and set UxSTA<13> prior to performing read-modify-write operations. Copy the new value back to the UxSTA register.

Affected Silicon Revisions

A2	A3	A4	C1	C2			
X							

22. Module: UART

When UTXISEL<1:0> = 10, a UART interrupt flag should be set after one byte from the FIFO is transferred to the Transmit Shift Register (TSR). Instead, the interrupt flag may be set only after all bytes are transferred from the FIFO and the FIFO is empty. This behavior is similar to the UTXISEL<1:0> = 00 mode.

Work around

None.

Affected Silicon Revisions

A2	A3	A4	C1	C2			
X							

23. Module: UART (Hardware Flow Control)

UART1 and UART2 hardware flow control options are not available for the 64-pin variants of the PIC24F128GA010 product family. As a result, the $\overline{\text{UxCTS}}$ and $\overline{\text{UxRTS}}$ pins are not available and the UEN<1:0> control bits are read as '0' (unimplemented). UART2 hardware flow control is not available for the 80-pin PIC24F128GA010 family variants. Associated pins and bits are not available for these devices.

Work around

None.

Affected Silicon Revisions

A2	A3	A4	C1	C2			
X	X	X					

24. Module: UART

When the UART is in High-Speed mode (BRGH = 1), the auto-baud sequence can calculate the baud rate as if it were in Low-Speed mode.

Work around

The calculated baud rate can be modified by the following equation:

$$\text{New BRG Value} = (\text{Auto-Baud BRG} + 1) * 4 \cdot 1$$

The user should verify that the baud rate error does not exceed application limits.

Affected Silicon Revisions

A2	A3	A4	C1	C2			
X	X	X					

25. Module: UART (Auto-Baud)

With the auto-baud feature selected, the Sync Break character (0x55) may be loaded into the FIFO as data.

Work around

To prevent the Sync Break character from being loaded into the FIFO, load the UxBRG register with either 0x0000 or 0xFFFF prior to enabling the auto-baud feature (ABAUD = 1).

Affected Silicon Revisions

A2	A3	A4	C1	C2			
X	X	X					

26. Module: Interrupts (Traps)

The device may not exit Doze mode if certain trap conditions occur. Address error, stack error and math error traps are affected. Oscillator failure and all interrupt sources are not affected and can cause the device to correctly exit Doze mode.

Work around

None.

Affected Silicon Revisions

A2	A3	A4	C1	C2			
X	X	X					

27. Module: Output Compare

The output compare module may output a single glitch for one T_{CY} after the module is enabled (OCM<2:0> = 000). This issue occurs when the output state of the associated Data Latch register (LATx) is in the opposite state of the Output Compare mode when the peripheral is enabled. It can also occur when switching between two Output Compare modes with opposite output states.

Work around

If the output glitch must be avoided, verify that the associated data latch value of the OCx pin matches the initial state of the desired Output Compare mode. For example, if Output Compare 5 is configured for mode, OCM<2:0> = 001, ensure that the LATD<4> bit is clear prior to writing the OCM bits. The port latch output value will match the initial output state of the OC5 pin and avoid the glitch when the peripheral is enabled.

Affected Silicon Revisions

A2	A3	A4	C1	C2			
X	X	X					

28. Module: A/D (INT0 Trigger)

With the External Interrupt 0 (INT0) selected to start an A/D conversion (SSRC<2:0> = 001), the device may not wake up from Sleep or Idle mode if more than one conversion is selected per interrupt (SMPI<3:0> <> 0000). Interrupts are generated correctly if the device is not in Sleep or Idle mode.

Work around

Configure the A/D to generate an interrupt after every conversion (SMPI<3:0> = 0000). Use another wake-up source, such as the WDT or another interrupt source, to exit the Sleep or Idle mode. Alternatively, perform A/D conversions in Run mode.

Affected Silicon Revisions

A2	A3	A4	C1	C2			
X	X	X					

29. Module: SPI (Framed Modes)

A frame synchronization pulse may not be output in SPIx Master mode if the pulse is selected to coincide with the first bit clock (SPIFE = 1). SCKx and SDOx waveforms are not affected.

Work around

Select the frame synchronization pulses to precede the first bit clock (SPIFE = 0). The frame pulses will output correctly as described in the product data sheet.

Affected Silicon Revisions

A2	A3	A4	C1	C2			
X	X	X					

30. Module: SPI (Slave Mode)

In SPIx Slave mode (MSTEN = 0), with the slave select option enabled (SSEN = 1), the peripheral may accept transfers regardless of the $\overline{\text{SSx}}$ pin state. The received data in SSPxBUF will be accurate but not intended for the device.

Work around

If the Slave select option is required (e.g., the device is one of multiple SPIx slave nodes on an SPIx network), two potential work arounds exist:

1. Configure the port associated with $\overline{\text{SSx}}$ to an input and periodically read the PORT register. If the pin is read '0', disable the SPIx peripheral (SPIEN = 0). Enable the peripheral (SPIEN = 1) if the pin is read as a logic '1'.
2. Read the pin associated with $\overline{\text{SSx}}$ after a transfer is complete, indicated by the SPIxF bit being set. If the port pin is read as a digital '1', read SSPxBUF and discard the contents.

Affected Silicon Revisions

A2	A3	A4	C1	C2			
X	X	X					

31. Module: Oscillator (Two-Speed Start-up)

The Two-Speed Start-up feature may not be available on exit from Sleep mode with the IESO bit (Internal External Switchover mode) enabled. Upon wake-up, the device will wait for the clock source used prior to entering Sleep mode to become ready.

Work around

None.

Affected Silicon Revisions

A2	A3	A4	C1	C2			
X	X	X					

32. Module: Core (Reset)

The CLKDIV register Reset value is incorrect. The register will reset with unimplemented bits equal to '1' for all Resets.

Work around

Mask out unimplemented bits to maintain software compatibility with future device revisions.

Affected Silicon Revisions

A2	A3	A4	C1	C2			
X	X	X					

33. Module: Core (Traps)

If a clock failure occurs when the device is in Idle mode, the oscillator failure trap does not vector to the Trap Service Routine (TSR). Instead, the device will simply wake-up from Idle mode and continue code execution if the Fail-Safe Clock Monitor (FSCM) is enabled.

Work around

Whenever the device wakes up from Idle (assuming the FSCM is enabled), the user software should check the status of the OSCFAIL bit (INTCON1<1>) to determine whether a clock failure occurred and then perform an appropriate clock switch operation.

Affected Silicon Revisions

A2	A3	A4	C1	C2			
X	X	X					

34. Module: Core (Resets)

On a Brown-out Reset, both the BOR and POR bits may be set. This may cause the Brown-out Reset condition to be indistinguishable from the Power-on Reset.

Work around

None.

Affected Silicon Revisions

A2	A3	A4	C1	C2			
X	X	X					

35. Module: I/O Ports

During Power-on Reset (POR), the device may drive the OSCO/CLKO/RC15 pin as a clock out output for approximately 20 μs. During this time, the pin will be driven high and low rather than being set to high-impedance. This may cause issues on designs that use the pin as a general purpose I/O. Designs should be reviewed to ensure that their intended operation will not be disrupted if the pin is driven during POR.

Work around

None.

Affected Silicon Revisions

A2	A3	A4	C1	C2			
X	X	X					

36. Module: I²C (Slave Mode)

During I²C Slave mode transactions, the Data/Address bit, D/$\overline{A}$, may not update during the data frame. This affects both 7 and 10-Bit Addressing modes.

I²C slave receptions are not affected by this issue.

Work around

Use the Read/$\overline{\text{Write}}$ bit, R/$\overline{W}$, and the Transmit Buffer Full Status Bit, TBF, to determine whether address or data information is being received.

For more information, see Figure 24-30 and Figure 24-31 in **Section 24. *"Inter-Integrated Circuit™ (I²C™)"*** (DS39702).

Affected Silicon Revisions

A2	A3	A4	C1	C2			
X	X	X					

37. Module: UART (Auto-Baud)

When an auto-baud is detected, the receive interrupt may occur twice. The first interrupt occurs at the beginning of the Start bit and the second after reception of the Sync field character.

Work around

If a receive interrupt occurs, check the URXDA bit (UxSTA<0>) to ensure that valid data is available. On the first interrupt, no data will be present. The second interrupt will have the Sync field character (55h) in the receive FIFO.

Affected Silicon Revisions

A2	A3	A4	C1	C2			
X	X	X					

38. Module: UART (Auto-Baud)

The auto-baud may miscalculate for certain baud rates and clock speed combinations, resulting in a BRG value that is 1 greater or less than the expected value. When UxBRG is less than 50, this can result in transmission and reception failures due to introducing error greater than 1%.

Work around

Test auto-baud calculations at various clock speed and baud rate combinations that would be used in applications. If an inaccurate UxBRG value is generated, manually correct the baud rate in user code.

Affected Silicon Revisions

A2	A3	A4	C1	C2			
X	X	X					

39. Module: UART

When the UART uses two Stop bits (STSEL = 1), it may sample the first Stop bit instead of the second one. If the device being communicated with is using one Stop bit in its communications, this may lead to framing errors.

Work around

None.

Affected Silicon Revisions

A2	A3	A4	C1	C2			
X	X	X	X	X			

40. Module: SPI

In SPIx Master mode, the Disable SCKx pin bit, DISSCK, may not disable the SPIx clock. As a result, the PIC® microcontroller must provide the SPIx clock in Master mode.

Work around

None.

Affected Silicon Revisions

A2	A3	A4	C1	C2			
X	X	X					

41. Module: Output Compare (PWM Mode)

In PWM mode, the output compare module may miss a compare event when the current duty cycle register (OCxRS) value is 0x0000 (0% duty cycle) and the OCxRS register is updated with a value of 0x0001. The compare event is only missed the first time a value of 0x0001 is written to OCxRS and the PWM output remains low for one PWM period. Subsequent PWM high and low times occur as expected.

Work around

If the current OCxRS register value is 0x0000, avoid writing a value of 0x0001 to OCxRS. Instead, write a value of 0x0002. In this case, however, the duty cycle will be slightly different from the desired value.

Affected Silicon Revisions

A2	A3	A4	C1	C2			
X	X	X					

42. Module: CRC

If a CRC FIFO overflow occurs, the VWORD indicator will reset to '1' instead of '0'. Further writes to the FIFO will cause the VWORD indicator to reset to '0' after seven writes are performed.

Work around

Poll the CRCFUL bit (CRCCON<7>) to ensure that no writes are performed on the FIFO when it is full.

Affected Silicon Revisions

A2	A3	A4	C1	C2			
X	X	X					

43. Module: UART (IrDA®)

When the UART is configured for IrDA interface operations (UxMODE<9:8> = 11), the 16x baud clock signal on the BCLKx pin will only be present when the module is transmitting. The pin will be Idle at all other times.

Work around

Configure one of the output compare modules to generate the required baud clock signal when the UART is receiving data or in an Idle state.

Affected Silicon Revisions

A2	A3	A4	C1	C2			
X	X						

44. Module: I^{2}C

Bit and byte-based operations may not have the intended affect on the I2CxSTAT register. It is possible for bit and byte operations performed on the lower byte of I2CxSTAT to clear the BCL bit (I2CxSTAT<10>). Bit and byte operation performed on the upper byte of I2CxSTAT, or on the BCL bit directly, may not be able to clear the BCL bit.

Work around

Modifications to the I2CxSTAT register should be done using word writes only. This can be done in 'C' by always writing to the register itself and not the individual bits. For example, the code:

```
I2C1STAT &= 0xFBFF
```

forces the compiler to use a word-based operation to clear the BCL bit. In assembly, it is done by not using `BSET` or `BCLR` instructions. or instructions with the `.b` modifier.

Affected Silicon Revisions

A2	A3	A4	C1	C2			
X							

45. Module: I^{2}C

After the ACKSTAT bit is set, while receiving a NACK from the master or a slave, it may be cleared by the reception of a Start or Stop bit.

Work around

Store the value of the ACKSTAT bit immediately after receiving a NACK.

Affected Silicon Revisions

A2	A3	A4	C1	C2			
X	X	X					

46. Module: RTCC

When performing writes to the ALCFGRPT register, some bits may become corrupted. The error occurs because of desynchronization between the CPU clock domain and the RTCC clock domain.

The error causes data from the instruction *following* the ALCFGRPT instruction to overwrite the data in ALCFGRPT.

Work around

Always follow writes to the ALCFGRPT register with an additional write of the same data to a dummy location. These writes can be performed to RAM locations, W registers or unimplemented SFR space.

The optimal way to perform the work around:

1. Read ALCFGRPT into a RAM location.
2. Modify the ALCFGRPT data, as required, in RAM.
3. Move the RAM value into ALCFGRPT and a dummy location in back-to-back instructions.

Affected Silicon Revisions

A2	A3	A4	C1	C2			
X	X	X					

47. Module: Core (Instruction Set)

If an instruction producing a read-after-write stall condition is executed inside a REPEAT loop, the instruction will be executed fewer times than was intended. For example, this loop:

```
repeat #0xf
inc [w1],[++w1]
```

will execute less than 15 times.

Work around

Avoid using REPEAT to repetitively execute instructions that create a stall condition. Instead, use a software loop using conditional branches.

Affected Silicon Revisions

A2	A3	A4	C1	C2			
X	X	X					

48. Module: Memory (Program Space Visibility)

When accessing data in the PSV area of data RAM, it is possible to generate a false address error trap condition by reading data located precisely at the lower address boundary (8000h). If data is read using an instruction with an auto-decrement, the resulting RAM address will be below the PSV boundary (i.e., at 7FFEh); this will result in an address error trap.

This false address error can also occur if a 32-bit MOV instruction is used to read the data at location 8000h.

Work around

Do not use the first location of a PSV page (address 8000h).

Affected Silicon Revisions

A2	A3	A4	C1	C2			
X	X	X					

49. Module: I/O (PORTB)

When RB5 is configured as an open-drain output, it remains in a high-impedance state. The settings of LATB5 and TRISB5 have no effect on the pin's state.

Work around

If open-drain operation is not required, configure RB5 as a regular I/O (ODCB<5> = 0).

If open-drain operation is required, there are two options:

- select a different I/O pin for the open-drain function; or
- place an external transistor on the pin and configure the pin as a regular I/O.

Affected Silicon Revisions

A2	A3	A4	C1	C2			
X	X	X					

50. Module: RTCC (Alarm)

Under certain circumstances, the value of the Alarm Repeat Counter (ALCFGRPT<7:0>) may be unexpectedly decremented. This happens only when a byte write to the upper byte of ALCFGRPT is performed in the interval between a device POR/BOR and the first edge from the RTCC clock source.

Work around

Do not perform byte writes on ALCFGRPT, particularly the upper byte.

Alternatively, wait until one period of the SOSC has completed before performing byte writes to ALCFGRPT.

Affected Silicon Revisions

A2	A3	A4	C1	C2			
X	X	X	X	X			

51. Module: UART (UERIF Interrupt)

The UART error interrupt may not occur, or occur at an incorrect time, if multiple errors occur during a short period of time.

Work around

Read the error flags in the UxSTA register whenever a byte is received to verify the error status. In most cases, these bits will be correct, even if the UART error interrupt fails to occur. For possible exceptions, refer to Errata # 52.

Affected Silicon Revisions

A2	A3	A4	C1	C2			
X	X	X					

52. Module: UART (FIFO Error Flags)

Under certain circumstances, the PERR and FERR error bits may not be correct for all bytes in the receive FIFO. This has only been observed when both of the following conditions are met:

- the UART receive interrupt is set to occur when the FIFO is full or ¾ full (UxSTA<7:6> = `1x`); and
- more than 2 bytes with an error are received.

In these cases, only the first two bytes with a parity or framing error will have the corresponding bits indicate correctly. The error bits will not be set after this.

Work around

None.

Affected Silicon Revisions

A2	A3	A4	C1	C2			
X	X	X					

53. Module: UART

The UART may not transmit if data is written to TXxREG before the module is enabled.

Work around

To ensure transmission occurs, always enable the UART before the buffer is loaded. Use the procedure in **Section 16.2 "Transmitting in 8-Bit Data Mode"** or **Section 16.3 "Transmitting in 9-Bit Data Mode"** of the device data sheet (DS39747).

Affected Silicon Revisions

A2	A3	A4	C1	C2			
X	X	X					

54. Module: I^{2}C (Master Mode)

Under certain circumstances, a module operating in Master mode may Acknowledge its own command addressed to a slave device. This happens when the following occurs:

- 10-Bit Addressing mode is used (A10M = `1`); and
- the I^{2}C master has the same two upper address bits (I2CADD<9:8>) as the addressed slave module.

In these cases, the master also Acknowledges the address command and generates an erroneous I^{2}C slave interrupt, as well as the I^{2}C master interrupt.

Work around

Several options are available:

- When using 10-Bit Addressing mode, make certain that the master and slave devices do not share the same 2 MSbs of their addresses.

If this cannot be avoided:

- Clear the A10M bit (I2CxCON<10> = `0`) prior to performing a Master mode transmit.
- Read the ADD10 bit (I2CxSTAT<8>) to check for a full 10-bit match whenever a slave I^{2}C interrupt occurs on the master module.

Affected Silicon Revisions

A2	A3	A4	C1	C2			
X	X	X					

55. Module: I^{2}C (Slave Mode)

Under certain circumstances, a module operating in Slave mode may not respond correctly to some of the special addresses reserved by the I^{2}C protocol. This happens when the following occurs:

- 10-Bit Addressing mode is used (A10M = `1`); and
- the A<7:1> bits of the slave address (I2CADD<7:1>) fall into the range of the reserved 7-bit address ranges: '`1111xxx`' or '`0000xxx`'.

In these cases, the Slave module Acknowledges the command and triggers an I^{2}C slave interrupt; it does *not* copy the data into the I2CxRCV register or set the RBF bit.

Work around

Do not set bits, A<7:1>, of the module's slave address equal to '`1111xxx`' or '`0000xxx`'.

Affected Silicon Revisions

A2	A3	A4	C1	C2			
X	X	X					

56. Module: I^2C

The Transmit Buffer Full (TBF) flag (I2CxSTAT<0>) may not be cleared by hardware if a collision on the I^2C bus occurs before the first falling clock edge during a transmission.

Work around

None.

Affected Silicon Revisions

A2	A3	A4	C1	C2			
X	X	X					

57. Module: SPI (Master Mode)

In Master mode, the SPIx Interrupt Flag (SPIxIF) and the SPIRBF bit (SPIxSTAT<0>) may both become set one-half clock cycle early, instead of on the clock edge. This occurs only under the following circumstances:

- Enhanced Buffer mode is disabled (SPIBEN = 0); and
- the module is configured for serial data output changes on transition from clock active to clock Idle state (CKE = 1)

If the application is using the interrupt flag to determine when data to be transmitted is written to the transmit buffer, the data currently in the buffer may be overwritten.

Work around

Before writing to the SPIx buffer, check the SCKx pin to determine if the last clock edge has passed. Example 1 (below) demonstrates a method for doing this. In this example, the RD1 pin functions as the SPIx clock, SCKx, which is configured as Idle low.

Affected Silicon Revisions

A2	A3	A4	C1	C2			
X	X	X					

EXAMPLE 1: CHECKING THE STATE OF SPIxIF AGAINST THE SPIx CLOCK

```
while(IFS0bits.SPI1IF == 0){}     //wait for the transmission to complete
while(PORTDbits.RD1 == 1){}       //wait for the last clock to finish
SPI1BUF = 0xFF;                   //write new data to the buffer
```

58. Module: RTCC (Alarm)

The RTCC alarm repeat will generate an incorrect number of pin toggles. If the repeat count (x) is even, it will toggle the alarm pin 'x' times. If the repeat count is odd, one less than x toggles will be observed (x – 1).

Work around

None at this time.

Affected Silicon Revisions

A2	A3	A4	C1	C2			
	X	X					

59. Module: I/O Pins

The I/O pin output, V_{OL}, meets the specifications in Table 3 below.

Work around

None.

Affected Silicon Revisions

A2	A3	A4	C1	C2			
		X					

TABLE 3: DC CHARACTERISTICS: I/O PIN OUTPUT SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ T_A ≤ +85°C for Industrial				
Param No.	Sym	Characteristic	Min	Typ[1]	Max	Units	Conditions
	V_{OL}	**Output Low Voltage**					
DO10		All I/O Pins	—	—	.55	V	I_{OL} = 8.5 mA, V_{DD} = 3.6V
			—	—	.4	V	I_{OL} = 7.8 mA, V_{DD} = 3.6V
			—	—	.55	V	I_{OL} = 6.0 mA, V_{DD} = 2.0V
			—	—	.4	V	I_{OL} = 5.0 mA, V_{DD} = 2.0V

Note 1: Data in "Typ" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

60. Module: SPI (Framed SPIx Modes)

Framed SPIx modes, as described in the device data sheet, are not supported. When using the module, verify the FRMEN bit (SPIxCON2<15>) is cleared.

All other SPIx modes function as described.

Work around

None.

Affected Silicon Revisions

A2	A3	A4	C1	C2			
			X	X			

61. Module: SPI (Enhanced Mode)

SPIx operating in Enhanced Buffer mode (SPIBEN = `1`) may set the interrupt flag, SPIxIF, before the last bit has been transmitted from the Shift register. This issue only affects one of the eight interrupt modes, SISEL<2:0> = `101`, which generates an interrupt when the last bit has shifted out of the Shift register, indicating the transfer is complete. All other interrupt modes in Enhanced Buffer mode work as described in the device data sheet.

Work around

Multiple work arounds are available. Select another Buffer Interrupt mode using the SISEL<2:0> bits in the SPIxSTAT register. A comparable mode is to generate an interrupt when the FIFO is empty (SISEL<2:0> = `110`). Another option is to monitor the SRMPT bit (SPIxSTAT<7>) to determine when the Shift register is empty.

Affected Silicon Revisions

A2	A3	A4	C1	C2			
			X	X			

62. Module: Core (Code Protection)

When general segment code protection has been enabled (GCP Configuration bit is programmed), applications are unable to write to the first 512 bytes of the program memory space (0000h through 0200h). In applications that may require the interrupt vectors to be changed during run time, such as bootloaders, modifications to the interrupt vector tables will not be possible.

Work around

Create two new interrupt vector tables, one each for the IVT and AIVT, in an area of program space beyond the affected region. Map the addresses in the old vector tables to the new tables. These new tables can then be modified as needed to the actual addresses of the ISRs.

Affected Silicon Revisions

A2	A3	A4	C1	C2			
			X				

63. Module: UART (Transmit Interrupt)

When using UTXISEL<1:0> = `01` (interrupt when the last character is shifted out of the Transmit Shift register) and the final character is being shifted out through the Transmit Shift Register (TSR), the TX interrupt may occur before the final bit is shifted out.

Work around

If it is critical that the interrupt processing occurs only when all transmit operations are complete, after which the following work around can be implemented:

Hold off the interrupt routine processing by adding a loop at the beginning of the routine that polls the Transmit Shift register empty bit, as shown in Example 2.

Affected Silicon Revisions

A2	A3	A4	C1	C2			
			X	X			

EXAMPLE 2: DELAYING THE ISR BY POLLING THE TRMT BIT

```
// in UART2 initialization code
...
U2STAbits.UTXISEL0  = 1;          // Set to generate TX interrupt when all
U2STAbits.UTXISEL1  = 0;          // transmit operations are complete.
...

U2TXInterrupt(void)
{
    while(U2STAbits.TRMT==0);     // wait for the transmit buffer to be empty
    ...                           // process interrupt
```

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS39747**E**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

None.

APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (6/2009)

Initial release of this document; issued for revision C2. Incorporates the following current and historical silicon issues from revisions A2, A3, A4 and C1:

- 1 (Core)*
- 2 (I^2C)
- 3 (UART)
- 4 (Resets)
- 5 (Timers)
- 6 (SPI – Enhanced Mode)*
- 7 (JTAG – Programming)*
- 8 (A/D)
- 9 (I^2C)
- 10 (UART)
- 11 (SPI – Master Mode)*
- 12 (CPU)
- 13-14 (PMP – Master Mode)*
- 15-16 (RTCC)
- 17 (I^2C– Slave Mode)*
- 18 (I^2C)
- 19-22 (UART)*
- 23 (UART– Hardware Flow Control)*
- 24 (UART)
- 25 (UART– Auto-Baud)*
- 26 (Interrupts – Traps)*
- 27 (Output Compare)
- 28 (A/D – INT0 Trigger)*
- 29 (SPI – Framed Modes)*
- 30 (SPI – Slave Mode)
- 31 (Oscillator – Two-Speed Start-up)*
- 32, 34 (Core – Reset)
- 33 (Core – Traps)*
- 35 (I/O Ports)
- 36 (I^2C – Slave Mode)*
- 37-38 (UART– Auto-Baud)*
- 39 (UART)
- 40 (SPI)
- 41 (Output Compare – PWM Mode)*
- 42 (CRC)
- 43 (UART– IrDA) *
- 44-45 (I^2C)
- 46 (RTCC)
- 47 (Core – Instruction Set)
- 48 (Memory – Program Space Visibility)
- 49 (I/O – PORTB)
- 50 (RTCC– Alarm)*
- 51 (UART – UERIF Interrupt)
- 52 (UART – FIFO Error Flags)
- 53 (UART)
- 54 (I^2C – Master Mode)
- 55 (I^2C – Slave Mode)
- 56 (I^2C)
- 57 (SPI – Master Mode)
- 58 (RTCC– Alarm)*
- 59 (I/O Pins)
- 60 (SPI – Framed SPIx Modes)
- 61 (SPI– Enhanced Mode)*
- 62 (Core – Code Protection).

Issues marked with * have had additional descriptive text added to their titles, but are otherwise unchanged from the original publication.

Issues 39 (UART) and 45 (I^2C) have been revised with updated language that reflects a more complete understanding of their scope and/or root causes.

A previous issue from revision A2 (I^2C) has been deleted as a duplicate of issue 45.

This document replaces these errata documents:

- *"PIC24FJ128GA010 Family Rev. A2 Silicon Errata"* (DS80275)
- *"PIC24FJ128GA010 Family Rev. A3 Silicon Errata"* (DS80295)
- *"PIC24FJ128GA010 Family Rev. A4 Silicon Errata"* (DS80330)
- *"PIC24FJ128GA010 Family Rev. C1 Silicon Errata"* (DS80422)

Rev B Document (11/2011)

Adds silicon issue 63 (UART – Transmit Interrupt) to silicon revision C1 and C2.

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
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