



# PIC18F23/43K20

## PIC18F23/43K20 Family Silicon Errata and Data Sheet Clarification

The PIC18F23/43K20 family devices that you have received conform functionally to the current Device Data Sheet (DS41303G), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in [Table 1](#). The silicon issues are summarized in [Table 2](#).

The errata described in this document will be addressed in future revisions of the PIC18F23/43K20 silicon.

**Note:** This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of [Table 2](#) apply to the current silicon revision (**B0**).

Data Sheet clarifications and corrections start on page 6, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers and emulation tools, which are available at the Microchip corporate web site ([www.microchip.com](http://www.microchip.com)).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with MPLAB ICD 2, MPLAB ICD 3, PICkit™ 2 or PICkit 3:

1. Using the appropriate interface, connect the device to the MPLAB ICD 2 programmer/debugger, PICkit 2 or PICkit 3.
2. From the main menu in MPLAB IDE, select Configure>Select Device, and then select the target part number in the dialog box.
3. Select the MPLAB hardware tool (Programmer>Select Tool).
4. Perform a "Connect" operation to the device (Programmer>Connect). Depending on the development tool used, the part number and Device Revision ID value appear in the **Output** window.

**Note:** If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The Device ID values for the various devices and silicon revisions are shown in [Table 1](#).

**TABLE 1: SILICON DEVREV VALUES**

Part Number	Device ID <sup>(1)</sup>	Revision ID for Silicon Revision <sup>(2)</sup>		
		A0	A1	B0
PIC18F23K20	20E0h	00h	01h	02h
PIC18F43K20	20C0h	00h	01h	02h

- Note 1:** The device and revision data is stored in the Device ID located at 3FFFFE:3FFFFFh in Configuration and ID memory.
- 2:** Refer to the "PIC18F2XK20/4XK20 Memory Programming Specification" (DS41297) for detailed information.

# PIC18F23/43K20

**TABLE 2: SILICON ISSUE SUMMARY (PIC18F23/43K20)**

Module	Feature	Item Number	Issue Summary	Affected Revisions <sup>(1)</sup>		
				A0	A1	B0
<a href="#">BOR</a>	Reset	<a href="#">1.</a>	Unexpected Reset when using comparator.	X	X	
<a href="#">Comparator</a>	Comparator	<a href="#">2.</a>	Output glitch with FVR selected for ADC.			X
<a href="#">ECCP</a>	Full-Bridge	<a href="#">3.</a>	Dead band time is 4/Fosc instead of 1/Fosc.	X	X	X
<a href="#">ECCP</a>	Full-Bridge	<a href="#">4.</a>	Compromised dead band.	X	X	X
<a href="#">MSSP (SPI clock)</a>	SPI clock	<a href="#">5.</a>	Improper start in Timer2/2 Clock mode.	X	X	X
<a href="#">MSSP (SPI Master mode)</a>	SPI Master	<a href="#">6.</a>	Improper sampling of last bit.	X	X	X
<a href="#">MSSP (SPI Master mode)</a>	SPI Master	<a href="#">7.</a>	Write collision on transmission.	X	X	X
<a href="#">MSSP (Master I2C™ mode)</a>	I <sup>2</sup> C™ Master	<a href="#">8.</a>	Improper handling of Stop event.	X	X	X
<a href="#">EUSART</a>	OERR Flag	<a href="#">9.</a>	Clearing SPEN bit does not clear OERR flag.	X	X	X
<a href="#">EUSART</a>	BAUDCON	<a href="#">10.</a>	RCIDL may improperly stay low.	X	X	X
<a href="#">Data EEPROM Memory</a>	Endurance	<a href="#">11.</a>	Endurance limited to 10K cycles.	X	X	
<a href="#">Program Flash Memory</a>	Endurance	<a href="#">12.</a>	Endurance limited to 1K cycles.	X	X	
<a href="#">ADC</a>	ADC Conversion	<a href="#">13.</a>	ADC conversion may be limited to half scale.	X		

**Note 1:** Only those issues indicated in the last column apply to the current silicon revision.

## Silicon Errata Issues

**Note:** This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**B0**).

### 1. Module: BOR

An unexpected Brown-out Reset may occur when enabling the comparator with the Fixed Voltage Reference (FVR) selected as the VIN+ input.

#### Work around

Disconnect the FVR from the VIN+ comparator inputs prior to enabling the comparator and then reconnect it after enabling the comparator.

#### Affected Silicon Revisions

A0	A1	B0					
X	X						

### 2. Module: Comparator

There may be a glitch on the comparator output when both the comparator and the ADC are using the Fixed Voltage Reference (FVR) as an input and the ADC is enabled, disabled, or starts a conversion.

#### Work around

Do not use the FVR as an input to both the comparator and the ADC at the same time.

#### Affected Silicon Revisions

A0	A1	B0					
		X					

### 3. Module: ECCP

Changing direction in Full-Bridge mode inserts a dead band time of  $4/F_{osc} * (TMR2 \text{ Prescale})$  instead of  $1/F_{osc} * (TMR2 \text{ Prescale})$  as specified in the data sheet.

#### Work around

None.

#### Affected Silicon Revisions

PIC18F23/43K20

A0	A1	B0					
X	X	X					

### 4. Module: ECCP

In Full-Bridge mode when  $PR2 = CCPR1L$  and  $DC1B<1:0> = 00$  and the direction is changed then the dead time before the modulated output starts is compromised. The modulated signal improperly starts immediately with the direction change and stays on for  $Tosc * TMR2Presale * DC1B<1:0>$ .

#### Work around

Avoid changing direction when the duty cycle is within three Least Significant steps of 100% duty cycle. Instead, clear the  $DC1B<1:0>$  bits before the direction change and then set them to the desired value after the direction change is complete.

#### Affected Silicon Revisions

PIC18F23/43K20

A0	A1	B0					
X	X	X					

### 5. Module: MSSP (SPI clock)

When the SPI clock is configured for Timer2/2 ( $SSPCON1<3:0> = 0011$ ), and the CKE bit of the SSPSTAT register is '1', then when SSPBUF is written the SCK output is improperly and immediately driven to the non-Idle state together with the MSb value of the SSPBUF. The duration at which SDO and SCK remain at these levels may be shorter than a full half-bit period. The remaining bits in the byte are output properly.

#### Work around

None.

#### Affected Silicon Revisions

PIC18F23/43K20

A0	A1	B0					
X	X	X					

# PIC18F23/43K20

## 6. Module: MSSP (SPI Master mode)

In SPI Master mode, when the CKE bit of the SSPSTAT register is cleared and the SMP bit of the SSPSTAT register is set, then the last bit of the incoming data stream (bit 0) at the SDI pin will not be sampled properly.

### Work around

none.

### Affected Silicon Revisions

PIC18F23/43K20

A0	A1	B0					
X	X	X					

## 7. Module: MSSP (SPI Master mode)

In SPI Master mode, if the SSPBUF register is written while a byte is actively being transmitted, an extra clock pulse will be improperly generated at the end of the transmission. Further writes to the SSPBUF register will be inhibited although 8 or 9 clock pulses will be generated for each attempted write. The WCON bit of the SSPCON register is properly set indicating that a write collision occurred. However, the write collision condition can only be cleared by resetting the MSSP module. Clear the MSSP by clearing the SSPEN bit of the SSPCON1 register.

### Work around

Use the SSPIF bit of the PIR1 register or the BF bit of the SSPSTAT register to determine that the transmission is complete before writing the SSPBUF register. In the event that a write collision does occur, use the Slave Select feature to resynchronize the Slave clock.

### Affected Silicon Revisions

PIC18F23/43K20

A0	A1	B0					
X	X	X					

## 8. Module: MSSP (Master I<sup>2</sup>C™ mode)

In Master I<sup>2</sup>C Receive mode, if a Stop condition occurs in the middle of an address or data reception, then the SCL clock stream will continue endlessly and the RCEN bit of the SSPCON2 register will remain set improperly. When a Start condition occurs after the improper Stop condition, then 9 additional clocks will be generated followed by the RCEN bit going low.

### Work around

Use low-impedance pull-ups on the SDA line to reduce the possibility of noise glitches, which may trigger an improper Stop event. Use a time-out event timer to detect the unexpected Stop condition and resulting stuck RCEN bit. Clear stuck RCEN bit by clearing SSPEN bit of SSPCON1.

### Affected Silicon Revisions

PIC18F23/43K20

A0	A1	B0					
X	X	X					

## 9. Module: EUSART

The OERR flag of the RCSTA register is reset only by clearing the CREN bit of the RCSTA register or by a device Reset. Clearing the SPEN bit of the RCSTA register does not clear the OERR flag.

### Work around

Clear the OERR flag by clearing the CREN bit instead of clearing the SPEN bit.

### Affected Silicon Revisions

PIC18F23/43K20

A0	A1	B0					
X	X	X					

## 10. Module: EUSART

In Asynchronous Receive mode, the RCIDL bit of the BAUDCON register will properly go low when an invalid Start bit less than 1/16th of a bit time is received. The RCIDL bit will then properly go high 1/8th of a bit time later. However, if another invalid Start bit occurs less than 1 bit time after the leading edge of the first invalid Start bit then the RCIDL bit will improperly stay high then improperly go low one bit time later. The RCIDL bit will then stay low improperly until a valid Start bit is received.

### Work around

When monitoring the RCIDL bit, measure the length of time between the RCIDL going low and the RCIF flag going high. If this time is greater than one character time then restore the RCIDL bit by resetting the EUSART module. The EUSART module is reset when the SPEN bit of the RCSTA register is cleared.

### Affected Silicon Revisions

PIC18F23/43K20

A0	A1	B0					
X	X	X					

## 11. Module: Data EEPROM Memory

The write/erase endurance of Data EE Memory is limited to 10K cycles.

### Work around

Use error correction method that stores data in multiple locations.

### Affected Silicon Revisions

PIC18F23/43K20

A0	A1	B0					
X	X						

## 12. Module: Program Flash Memory

The write/erase endurance of the Program Flash Memory is limited to 1K cycles when VDD is above 3V. Endurance degrades when VDD is below 3V.

### Work around

For data tables in Program Flash Memory use error correction method that stores data in multiple locations.

### Affected Silicon Revisions

PIC18F23/43K20

A0	A1	B0					
X	X						

## 13. Module: ADC

After extended stress the Most Significant bit (MSb) of the ADC conversion result can become stuck at '0'. Conversions resulting in code 511 or less are still accurate, but conversions that should result in codes greater than 511 are instead pinned at 511.

The potential for failures is a function of several factors:

- The potential for failures increases over the life of the part. No failures have ever been seen for accelerated stress estimated to be equivalent to 34 years at room temperature. The failure rate after accelerated stress estimated to be equivalent to 146 years at room temperature can be as high as 10% for VDD = 1.8V. The time to failure will decrease as the operating temperature increases.
- The potential for failures is highest at low VDD and decreases as VDD increases.

### Work around

1. Restrict the input voltage to less than 1/2 of the ADC voltage reference so that the expected result is always a code less than or equal to 511.
2. Use manual acquisition time (ACQT<2:0> = 000) and put the part to Sleep after each conversion.

### Affected Silicon Revisions

PIC18F23/43K20

A0	A1	B0					
X							

# PIC18F23/43K20

---

## Data Sheet Clarifications

The following typographical corrections and clarifications are to be noted for the latest version of the device data sheet (DS41303G):

None.

## APPENDIX A: DOCUMENT REVISION HISTORY

### **Rev. A Document (4/2009)**

First revision of this document.

Data Sheet Clarification: Added Module 1: MSSP I<sup>2</sup>C™ (Table 17-3); Module 2: ADC (Equation 19-1); Module 3: Interrupts.

Added Module 1: ECCP; Module 2: ECCP; Module 3: MSSP; Module 4: MSSP; Module 5: MSSP; Module 6: MSSP; Module 7: EUSART; Module 8: EUSART; Module 9: Data EEPROM Memory; Module 10: Program Flash Memory; Added Module 11: ADC.

### **Rev. B Document (9/2009)**

Added Silicon Revision A1.

Removed Data Sheet Clarification items.

### **Rev. C Document (7/2010)**

Removed ADC Work around #2 and changed #3 to #2 (Module 11).

### **Rev. D Document (7/2011)**

Added Silicon Revision B0; Added Modules BOR and Comparator.

# PIC18F23/43K20

---

NOTES:



---

**Note the following details of the code protection feature on Microchip devices:**

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

---

Information contained in this publication regarding device applications and the like is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION, INCLUDING BUT NOT LIMITED TO ITS CONDITION, QUALITY, PERFORMANCE, MERCHANTABILITY OR FITNESS FOR PURPOSE. Microchip disclaims all liability arising from this information and its use. Use of Microchip devices in life support and/or safety applications is entirely at the buyer's risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights.

#### **Trademarks**

The Microchip name and logo, the Microchip logo, dsPIC, KEELOQ, KEELOQ logo, MPLAB, PIC, PICmicro, PICSTART, PIC<sup>32</sup> logo, rfPIC and UNI/O are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.


FilterLab, Hampshire, HI-TECH C, Linear Active Thermistor, MXDEV, MXLAB, SEEVAL and The Embedded Control Solutions Company are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Analog-for-the-Digital Age, Application Maestro, chipKIT, chipKIT logo, CodeGuard, dsPICDEM, dsPICDEM.net, dsPICworks, dsSPEAK, ECAN, ECONOMONITOR, FanSense, HI-TIDE, In-Circuit Serial Programming, ICSP, Mindi, MiWi, MPASM, MPLAB Certified logo, MPLIB, MPLINK, mTouch, Omniscent Code Generation, PICC, PICC-18, PICDEM, PICDEM.net, PICKit, PICtail, REAL ICE, rfLAB, Select Mode, Total Endurance, TSHARC, UniWinDriver, WiperLock and ZENA are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

SQTP is a service mark of Microchip Technology Incorporated in the U.S.A.

All other trademarks mentioned herein are property of their respective companies.

© 2009-2011, Microchip Technology Incorporated, Printed in the U.S.A., All Rights Reserved.

 Printed on recycled paper.

ISBN: 978-1-61341-379-1

**QUALITY MANAGEMENT SYSTEM**  
**CERTIFIED BY DNV**  
**== ISO/TS 16949:2009 ==**

*Microchip received ISO/TS-16949:2009 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC<sup>®</sup> MCUs and dsPIC<sup>®</sup> DSCs, KEELOQ<sup>®</sup> code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.*

## Worldwide Sales and Service

### AMERICAS

**Corporate Office**  
2355 West Chandler Blvd.  
Chandler, AZ 85224-6199  
Tel: 480-792-7200  
Fax: 480-792-7277  
Technical Support:  
<http://www.microchip.com/support>  
Web Address:  
[www.microchip.com](http://www.microchip.com)

**Atlanta**  
Duluth, GA  
Tel: 678-957-9614  
Fax: 678-957-1455

**Boston**  
Westborough, MA  
Tel: 774-760-0087  
Fax: 774-760-0088

**Chicago**  
Itasca, IL  
Tel: 630-285-0071  
Fax: 630-285-0075

**Cleveland**  
Independence, OH  
Tel: 216-447-0464  
Fax: 216-447-0643

**Dallas**  
Addison, TX  
Tel: 972-818-7423  
Fax: 972-818-2924

**Detroit**  
Farmington Hills, MI  
Tel: 248-538-2250  
Fax: 248-538-2260

**Indianapolis**  
Noblesville, IN  
Tel: 317-773-8323  
Fax: 317-773-5453

**Los Angeles**  
Mission Viejo, CA  
Tel: 949-462-9523  
Fax: 949-462-9608

**Santa Clara**  
Santa Clara, CA  
Tel: 408-961-6444  
Fax: 408-961-6445

**Toronto**  
Mississauga, Ontario,  
Canada  
Tel: 905-673-0699  
Fax: 905-673-6509

### ASIA/PACIFIC

**Asia Pacific Office**  
Suites 3707-14, 37th Floor  
Tower 6, The Gateway  
Harbour City, Kowloon  
Hong Kong  
Tel: 852-2401-1200  
Fax: 852-2401-3431

**Australia - Sydney**  
Tel: 61-2-9868-6733  
Fax: 61-2-9868-6755

**China - Beijing**  
Tel: 86-10-8569-7000  
Fax: 86-10-8528-2104

**China - Chengdu**  
Tel: 86-28-8665-5511  
Fax: 86-28-8665-7889

**China - Chongqing**  
Tel: 86-23-8980-9588  
Fax: 86-23-8980-9500

**China - Hangzhou**  
Tel: 86-571-2819-3180  
Fax: 86-571-2819-3189

**China - Hong Kong SAR**  
Tel: 852-2401-1200  
Fax: 852-2401-3431

**China - Nanjing**  
Tel: 86-25-8473-2460  
Fax: 86-25-8473-2470

**China - Qingdao**  
Tel: 86-532-8502-7355  
Fax: 86-532-8502-7205

**China - Shanghai**  
Tel: 86-21-5407-5533  
Fax: 86-21-5407-5066

**China - Shenyang**  
Tel: 86-24-2334-2829  
Fax: 86-24-2334-2393

**China - Shenzhen**  
Tel: 86-755-8203-2660  
Fax: 86-755-8203-1760

**China - Wuhan**  
Tel: 86-27-5980-5300  
Fax: 86-27-5980-5118

**China - Xian**  
Tel: 86-29-8833-7252  
Fax: 86-29-8833-7256

**China - Xiamen**  
Tel: 86-592-2388138  
Fax: 86-592-2388130

**China - Zhuhai**  
Tel: 86-756-3210040  
Fax: 86-756-3210049

### ASIA/PACIFIC

**India - Bangalore**  
Tel: 91-80-3090-4444  
Fax: 91-80-3090-4123

**India - New Delhi**  
Tel: 91-11-4160-8631  
Fax: 91-11-4160-8632

**India - Pune**  
Tel: 91-20-2566-1512  
Fax: 91-20-2566-1513

**Japan - Yokohama**  
Tel: 81-45-471- 6166  
Fax: 81-45-471-6122

**Korea - Daegu**  
Tel: 82-53-744-4301  
Fax: 82-53-744-4302

**Korea - Seoul**  
Tel: 82-2-554-7200  
Fax: 82-2-558-5932 or  
82-2-558-5934

**Malaysia - Kuala Lumpur**  
Tel: 60-3-6201-9857  
Fax: 60-3-6201-9859

**Malaysia - Penang**  
Tel: 60-4-227-8870  
Fax: 60-4-227-4068

**Philippines - Manila**  
Tel: 63-2-634-9065  
Fax: 63-2-634-9069

**Singapore**  
Tel: 65-6334-8870  
Fax: 65-6334-8850

**Taiwan - Hsin Chu**  
Tel: 886-3-6578-300  
Fax: 886-3-6578-370

**Taiwan - Kaohsiung**  
Tel: 886-7-213-7830  
Fax: 886-7-330-9305

**Taiwan - Taipei**  
Tel: 886-2-2500-6610  
Fax: 886-2-2508-0102

**Thailand - Bangkok**  
Tel: 66-2-694-1351  
Fax: 66-2-694-1350

### EUROPE

**Austria - Wels**  
Tel: 43-7242-2244-39  
Fax: 43-7242-2244-393

**Denmark - Copenhagen**  
Tel: 45-4450-2828  
Fax: 45-4485-2829

**France - Paris**  
Tel: 33-1-69-53-63-20  
Fax: 33-1-69-30-90-79

**Germany - Munich**  
Tel: 49-89-627-144-0  
Fax: 49-89-627-144-44

**Italy - Milan**  
Tel: 39-0331-742611  
Fax: 39-0331-466781

**Netherlands - Drunen**  
Tel: 31-416-690399  
Fax: 31-416-690340

**Spain - Madrid**  
Tel: 34-91-708-08-90  
Fax: 34-91-708-08-91

**UK - Wokingham**  
Tel: 44-118-921-5869  
Fax: 44-118-921-5820