# PIC18F97J60 Family Silicon Errata and Data Sheet Clarification

The PIC18F97J60 family parts you have received conform functionally to the current Device Data Sheet (DS39762**E**), except for the anomalies described below.

**The following silicon errata apply only to PIC18F97J60 family devices with these Device/Revision IDs**:

| Part Number | Device ID | Revision ID |
|---|---|---|
| PIC18F66J60 | 0001 1000 000 | 000xx(1) |
| PIC18F66J65 | 0001 1111 000 | 000xx(1) |
| PIC18F67J60 | 0001 1111 001 | 000xx(1) |
| PIC18F86J60 | 0001 1000 001 | 000xx(1) |
| PIC18F86J65 | 0001 1111 010 | 000xx(1) |
| PIC18F87J60 | 0001 1111 011 | 000xx(1) |
| PIC18F96J60 | 0001 1000 010 | 000xx(1) |
| PIC18F96J65 | 0001 1111 100 | 000xx(1) |
| PIC18F97J60 | 0001 1111 101 | 000xx(1) |

**Note 1:** xx = 00 for A0, 01 for A1/A2 and 11 for A3.

The Device IDs (DEVID1 and DEVID2) are located at addresses, 3FFFFEh:3FFFFFh, in the device's configuration space. They are shown in binary in the format: "DEVID2 DEVID1".

The errata described in this document will be addressed in future revisions of the PIC18F97J60 Family silicon.

Data Sheet Clarifications and corrections start on page 5, following the discussion of silicon issues.

## Silicon Errata Issues

### 1. Module: Resets

$\overline{\text{MCLR}}$ and BOR Resets behave as a POR Reset. Special Function Registers' Reset values after a $\overline{\text{MCLR}}$ or BOR would have the same values as those after a POR. All other Resets behave as described in the data sheet.

**Work around**

None.

**Affected Silicon Revisions**

| A0 | A1 | A2 | A3 | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | X | | | | |

### 2. Module: I/O (PORTJ)

**Note:** This issue is only applicable to the 100-pin device.

When configured to operate in Microcontroller mode (CONFIG3L<EMB1:0> = 11), PORTJ pins do not go to a high-impedance state immediately after a POR Reset. Instead, PORTJ<4,0> are driven low, while all other PORTJ pins are driven high, until the device exits the Reset condition (refer to **Section 4.6.1 "Time-out Sequence"** of the Device Data Sheet for details on when the device exits the Reset condition) before transitioning to a high-impedance state. Note that since MCLR and BOR Resets are also treated as a POR Reset (see Errata Issue #1), PORTJ pins will also be driven as outputs until the device exits these Reset conditions.

**Work around**

If using a PORTJ pin as an input, make sure to check that your circuit will not create a short-circuit condition during a Reset. For example, if you need to have a direct pull-down to ground input, do this on PORTJ<4> or PORTJ<0>, since they are temporary driven low. If using a PORTJ pin as an output, then use a pin that will temporarily drive low for driving active-high loads, and use a pin that temporarily will drive high for driving active-low loads. This way, the temporary output signals are in the Idle state.

**Affected Silicon Revisions**

| A0 | A1 | A2 | A3 | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | X | | | | |

### 3. Module: I/O (PORTJ) and External Memory Bus

**Note:** This issue is only applicable to the 100-pin device.

In an Extended Microcontroller mode (CONFIG3L<EMB1:0> = 00, 01 or 10), each control signal on PORTJ is supposed to be driven to its Idle state. However, the control signals on PORTJ pins go to a high-impedance state for a brief interval after a MCLR Reset. The brief loss of control signals may cause the corruption of data in memory devices connected to the External Memory Bus (EMB).

**Work around**

To maintain the default states on the control lines, use pull-up or pull-down resistors on all PORTJ pins (pull-down on PORTJ<4,0>, pull-up on all others).

**Affected Silicon Revisions**

| A0 | A1 | A2 | A3 | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | X | | | | |

## 4. Module: Ethernet (Buffer Memory)

The receive hardware may corrupt the circular receive buffer (including the Next Packet Pointer and receive status vector fields) when an even value is programmed into the ERXRDPTH:ERXRDPTL registers.

**Work around**

Ensure that only odd addresses are written to the ERXRDPT registers. Assuming that ERXND contains an odd value, many applications can derive a suitable value to write to ERXRDPT by subtracting 1 from the Next Packet Pointer (a value always ensured to be even because of hardware padding) and then compensating for a potential ERXST to ERXND wraparound.

Assuming that the receive buffer area does not span the 1FFFh to 0000h memory boundary, the logic in Example 1 will ensure that ERXRDPT is programmed with an odd value.

**EXAMPLE 1:**

```
if (Next Packet Pointer – 1 < ERXST) or
(Next Packet Pointer – 1 > ERXND)
      then:
ERXRDPT = ERXND
      else:
ERXRDPT = Next Packet Pointer – 1
```

**Affected Silicon Revisions**

| A0 | A1 | A2 | A3 | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | X | | | | |

## 5. Module: Ethernet (MIIM)

When writing to any PHY register through the MIIM interface's MIWRL and MIWRH registers, the low byte actually written to the PHY register may be corrupted. The corruption occurs when the following actions are taken:

- The application writes to MIWRL
- The PIC® MCU core executes any instruction that reads or writes to any memory address that has the Least Significant six address bits of 36h (‘b110110)
- The application writes to MIWRH

For example, the following sequence will result in a corrupted write to a PHY register:

```
MOVFF     0xCF5, MIWRL
NOP
MOVFF     0xCF6, MIWRH
```

In this example, 0xCF5 and 0xCF6 are GPR memory locations that the application wishes to write to the current PHY register defined by the MIREGADR SFR. When the PIC MCU core reads from the GPR at address, 0xCF6 (‘b110011110110), the value originally written to MIWRL will be corrupted.

**Work around 1**

Ensure that following a write to MIWRL, the firmware does not access any of the problem memory locations prior to writing to MIWRH. After finished writing to MIWRH, normal operation can resume.

If interrupts are enabled, disable them prior to writing to MIWRL and MIWRH to prevent an Interrupt Service Routine (ISR) from performing any reads or writes to a problem memory address.

Special care must be taken to ensure that the source data to be written to MIWRH does not result in a problem memory access.

The following PHY write sequence avoids the problem:

1. Copy the low byte to be written to the PHY into the PRODL register.

   PRODL is at address, FF3h, and not subject to the memory address issue.
2. Copy the high byte to be written to the PHY into the PRODH register.

   PRODH is at address, FF4h, and not subject to the memory address issue.
3. Disable all interrupts by clearing GIEH and GIEL in the INTCON register.
4. Move PRODL into MIWRL.
5. Wait one instruction cycle as required by the MAC host interface logic.
6. Move PRODH into MIWRH.
7. Enable all interrupts that are needed by restoring GIEH and GIEL in INTCON.

**Work around 2**

If you cannot disable interrupts, as specified in **Work around 1**, because the application cannot tolerate interrupt latency variations:

- Perform the write (with interrupts enabled), but
- Verify the correct values were written by reading the PHY register

If a corrupted value was written due to an interrupt occurring, perform the write again and reverify. The source data must be stored in a non-problem location.

The application should follow the following procedure:

1. Copy the low byte to be written to the PHY into the PRODL register.

   PRODL is at address, FF3h, and not subject to the memory address issue.

2. Copy the high byte to be written to the PHY into the PRODH register.

   PRODH is at address, FF4h, and not subject to the memory address issue.

3. Move PRODL into MIWRL.
4. Wait one instruction cycle as required by the MAC host interface logic.
5. Move PRODH into MIWRH.
6. Wait two TCY and then poll the BUSY bit (MISTAT<0>) until it is clear.
7. Perform a PHY register read of the same location.
8. Compare the read result with the original value copied to the PRODH:PRODL registers. If they do not match, return to step 1.

**Affected Silicon Revisions**

| A0 | A1 | A2 | A3 | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | X | | | | |

## 6. Module: Ethernet (RX Filter)

When enabled, the Pattern Match receive filter may allow some packets with an incorrect data pattern to be received. Also, in certain configurations, packets with a valid pattern may be incorrectly discarded.

**Work around**

Do not use the Pattern Match hardware filter. Instead, use the Unicast, Mutlicast, Broadcast and Hash Table receive filters to accept all needed packets and filter out unwanted ones in software.

**Affected Silicon Revisions**

| A0 | A1 | A2 | A3 | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | X | | | | |

## 7. Module: Ethernet (TX)

When configured for half duplex and a transmit operation encounters unusual collision timing, there is a small chance that the Ethernet transmit engine will internally deadlock. The PHY will stop transmitting the packet and normal RX operations will continue. However, the TXRTS bit (ECON1<3>) will stay set indefinitely. The TXIF (EIR<3>) and TXERIF (EIR<1>) bits will not become set.

This deadlock condition applies only to half-duplex operation and is most readily observable when the network has a duplex mismatch (i.e., PIC18F97J60 family device is configured for half duplex and the remote node is configured for full duplex). In most cases, high network utilization is needed to observe the issue.

**Work around**

To prevent most transmit deadlock conditions, issue a TX Logic Reset prior to transmitting each packet:

1. Set TXRST (ECON1<7>).
2. Clear TXRST.
3. Wait 1.6 μs or longer.
4. Set TXRTS to start the transmission.

Issuing a TX Logic Reset may cause the Ethernet transmit error interrupt to occur and the associated TXERIF bit to become set, which can be ignored.

To detect and recover from any possible deadlock conditions, applications should implement a timer to poll the TXRTS bit. If the Ethernet hardware enters the deadlock state and fails to clear this bit by the time the timer expires, software should manually clear the TXRTS bit, issue a TX Logic Reset and then set the TXRTS bit to retry transmission. The timer should be cleared and restarted whenever the application sets TXRTS. The timer expiration time should be chosen to allow adequate time for ordinary packets to finish transmitting, after accounting for possible delays, due to the medium being occupied by other nodes. For example, a time-out value of 3 ms is suitable since it will allow a maximum length 1518-byte packet to be transmitted at 10Base-T speeds, while giving reasonable margin to account for potential collisions.

**Affected Silicon Revisions**

| A0 | A1 | A2 | A3 | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | X | | | | |

### 8. Module: Ethernet (DMA)

When the DMA is configured to compute an IP checksum, there is a small chance that an incoming packet receive event will cause the DMA to internally deadlock. In these cases, the DMAST bit (ECON1<5>) stays set indefinitely, and the DMA done interrupt never occurs.

**Work around**

Perform checksum calculations in software. Use the DMA only for copy operations.

**Affected Silicon Revisions**

| A0 | A1 | A2 | A3 | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | X | | | | |

### 9. Module: I/O (PORTJ)

**Note:** This issue is only applicable to the 80-pin device.

The weak internal pull-up resistors on pins, RJ4 and RJ5, cannot be enabled on the PIC18F86J60, PIC18F86J65 and PIC18F87J60 devices. Setting the RJPU bit (PORTA<7>) has no effect on the I/O pin state.

**Work around**

Install external pull-up resistors on RJ4 and RJ5. Alternatively, use any of the PORTB, PORTD or PORTE pins, which all have weak internal pull ups.

**Affected Silicon Revisions**

| A0 | A1 | A2 | A3 | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | X | | | | |

## Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS39762**E**):

| | |
|---|---|
| **Note:** | Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity. |

### 1. Module: Module: Electrical Characteristics

In Table 27-2, on page 430, the maximum Input Offset Voltage (Param No D300) is changed from ±10 mV to ±25 mV. The modified value is indicated in bold text in the following table:

**TABLE 27-2: COMPARATOR SPECIFICATIONS**

| Operating Conditions: 3.0V ≤ $V_{DD}$ ≤ 3.6V, -40°C ≤ $T_A$ ≤ +85°C (unless otherwise stated) | | | | | | | |
|---|---|---|---|---|---|---|---|
| Param No | Sym | Characteristics | Min | Typ | Max | Units | Comments |
| D300 | $V_{IOFF}$ | Input Offset Voltage* | — | ±5.0 | ±**25** | mV | |
| D301 | $V_{ICM}$ | Input Common-Mode Voltage* | 0 | — | $AV_{DD}$ – 1.5 | V | |
| D302 | CMRR | Common-Mode Rejection Ratio* | 55 | — | — | dB | |
| 300 | $T_{RESP}$ | Response Time(1)* | — | 150 | 400 | ns | |
| 301 | $T_{MC2OV}$ | Comparator Mode Change to Output Valid* | — | — | 10 | µs | |

* These parameters are characterized but not tested.

Note 1: Response time measured with one comparator input at ($AV_{DD}$ – 1.5)/2, while the other input transitions from $V_{SS}$ to $AV_{DD}$.

## REVISION HISTORY

Rev A Document (2/2009)

Original version of this document. Includes silicon issues 1 (Resets), 2 (I/O – PORTJ), 3 (I/O (PORTJ) and External Memory Bus), 4 (Ethernet – Buffer Memory), 5 (Ethernet – MIIM), 6 (Ethernet – RX Filter), 7 (Ethernet – TX), 8 (Ethernet – DMA) and 9 (I/O – PORTJ).

Rev B Document (3/2010)

Changed the title to A1/A2 as this document now also covers the A2 silicon. Updated the data sheet reference revision from “D” to “E”.

Rev C Document (10/2010)

Merged silicon errata documents for Revision A0 and Revision A1/A2. Updated all affected silicon errata for each module to include Revision A3. Merged data sheet errata to create a single errata document for this part.

**NOTES:**

**Note the following details of the code protection feature on Microchip devices:**

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