DS90C031B LVDS Quad CMOS Differential Line Driver

Check for Samples: DS90C031B

FEATURES

- **>155.5 Mbps (77.7 MHz) switching rates**
- **High impedance LVDS outputs with power-off**
- **±350 mV differential signaling**
- **Ultra low power dissipation**
- **400 ps maximum differential skew (5V, 25°C)**
- **3.5 ns maximum propagation delay**
- **Industrial operating temperature range**
- **Pin compatible with DS26C31, MB571 (PECL) and 41LG (PECL)**
- **Conforms to ANSI/TIA/EIA-644 LVDS standard**
- **Offered in narrow body SOIC package**
- **Fail-safe logic for floating inputs**

DESCRIPTION

The DS90C031B is a quad CMOS differential line driver designed for applications requiring ultra low power dissipation and high data rates. The device supports data rates in excess of 155.5 Mbps (77.7 MHz) and uses Low Voltage Differential Signaling (LVDS) technology.

The DS90C031B accepts TTL/CMOS input levels and translates them to low voltage (350 mV) differential output signals. In addition the driver supports a TRI-STATE function that may be used to disable the output stage, disabling the load current, and thus dropping the device to an ultra low idle power state of 11 mW typical.

In addition, the DS90C031B provides power-off high impedance LVDS outputs. This feature assures minimal loading effect on the LVDS bus lines when V_{CC} is not present.

The DS90C031B and companion line receiver (DS90C032B) provide a new alternative to high power pseudo-ECL devices for high speed point-to-point interface applications.

Connection Diagram

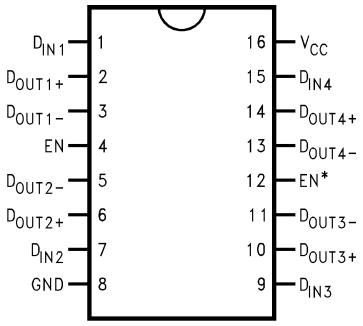
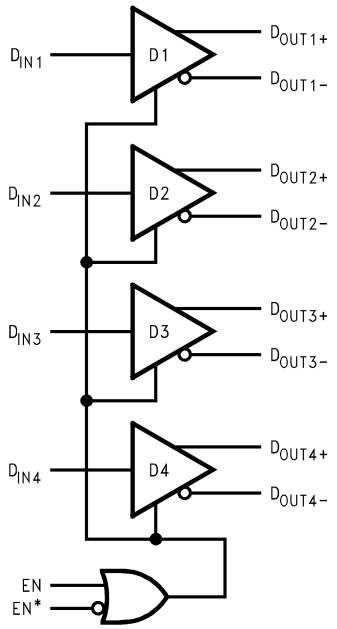


Figure 1. Dual-In-Line
See Package Number D (R-PDSO-G16)

Functional Diagram



Driver Truth Table

Enables		Input	Outputs	
EN	EN*	D_{IN}	D_{OUT+}	D_{OUT-}
L	H	X	Z	Z
All other combinations of ENABLE inputs		L	L	H
		H	H	L

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)

Supply Voltage (V_{CC})	−0.3V to +6V
Input Voltage (D_{IN})	−0.3V to (V_{CC} + 0.3V)
Enable Input Voltage (EN, EN*)	−0.3V to (V_{CC} + 0.3V)
Output Voltage (D_{OUT+}, D_{OUT-})	−0.3V to +5.8V
Short Circuit Duration (D_{OUT+}, D_{OUT-})	Continuous
Maximum Package Power Dissipation at +25°C	1068 mW
Derate Power Dissipation	8.5 mW/°C above +25°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature Range, Soldering (4 seconds)	+260°C
Maximum Junction Temperature	+150°C
ESD Rating	
HBM, 1.5 kΩ, 100 pF	≥ 2kV
EIAJ, 0 Ω, 200 pF	≥ 250V

(1) "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" specifies conditions of device operation.

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage (V_{CC})	+4.5	+5.0	+5.5	V
Operating Free Air Temperature (T_A)	−40	+25	+85	°C

Electrical Characteristics

Over supply voltage and operating temperature ranges, unless otherwise specified. (1) (2)

Symbol	Parameter	Test Conditions	Pin	Min	Typ	Max	Units
V_{OD1}	Differential Output Voltage	R_L = 100Ω (Figure 2)	D_{OUT-}, D_{OUT+}	250	345	450	mV
ΔV_{OD1}	Change in Magnitude of V_{OD1} for Complementary Output States				4	35	|mV|
V_{OS}	Offset Voltage			1.10	1.25	1.35	V
ΔV_{OS}	Change in Magnitude of V_{OS} for Complementary Output States				5	25	|mV|
V_{OH}	Output Voltage High	R_L = 100Ω			1.41	1.60	V
V_{OL}	Output Voltage Low			0.90	1.07		V
V_{IH}	Input Voltage High		D_{IN}, EN, EN*	2.0		V_{CC}	V
V_{IL}	Input Voltage Low			GND		0.8	V
I_I	Input Current	V_{IN} = V_{CC}, GND, 2.5V or 0.4V		−10	±1	+10	µA
V_{CL}	Input Clamp Voltage	I_{CL} = −18 mA		−1.5	−0.8		V
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V (3)	D_{OUT-}, D_{OUT+}		−3.5	−5.0	mA
I_{OZ}	Output TRI-STATE Current	EN = 0.8V and EN* = 2.0V, V_{OUT} = 0V or V_{CC}		−10	±1	+10	µA
I_{OFF}	Power - Off Leakage	V_O = 0V or 2.4V, V_{CC} = 0V or Open		−10	±1	+10	µA
I_{CC}	No Load Supply Current Drivers Enabled	D_{IN} = V_{CC} or GND	V_{CC}		1.7	3.0	mA
		D_{IN} = 2.5V or 0.4V			4.0	6.5	mA
I_{CCL}	Loaded Supply Current Drivers Enabled	R_L = 100Ω (all channels), V_{IN} = V_{CC} or GND (all inputs)			15.4	21.0	mA
I_{CCZ}	No Load Supply Current Drivers Disabled	D_{IN} = V_{CC} or GND, EN = GND, EN* = V_{CC}			2.2	4.0	mA

(1) Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground except: V_{OD1} and ΔV_{OD1}.
(2) All typicals are given for: V_{CC} = +5.0V, T_A = +25°C.
(3) Output short circuit current (I_{OS}) is specified as magnitude only, minus sign indicates direction only.

Switching Characteristics

V_{CC} = +5.0V, T_A = +25°C (1) (2) (3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHLD}	Differential Propagation Delay High to Low	R_L = 100Ω, C_L = 5 pF (Figure 3 and Figure 4)	1.0	2.0	3.0	ns
t_{PLHD}	Differential Propagation Delay Low to High		1.0	2.1	3.0	ns
t_{SKD}	Differential Skew $\|t_{PHLD} - t_{PLHD}\|$		0	80	400	ps
t_{SK1}	Channel-to-Channel Skew (4)		0	300	600	ps
t_{TLH}	Rise Time			0.35	1.5	ns
t_{THL}	Fall Time			0.35	1.5	ns
t_{PHZ}	Disable Time High to Z	R_L = 100Ω, C_L = 5 pF (Figure 5 and Figure 6)		2.5	10	ns
t_{PLZ}	Disable Time Low to Z			2.5	10	ns
t_{PZH}	Enable Time Z to High			2.5	10	ns
t_{PZL}	Enable Time Z to Low			2.5	10	ns

(1) All typicals are given for: V_{CC} = +5.0V, T_A = +25°C.
(2) Generator waveform for all tests unless otherwise specified: f = 1 MHz, Z_O = 50Ω, t_r ≤ 6 ns, and t_f ≤ 6 ns.
(3) C_L includes probe and jig capacitance.
(4) Channel-to-Channel Skew is defined as the difference between the propagation delay of the channel and the other channels in the same chip with an event on the inputs.

Switching Characteristics

V_{CC} = +5.0V ± 10%, T_A = −40°C to +85°C (1) (2) (3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHLD}	Differential Propagation Delay High to Low	R_L = 100Ω, C_L = 5 pF (Figure 3 and Figure 4)	0.5	2.0	3.5	ns
t_{PLHD}	Differential Propagation Delay Low to High		0.5	2.1	3.5	ns
t_{SKD}	Differential Skew $\|t_{PHLD} - t_{PLHD}\|$		0	80	900	ps
t_{SK1}	Channel-to-Channel Skew (4)		0	0.3	1.0	ns
t_{SK2}	Chip to Chip Skew (5)				3.0	ns
t_{TLH}	Rise Time			0.35	2.0	ns
t_{THL}	Fall Time			0.35	2.0	ns
t_{PHZ}	Disable Time High to Z	R_L = 100Ω, C_L = 5 pF (Figure 5 and Figure 6)		2.5	15	ns
t_{PLZ}	Disable Time Low to Z			2.5	15	ns
t_{PZH}	Enable Time Z to High			2.5	15	ns
t_{PZL}	Enable Time Z to Low			2.5	15	ns

(1) All typicals are given for: V_{CC} = +5.0V, T_A = +25°C.
(2) Generator waveform for all tests unless otherwise specified: f = 1 MHz, Z_O = 50Ω, t_r ≤ 6 ns, and t_f ≤ 6 ns.
(3) C_L includes probe and jig capacitance.
(4) Channel-to-Channel Skew is defined as the difference between the propagation delay of the channel and the other channels in the same chip with an event on the inputs.
(5) Chip to Chip Skew is defined as the difference between the minimum and maximum specified differential propagation delays.

PARAMETER MEASUREMENT INFORMATION

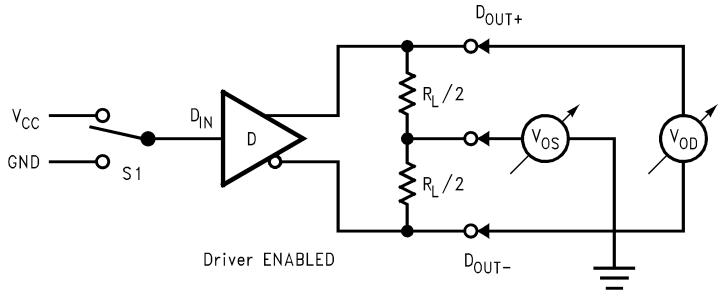


Figure 2. Driver V_{OD} and V_{OS} Test Circuit

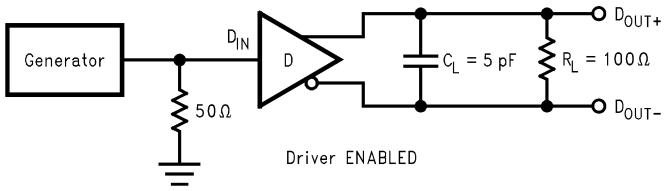


Figure 3. Driver Propagation Delay and Transition Time Test Circuit

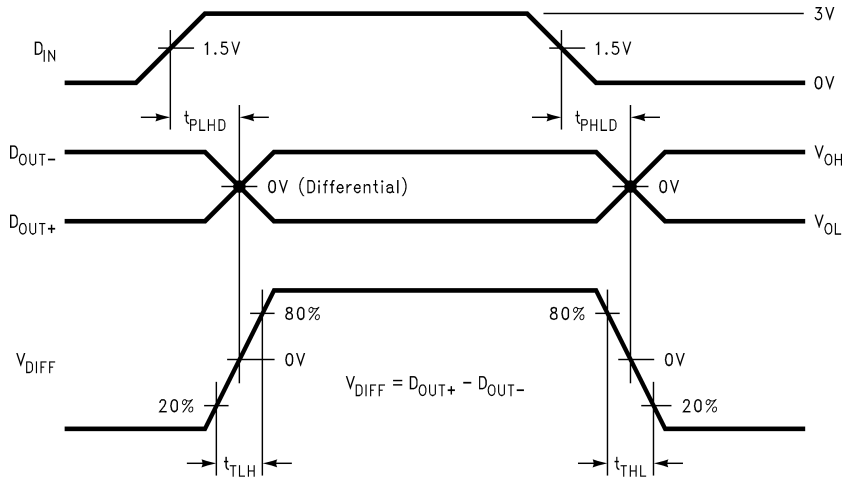


Figure 4. Driver Propagation Delay and Transition Time Waveforms

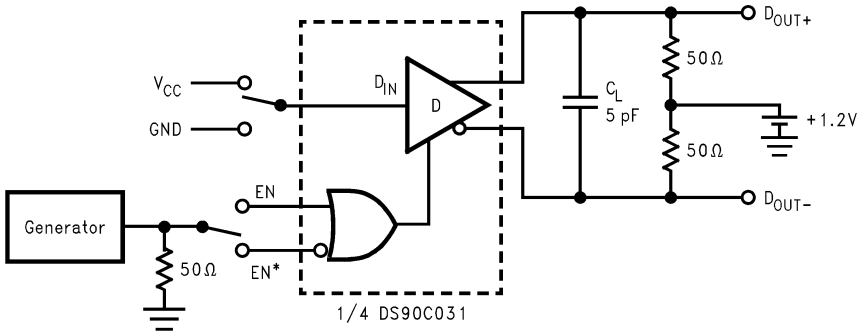


Figure 5. Driver TRI-STATE Delay Test Circuit

PARAMETER MEASUREMENT INFORMATION (continued)

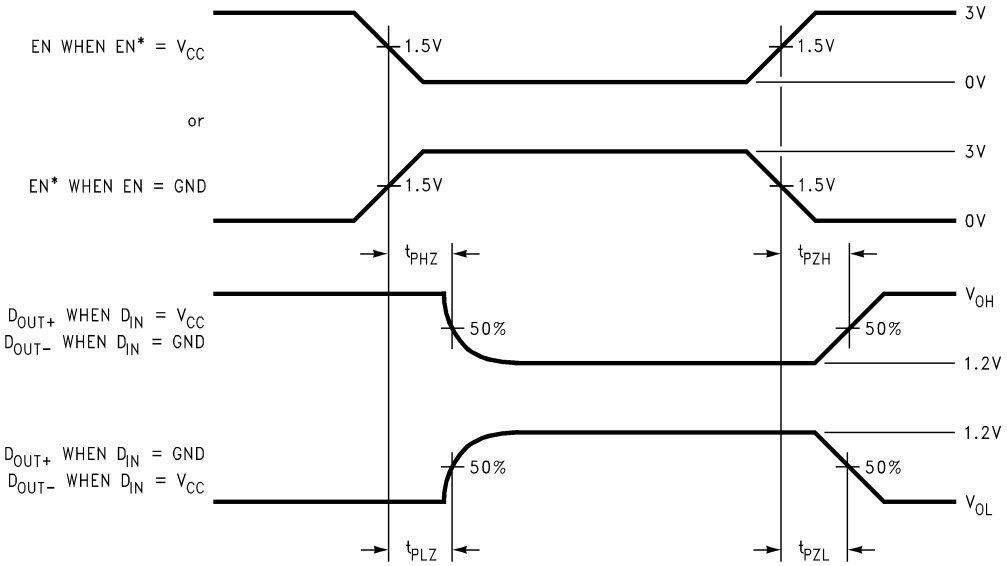


Figure 6. Driver TRI-STATE Delay Waveform

Typical Application

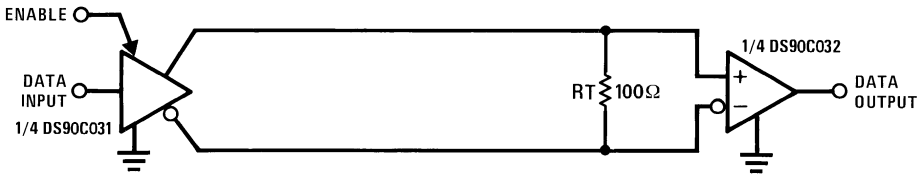


Figure 7. Point-to-Point Application

APPLICATIONS INFORMATION

LVDS drivers and receivers are intended to be primarily used in an uncomplicated point-to-point configuration as is shown in Figure 7. This configuration provides a clean signaling environment for the quick edge rates of the drivers. The receiver is connected to the driver through a balanced media which may be a standard twisted pair cable, a parallel pair cable, or simply PCB traces. Typically, the characteristic impedance of the media is in the range of 100Ω. A termination resistor of 100Ω should be selected to match the media, and is located as close to the receiver input pins as possible. The termination resistor converts the current sourced by the driver into a voltage that is detected by the receiver. Other configurations are possible such as a multi-receiver configuration, but the effects of a mid-stream connector(s), cable stub(s), and other impedance discontinuities as well as ground shifting, noise margin limits, and total termination loading must be taken into account.

The DS90C031B differential line driver is a balanced current source design. A current mode driver, generally speaking has a high output impedance and supplies a constant current for a range of loads (a voltage mode driver on the other hand supplies a constant voltage for a range of loads). Current is switched through the load in one direction to produce a logic state and in the other direction to produce the other logic state. The typical output current is a mere 3.4 mA with a minimum of 2.5 mA, and a maximum of 4.5 mA. The current mode **requires** (as discussed above) that a resistive termination be employed to terminate the signal and to complete the loop as shown in Figure 7. AC or unterminated configurations are not allowed. The 3.4 mA loop current will develop a differential voltage of 340 mV across the 100Ω termination resistor which the receiver detects with a 240 mV minimum differential noise margin neglecting resistive line losses (driven signal minus receiver threshold (340 mV – 100 mV = 240 mV). The signal is centered around +1.2V (Driver Offset, V_{OS}) with respect to ground as shown in Figure 8. Note that the steady-state voltage (V_{SS}) peak-to-peak swing is twice the differential voltage (V_{OD}) and is typically 680 mV.

The current mode driver provides substantial benefits over voltage mode drivers, such as an RS-422 driver. Its quiescent current remains relatively flat versus switching frequency. Whereas the RS-422 voltage mode driver increases exponentially in most case between 20 MHz–50 MHz. This is due to the overlap current that flows between the rails of the device when the internal gates switch. Whereas the current mode driver switches a fixed current between its output without any substantial overlap current. This is similar to some ECL and PECL devices, but without the heavy static I_{CC} requirements of the ECL/PECL designs. LVDS requires > 80% less current than similar PECL devices. AC specifications for the driver are a tenfold improvement over other existing RS-422 drivers.

The fail-safe circuitry guarantees that the outputs are enabled and at a logic "0" (the true output is low and the complement output is high) when the inputs are floating.

The TRI-STATE function allows the driver outputs to be disabled, thus obtaining an even lower power state when the transmission of data is not required.

The footprint of the DS90C031B is the same as the industry standard 26LS31 Quad Differential (RS-422) Driver.

The DS90C031B is electrically similar to the DS90C031, but differs by supporting high impedance LVDS outputs under power-off condition. This allows for multiple or redundant drivers to be used in certain applications. The DS90C031B is offered in a space saving narrow SOIC (150 mil.) package.

For additional LVDS application information, see TI's LVDS Owner's Manual available through TI's website http://www.ti.com/lsds/ti/analog/interface.page.

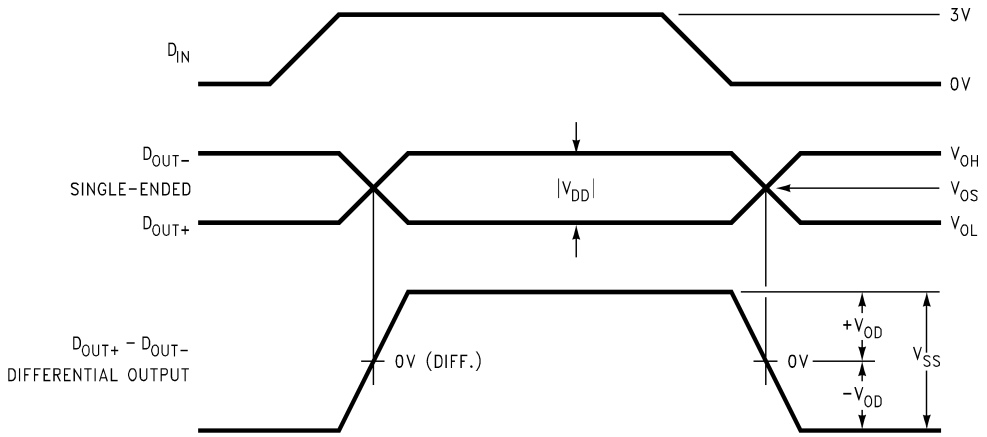


Figure 8. Driver Output Levels

Pin Descriptions

Pin No.	Name	Description
1, 7, 9, 15	D_{IN}	Driver input pin, TTL/CMOS compatible
2, 6, 10, 14	D_{OUT+}	Non-inverting driver output pin, LVDS levels
3, 5, 11, 13	D_{OUT-}	Inverting driver output pin, LVDS levels
4	EN	Active high enable pin, OR-ed with EN*
12	EN*	Active low enable pin, OR-ed with EN
16	V_{CC}	Power supply pin, +5V ± 10%
8	GND	Ground pin

TYPICAL PERFORMANCE CHARACTERISTICS

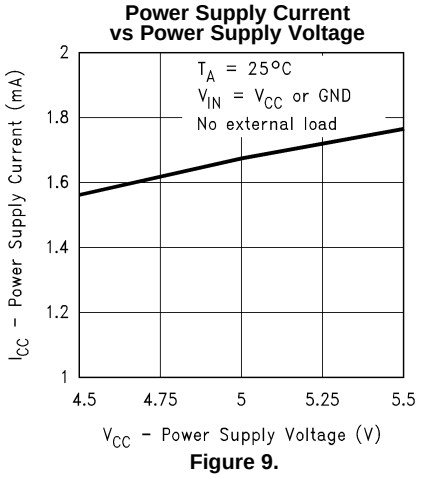


Figure 9.

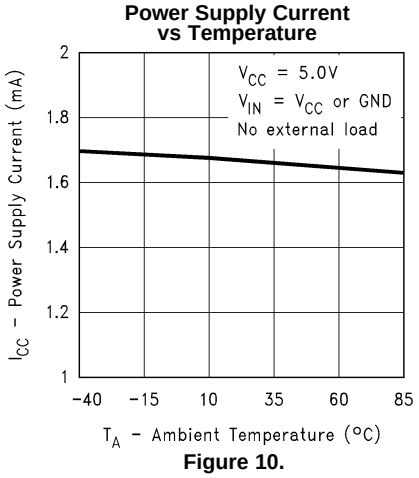


Figure 10.

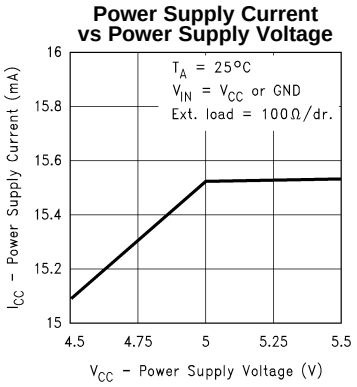


Figure 11.

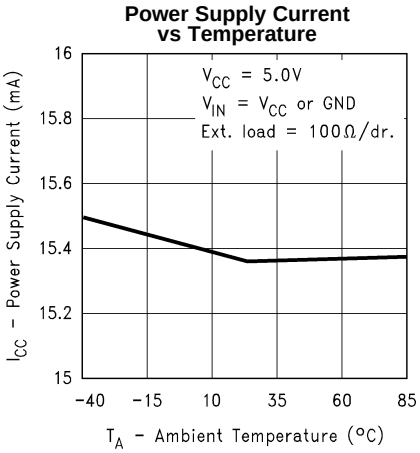


Figure 12.

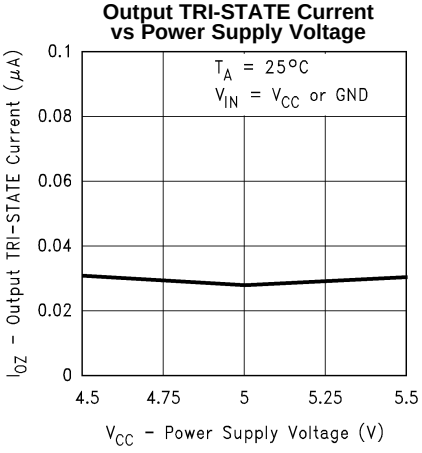


Figure 13.

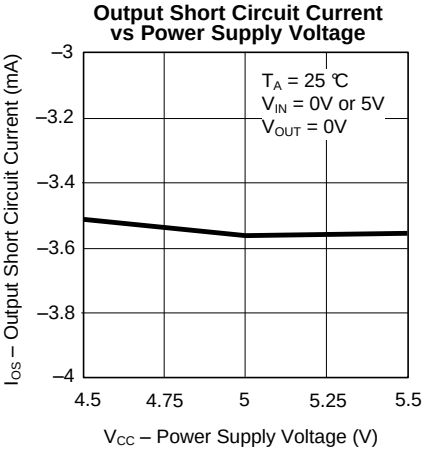


Figure 14.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Differential Output Voltage vs Power Supply Voltage

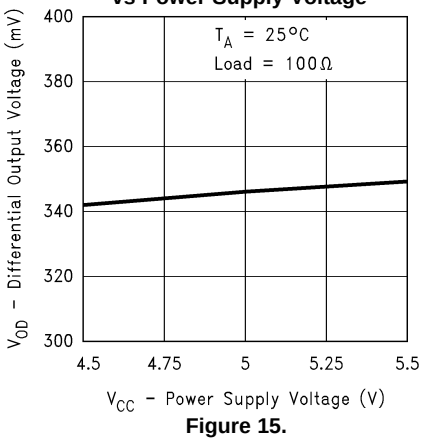


Figure 15.

Differential Output Voltage vs Ambient Temperature

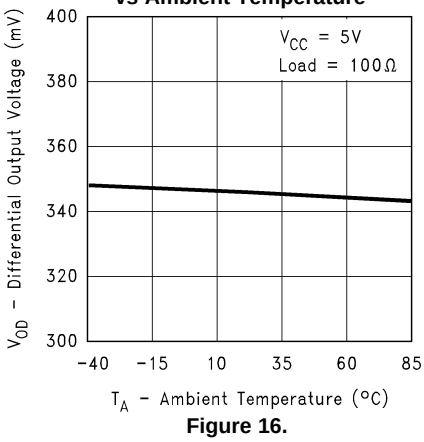


Figure 16.

Output Voltage High vs Power Supply Voltage

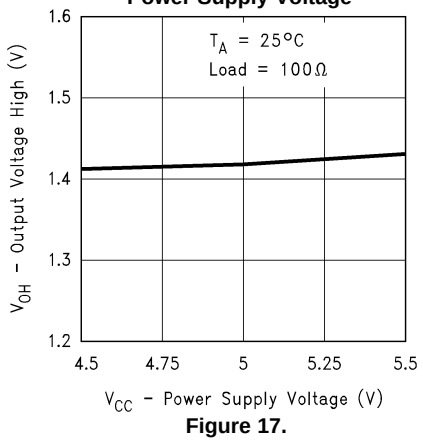


Figure 17.

Output Voltage High vs Ambient Temperature

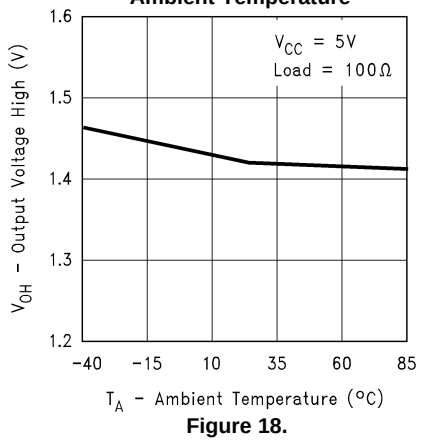


Figure 18.

Output Voltage Low vs Power Supply Voltage

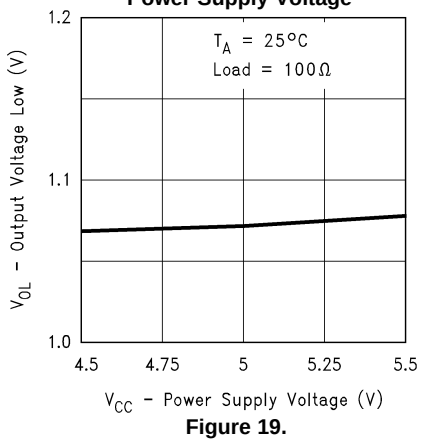


Figure 19.

Output Voltage Low vs Ambient Temperature

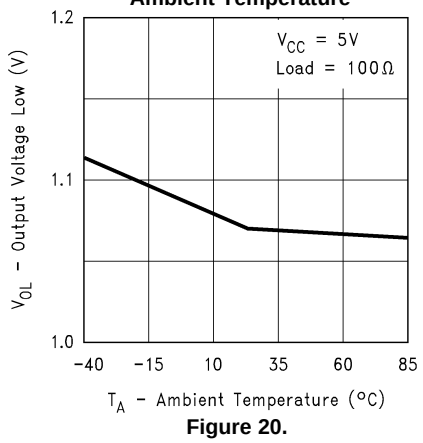


Figure 20.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Offset Voltage vs Power Supply Voltage

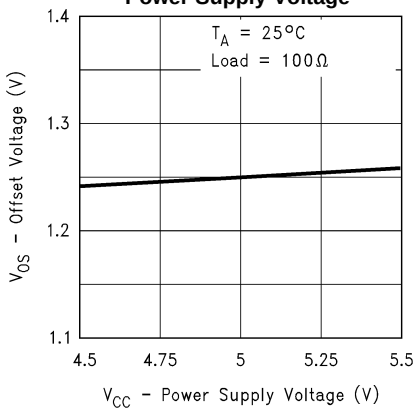


Figure 21.

Offset Voltage vs Ambient Temperature

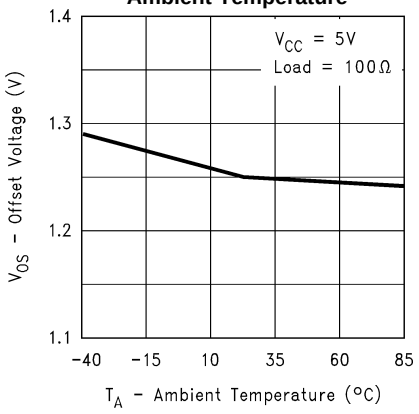


Figure 22.

Power Supply Current vs Frequency

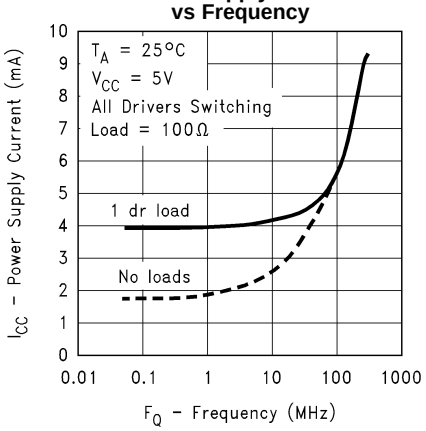


Figure 23.

Power Supply Current vs Frequency

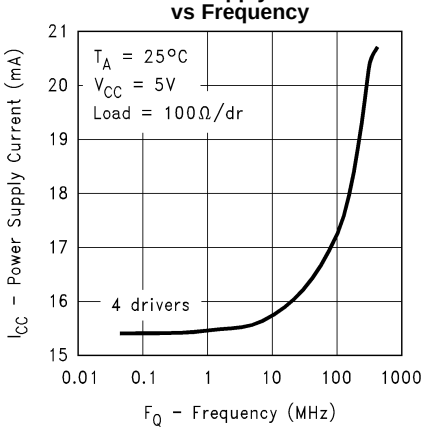


Figure 24.

Differential Output Voltage vs Load Resistor

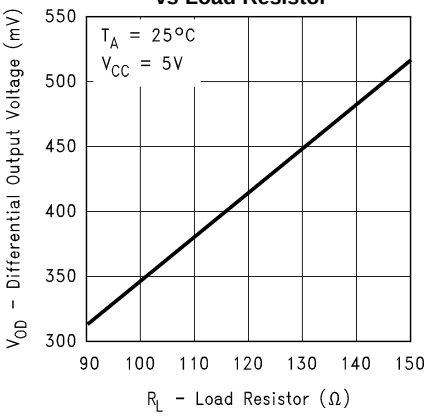


Figure 25.

Differential Propagation Delay vs Power Supply Voltage

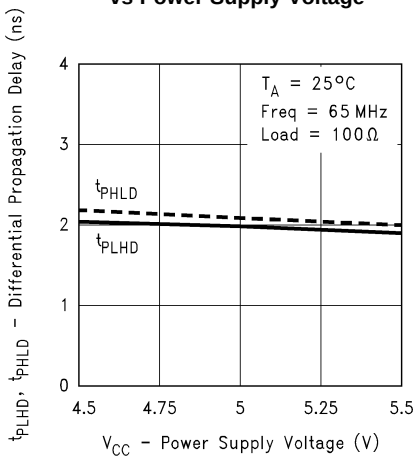


Figure 26.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Differential Propagation Delay vs Ambient Temperature

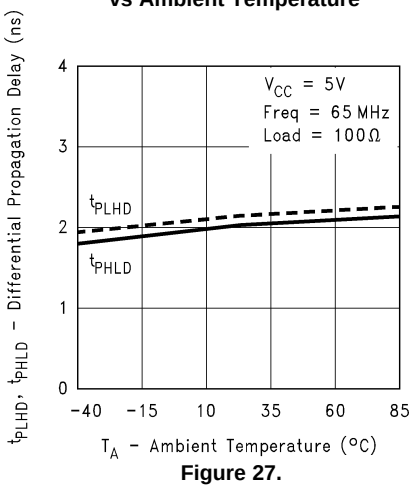


Figure 27.

Differential Skew vs Power Supply Voltage

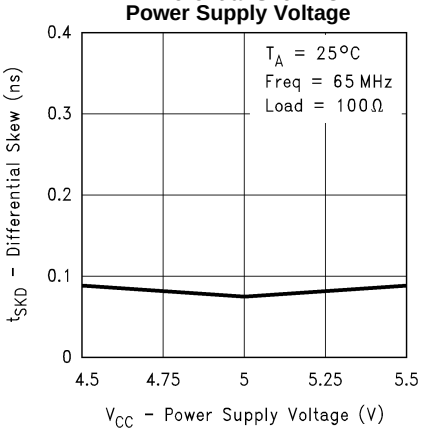


Figure 28.

Differential Skew vs Ambient Temperature

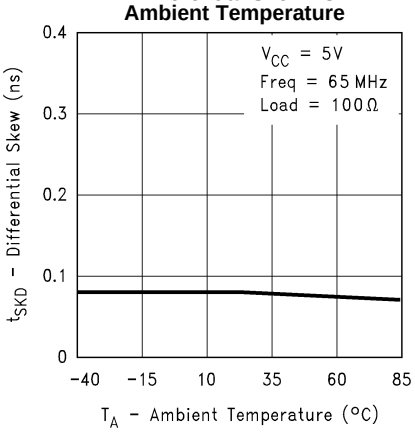


Figure 29.

Differential Transition Time vs Power Supply Voltage

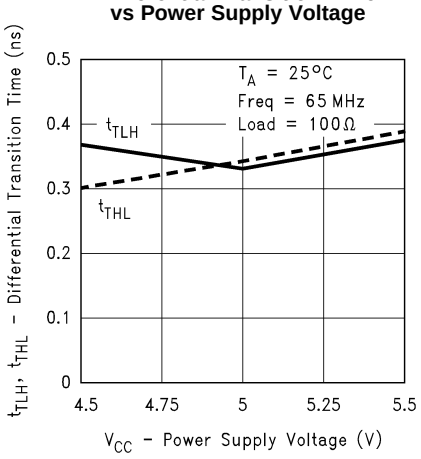


Figure 30.

Differential Transition Time vs Ambient Temperature

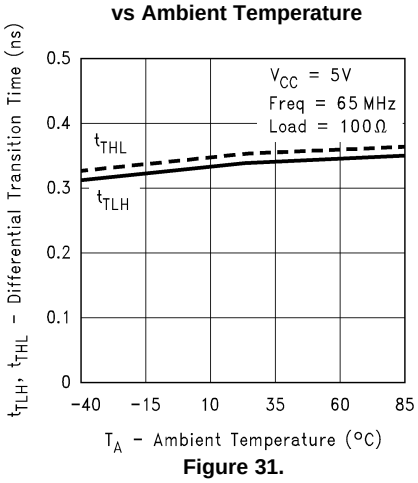


Figure 31.

REVISION HISTORY

Changes from Revision A (March 2013) to Revision B	Page
• Changed layout of National Data Sheet to TI format	12

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS90C031BTM	NRND	SOIC	D	16	48	TBD	Call TI	Call TI	-40 to 85	DS90C031BTM	
DS90C031BTM/NOPB	ACTIVE	SOIC	D	16	48	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	DS90C031BTM	Samples
DS90C031BTMX/NOPB	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	DS90C031BTM	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

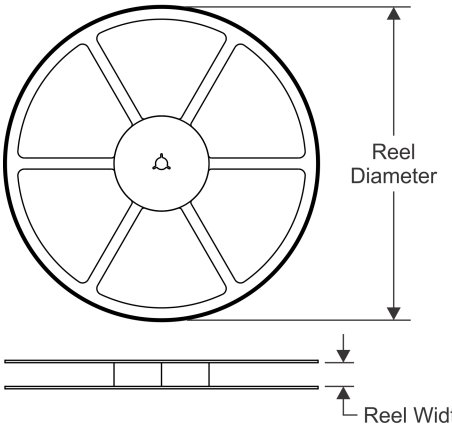
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

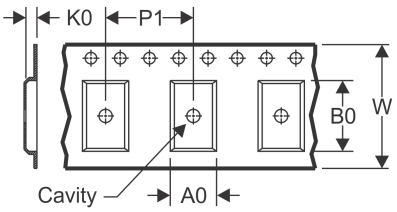
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

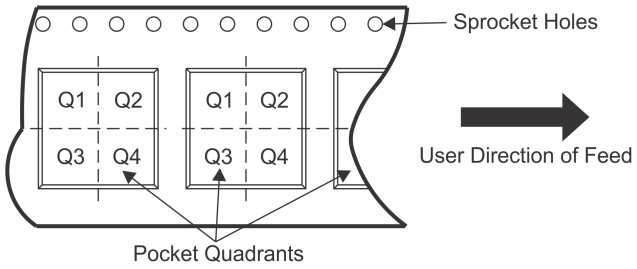


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

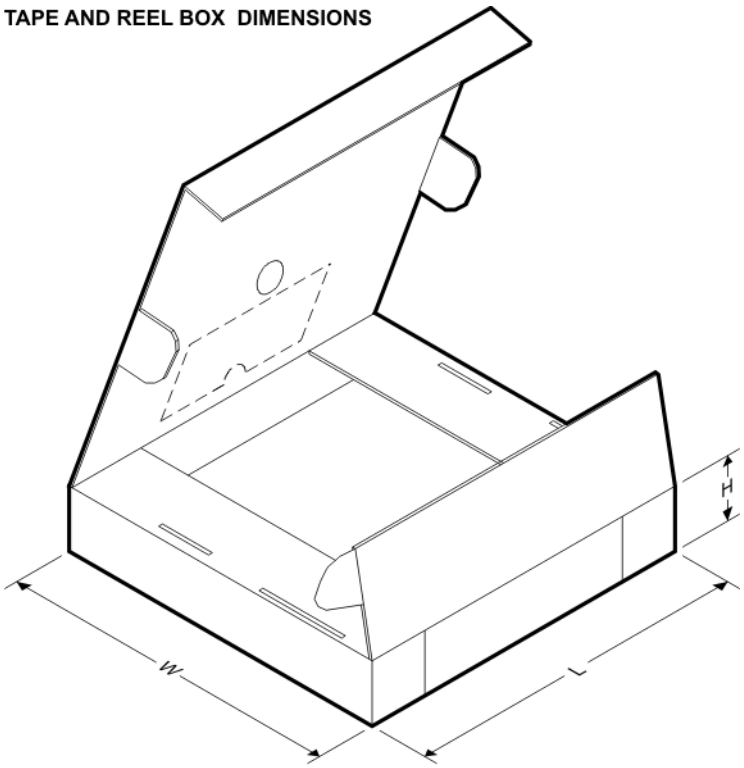
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS90C031BTMX/NOPB	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.3	8.0	16.0	Q1

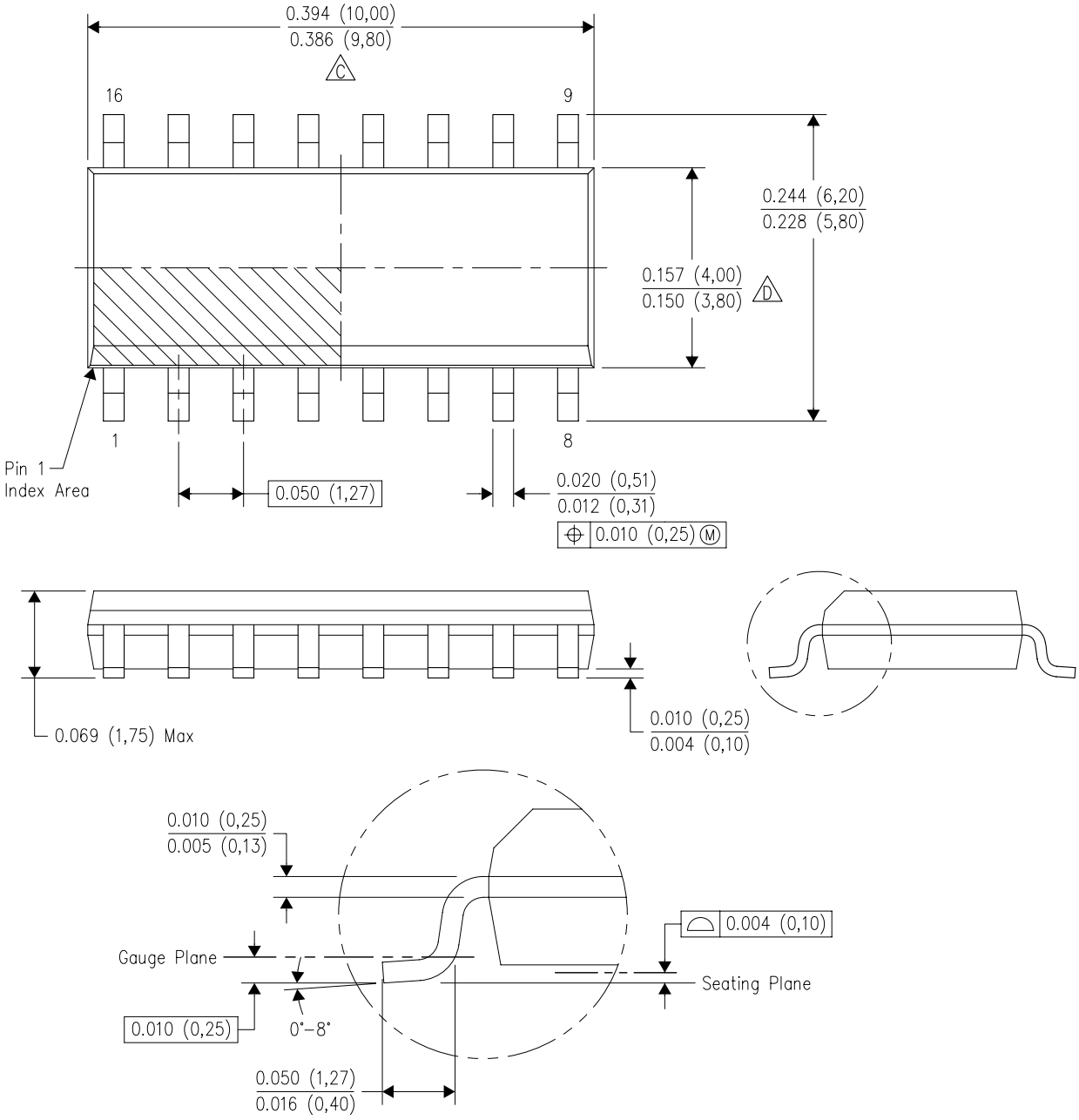
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS90C031BTMX/NOPB	SOIC	D	16	2500	367.0	367.0	35.0

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

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