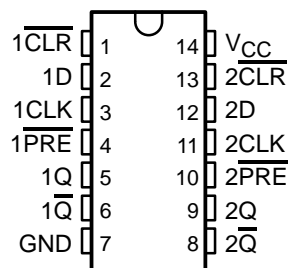


# CD54AC74, CD74AC74 DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH CLEAR AND PRESET

SCHS231D – SEPTEMBER 1998 – REVISED DECEMBER 2002

- AC Types Feature 1.5-V to 5.5-V Operation and Balanced Noise Immunity at 30% of the Supply
- Speed of Bipolar F, AS, and S, With Significantly Reduced Power Consumption
- Balanced Propagation Delays
- $\pm 24$ -mA Output Drive Current  
– Fanout to 15 F Devices
- SCR-Latchup-Resistant CMOS Process and Circuit Design
- Exceeds 2-kV ESD Protection Per MIL-STD-883, Method 3015

CD54AC74 ... F PACKAGE  
CD74AC74 ... E OR M PACKAGE  
(TOP VIEW)



## description/ordering information

The 'AC74 dual positive-edge-triggered devices are D-type flip-flops.

A low level at the preset ( $\overline{PRE}$ ) or clear ( $\overline{CLR}$ ) inputs sets or resets the outputs, regardless of the levels of the other inputs. When  $\overline{PRE}$  and  $\overline{CLR}$  are inactive (high), data at the data (D) input meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not related directly to the rise time of the clock pulse. Following the hold-time interval, data at the D input can be changed without affecting the levels at the outputs.

## ORDERING INFORMATION

T <sub>A</sub>	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–55°C to 125°C	PDIP – E	Tube	CD74AC74E	CD74AC74E
	SOIC – M	Tube	CD74AC74M	AC74M
		Tape and reel	CD74AC74M96	
	CDIP – F	Tube	CD54AC74F3A	CD54AC74F3A

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

## FUNCTION TABLE (each flip-flop)

INPUTS				OUTPUTS	
PRE	CLR	CLK	D	Q	Q̄
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H‡	H‡
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q <sub>0</sub>	Q̄ <sub>0</sub>

‡ This configuration is nonstable; that is, it does not persist when PRE or CLR returns to its inactive (high) level.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS  
INSTRUMENTS**

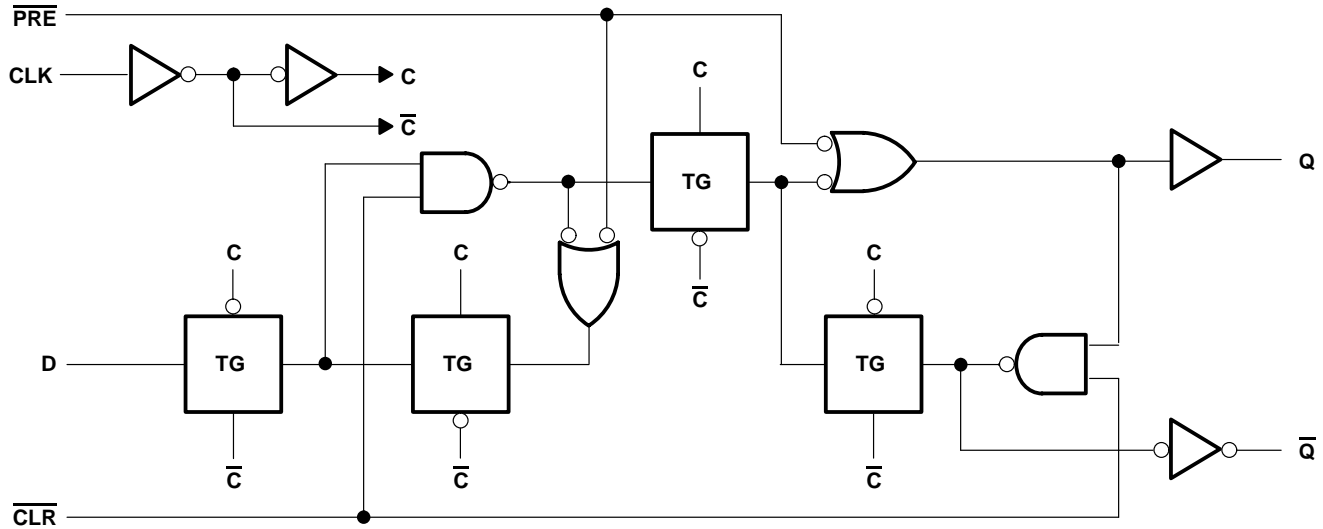
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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

# CD54AC74, CD74AC74 DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH CLEAR AND PRESET

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## logic diagram, each flip-flop (positive logic)



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ .....	-0.5 V to 6 V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ ) (see Note 1) .....	$\pm 20$ mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ ) (see Note 1) .....	$\pm 50$ mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ ) .....	$\pm 50$ mA
Continuous current through $V_{CC}$ or GND .....	$\pm 100$ mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): E package .....	80°C/W
M package .....	86°C/W
Storage temperature range, $T_{stg}$ .....	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The package thermal impedance is calculated in accordance with JESD 51-7.

# CD54AC74, CD74AC74 DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH CLEAR AND PRESET

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## recommended operating conditions (see Note 3)

		T <sub>A</sub> = 25°C		–55°C to 125°C		–40°C to 85°C		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
V <sub>CC</sub>	Supply voltage	1.5	5.5	1.5	5.5	1.5	5.5	V
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 1.5 V	1.2	1.2	1.2	1.2		V
		V <sub>CC</sub> = 3 V	2.1	2.1	2.1			
		V <sub>CC</sub> = 5.5 V	3.85	3.85	3.85			
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 1.5 V		0.3	0.3	0.3		V
		V <sub>CC</sub> = 3 V		0.9	0.9	0.9		
		V <sub>CC</sub> = 5.5 V		1.65	1.65	1.65		
V <sub>I</sub>	Input voltage	0	V <sub>CC</sub>	0	V <sub>CC</sub>	0	V <sub>CC</sub>	V
V <sub>O</sub>	Output voltage	0	V <sub>CC</sub>	0	V <sub>CC</sub>	0	V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 4.5 V to 5.5 V		–24	–24	–24		mA
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 4.5 V to 5.5 V		24	24	24		mA
Δt/Δv	Input transition rise or fall rate	V <sub>CC</sub> = 1.5 V to 3 V		50	50	50		ns/V
		V <sub>CC</sub> = 3.6 V to 5.5 V		20	20	20		

NOTE 3: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C		–55°C to 125°C		–40°C to 85°C		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V <sub>OH</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = –50 μA	1.5 V	1.4	1.4	1.4		V	
			3 V	2.9	2.9	2.9			
			4.5 V	4.4	4.4	4.4			
		I <sub>OH</sub> = –4 mA	3 V	2.58	2.4	2.48			
		I <sub>OH</sub> = –24 mA	4.5 V	3.94	3.7	3.8			
		I <sub>OH</sub> = –50 mA <sup>†</sup>	5.5 V		3.85				
V <sub>OL</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 50 μA	1.5 V		0.1	0.1	0.1	V	
			3 V		0.1	0.1	0.1		
			4.5 V		0.1	0.1	0.1		
		I <sub>OL</sub> = 12 mA	3 V		0.36	0.5	0.44		
		I <sub>OL</sub> = 24 mA	4.5 V		0.36	0.5	0.44		
		I <sub>OL</sub> = 50 mA <sup>†</sup>	5.5 V			1.65			
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5 V		±0.1	±1	±1	μA		
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V		4	80	40	μA		
C <sub>i</sub>				10	10	10	pF		

<sup>†</sup> Test one output at a time, not exceeding 1-second duration. Measurement is made by forcing indicated current and measuring voltage to minimize power dissipation. Test verifies a minimum 50-Ω transmission-line drive capability at 85°C and 75-Ω transmission-line drive capability at 125°C.



**CD54AC74, CD74AC74**  
**DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOPS**  
**WITH CLEAR AND PRESET**

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**timing requirements over recommended operating free-air temperature range,  $V_{CC} = 1.5\text{ V}$  (unless otherwise noted)**

		-55°C to 125°C		-40°C to 85°C		UNIT
		MIN	MAX	MIN	MAX	
$f_{\text{clock}}$	Clock frequency	9		10		MHz
$t_w$	Pulse duration	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ low		50	44	ns
		CLK		56	49	
$t_{\text{su}}$	Setup time	Data		44	39	ns
		$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ inactive				ns
$t_h$	Hold time	Data after CLK $\uparrow$		0	0	ns
$t_{\text{rec}}$	Recovery time, before CLK $\uparrow$	CLR $\uparrow$ or PRE $\uparrow$		34	30	ns

**timing requirements over recommended operating free-air temperature range,  $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$  (unless otherwise noted) (see Figure 1)**

		-55°C to 125°C		-40°C to 85°C		UNIT
		MIN	MAX	MIN	MAX	
$f_{\text{clock}}$	Clock frequency	79		90		MHz
$t_w$	Pulse duration	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ low		5.6	4.9	ns
		CLK		6.3	5.5	
$t_{\text{su}}$	Setup time	Data		4.9	4.3	ns
		$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ inactive				ns
$t_h$	Hold time	Data after CLK $\uparrow$		0	0	ns
$t_{\text{rec}}$	Recovery time, before CLK $\uparrow$	CLR $\uparrow$ or PRE $\uparrow$		4.7	4.1	ns

**timing requirements over recommended operating free-air temperature range,  $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted) (see Figure 1)**

		-55°C to 125°C		-40°C to 85°C		UNIT
		MIN	MAX	MIN	MAX	
$f_{\text{clock}}$	Clock frequency	110		125		MHz
$t_w$	Pulse duration	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ low		4	3.5	ns
		CLK		4.5	3.9	
$t_{\text{su}}$	Setup time	Data		3.5	3.1	ns
		$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ inactive				ns
$t_h$	Hold time	Data after CLK $\uparrow$		0	0	ns
$t_{\text{rec}}$	Recovery time, before CLK $\uparrow$	CLR $\uparrow$ or PRE $\uparrow$		2.7	2.4	ns



**CD54AC74, CD74AC74**  
**DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOPS**  
**WITH CLEAR AND PRESET**

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switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 1.5\text{ V}$ ,  $C_L = 50\text{ pF}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	–55°C to 125°C		–40°C to 85°C		UNIT
			MIN	MAX	MIN	MAX	
$f_{max}$			9		10		MHz
$t_{PLH}$	CLK	Q or $\bar{Q}$		125		114	ns
$t_{PHL}$				125		114	
$t_{PLH}$	$\overline{PRE}$ or $\overline{CLR}$	Q or $\bar{Q}$		132		120	ns
$t_{PHL}$				144		131	

switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	–55°C to 125°C		–40°C to 85°C		UNIT
			MIN	MAX	MIN	MAX	
$f_{max}$			79		90		MHz
$t_{PLH}$	CLK	Q or $\bar{Q}$	3.5	14	3.6	12.7	ns
$t_{PHL}$			3.5	14	3.6	12.7	
$t_{PLH}$	$\overline{PRE}$ or $\overline{CLR}$	Q or $\bar{Q}$	3.7	14.7	3.8	13.4	ns
$t_{PHL}$			4	16.1	4.1	14.6	

switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	–55°C to 125°C		–40°C to 85°C		UNIT
			MIN	MAX	MIN	MAX	
$f_{max}$			110		125		MHz
$t_{PLH}$	CLK	Q or $\bar{Q}$	2.5	10	2.6	9.1	ns
$t_{PHL}$			2.5	10	2.6	9.1	
$t_{PLH}$	$\overline{PRE}$ or $\overline{CLR}$	Q or $\bar{Q}$	2.6	10.5	2.7	9.5	ns
$t_{PHL}$			2.9	11.5	3	10.4	

operating characteristics,  $T_A = 25^\circ\text{C}$

PARAMETER		TYP	UNIT
$C_{pd}$	Power dissipation capacitance	55	pF

# CD54AC74, CD74AC74 DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH CLEAR AND PRESET

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## PARAMETER MEASUREMENT INFORMATION



† When  $V_{CC} = 1.5\text{ V}$ ,  $R1 = R2 = 1\text{ k}\Omega$

LOAD CIRCUIT

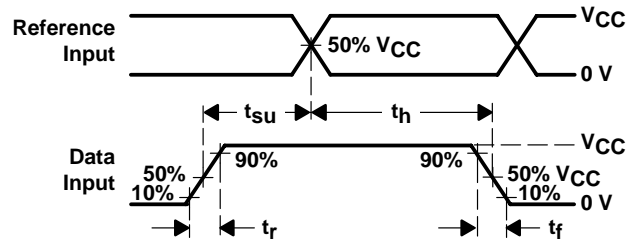
TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$2 \times V_{CC}$
$t_{PHZ}/t_{PZH}$	GND



VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
RECOVERY TIME



VOLTAGE WAVEFORMS  
SETUP AND HOLD AND INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES



VOLTAGE WAVEFORMS  
OUTPUT ENABLE AND DISABLE TIMES

- NOTES:
- A.  $C_L$  includes probe and test-fixture capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r = 3\text{ ns}$ ,  $t_f = 3\text{ ns}$ . Phase relationships between waveforms are arbitrary.
  - D. For clock inputs,  $f_{max}$  is measured with the input duty cycle at 50%.
  - E. The outputs are measured one at a time with one input transition per measurement.
  - F.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
  - G.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - H.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
CD54AC74F3A	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type
CD74AC74E	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD74AC74EE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD74AC74M	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74AC74M96	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74AC74M96E4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74AC74M96G4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74AC74ME4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74AC74MG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

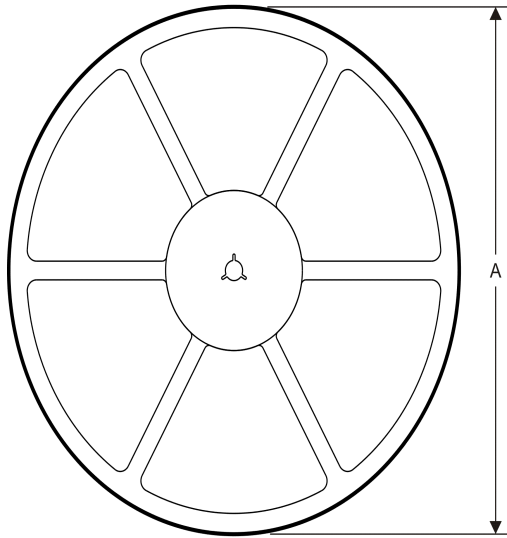
<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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**TAPE AND REEL INFORMATION**

**REEL DIMENSIONS**



**TAPE DIMENSIONS**



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**TAPE AND REEL INFORMATION**

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74AC74M96	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1



**TAPE AND REEL BOX DIMENSIONS**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74AC74M96	SOIC	D	14	2500	367.0	367.0	38.0

J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package is hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  -  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4211283-3/E 08/12

- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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