

ADS7824

www.burr-brown.com/databook/ADS7824.html

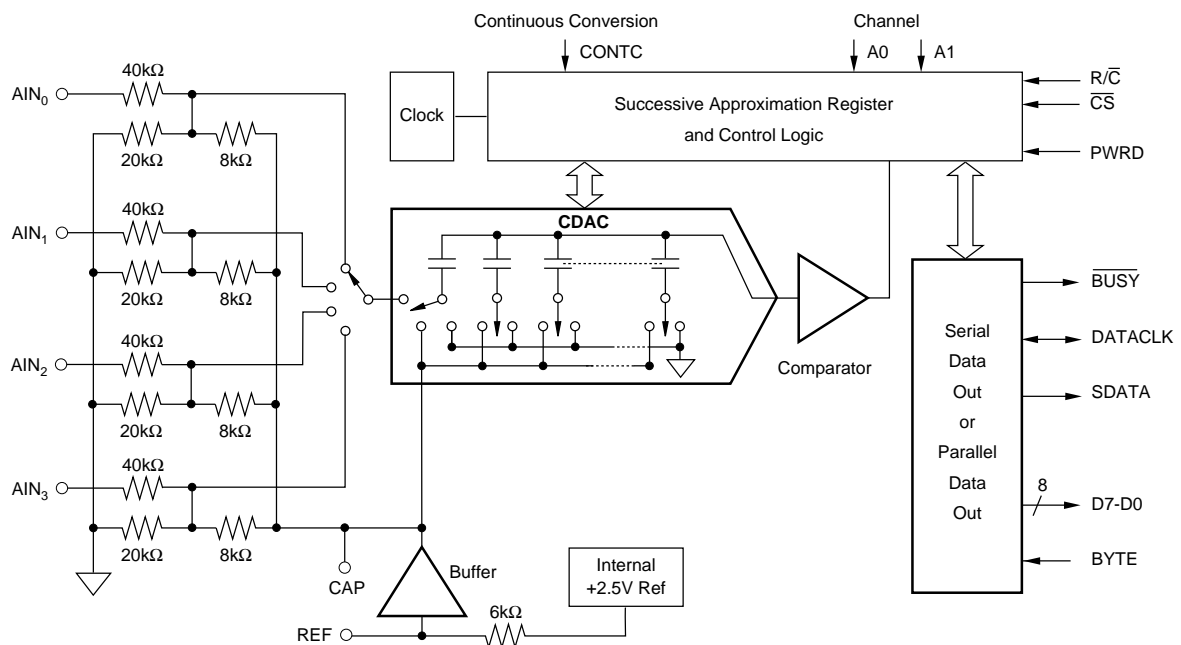
4 Channel, 12-Bit Sampling CMOS A/D Converter

FEATURES

- 25 μ s max SAMPLING AND CONVERSION
- SINGLE +5V SUPPLY OPERATION
- PIN-COMPATIBLE WITH 16-BIT ADS7825
- PARALLEL AND SERIAL DATA OUTPUT
- 28-PIN 0.3" PLASTIC DIP AND SOIC
- ± 0.5 LSB max INL AND DNL
- 50mW max POWER DISSIPATION
- 50 μ W POWER DOWN MODE
- ± 10 V INPUT RANGE, FOUR CHANNEL MULTIPLEXER
- CONTINUOUS CONVERSION MODE

DESCRIPTION

The ADS7824 can acquire and convert 12 bits to within ± 0.5 LSB in 25 μ s max while consuming only 50mW max. Laser-trimmed scaling resistors provide the standard industrial ± 10 V input range and channel-to-channel matching of $\pm 0.1\%$. The ADS7824 is a low-power 12-bit sampling A/D with a four channel input multiplexer, S/H, clock, reference, and a parallel/serial microprocessor interface. It can be configured in a continuous conversion mode to sequentially digitize all four channels. The 28-pin ADS7824 is available in a plastic 0.3" DIP and in a SOIC, both fully specified for operation over the industrial -40°C to $+85^{\circ}\text{C}$ range.



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 Internet: <http://www.burr-brown.com/> • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

At $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $f_S = 40\text{kHz}$, $V_{S1} = V_{S2} = V_S = +5\text{V} \pm 5\%$, using external reference, $\text{CONTC} = 0\text{V}$, unless otherwise specified.

PARAMETER	CONDITIONS	ADS7824P, U			ADS7824PB, UB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
RESOLUTION				12			*(1)	Bits
ANALOG INPUT Voltage Range Impedance Capacitance	Channel On or Off		$\pm 10\text{V}$ 45.7 35			*	*	V k Ω pF
THROUGHPUT SPEED Conversion Time Acquisition Time Multiplexer Settling Time Complete Cycle (Acquire and Convert) Complete Cycle (Acquire and Convert) Throughput Rate	Includes Acquisition CONTC = +5V		20 5 5	25 40	*	*	*	μs μs μs μs μs kHz
DC ACCURACY Integral Linearity Error Differential Linearity Error No Missing Codes Transition Noise ⁽³⁾ Full Scale Error ⁽⁴⁾ Full Scale Error Drift Full Scale Error ⁽⁴⁾ Full Scale Error Drift Bipolar Zero Error Bipolar Zero Error Drift Channel-to-Channel Mismatch Power Supply Sensitivity	Internal Reference Internal Reference +4.75 < V_S < +5.25		± 0.15 ± 0.15 Guaranteed 0.1	± 1 ± 1 ± 0.5 ± 7 ± 0.5 ± 10 ± 2 ± 0.1 ± 0.5		*	± 0.5 ± 0.5 ± 0.25 ± 5 ± 0.25 ± 0.1 *	LSB ⁽²⁾ LSB LSB % ppm/ $^\circ\text{C}$ % ppm/ $^\circ\text{C}$ mV ppm/ $^\circ\text{C}$ % LSB
AC ACCURACY Spurious-Free Dynamic Range ⁽⁵⁾ Total Harmonic Distortion Signal-to-(Noise+Distortion) Signal-to-Noise Channel Separation ⁽⁶⁾ -3dB Bandwidth Useable Bandwidth ⁽⁷⁾	$f_{IN} = 1\text{kHz}$ $f_{IN} = 1\text{kHz}$ $f_{IN} = 1\text{kHz}$ $f_{IN} = 1\text{kHz}$ $f_{IN} = 1\text{kHz}$	80 70 70 90	90 -90 73 73 100	-80	*	*	*	dB dB dB dB dB MHz kHz
SAMPLING DYNAMICS Aperture Delay Transient Response ⁽⁸⁾ Overvoltage Recovery ⁽⁹⁾	FS Step		40 5 1			*	*	ns μs μs
REFERENCE Internal Reference Voltage Internal Reference Source Current (Must use external buffer) External Reference Voltage Range for Specified Linearity External Reference Current Drain	 $V_{REF} = +2.5\text{V}$	2.48 2.3	2.5 1 2.5	2.52 2.7 100	*	*	*	V μA V μA
DIGITAL INPUTS Logic Levels V_{IL} V_{IH} I_{IL} I_{IH}		-0.3 +2.4		+0.8 $V_S + 0.3\text{V}$ ± 10 ± 10	*	*	*	V V μA μA
DIGITAL OUTPUTS Data Format Data Coding V_{OL} V_{OH} Leakage Current Output Capacitance	 $I_{SINK} = 1.6\text{mA}$ $I_{SOURCE} = 500\mu\text{A}$ High-Z State, $V_{OUT} = 0\text{V}$ to V_S High-Z State			+0.4 ± 5 15	*	*	*	V V μA pF

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SPECIFICATIONS (CONT)

ELECTRICAL

At $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $f_s = 40\text{kHz}$, $V_{S1} = V_{S2} = V_S = +5\text{V} \pm 5\%$, using external reference, $\text{CONTC} = 0\text{V}$, unless otherwise specified.

PARAMETER	CONDITIONS	ADS7824P, U			ADS7824PB, UB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
DIGITAL TIMING								
Bus Access Time	PAR/SER = +5V			83			*	ns
Bus Relinquish Time	PAR/SER = +5V			83			*	ns
Data Clock	PAR/SER = 0V							
Internal Clock (Output only when transmitting data)	EXT/INT LOW	0.5		1.5	*		*	MHz
External Clock	EXT/INT HIGH	0.1		10	*		*	MHz
POWER SUPPLIES								
$V_{S1} = V_{S2} = V_S$		+4.75	+5	+5.25	*	*	*	V
Power Dissipation	$f_s = 40\text{kHz}$ PWRD HIGH		50	50		*	*	mW μW
TEMPERATURE RANGE								
Specified Performance		-40		+85	*		*	$^{\circ}\text{C}$
Storage		-65		+150	*		*	$^{\circ}\text{C}$
Thermal Resistance (θ_{JA})								
Plastic DIP			75			*		$^{\circ}\text{C}/\text{W}$
SOIC			75			*		$^{\circ}\text{C}/\text{W}$

NOTES: (1) An asterisk (*) specifies same value as grade to the left. (2) LSB means Least Significant Bit. For the 12-bit, $\pm 10\text{V}$ input ADS7824, one LSB is 4.88mV. (3) Typical rms noise at worst case transitions and temperatures. (4) Full scale error is the worst case of -Full Scale or +Full Scale untrimmed deviation from ideal first and last code transitions, divided by the transition voltage (not divided by the full-scale range) and includes the effect of offset error. (5) All specifications in dB are referred to a full-scale $\pm 10\text{V}$ input. (6) A full scale sinewave input on one channel will be attenuated by this amount on the other channels. (7) Useable Bandwidth defined as Full-Scale input frequency at which Signal-to-(Noise+Distortion) degrades to 60dB, or 10 bits of accuracy. (8) The ADS7824 will accurately acquire any input step if given a full acquisition period after the step. (9) Recovers to specified performance after 2 x FS input overvoltage, and normal acquisitions can begin.

PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER ⁽¹⁾	TEMPERATURE RANGE	MAXIMUM INTEGRAL LINEARITY ERROR (LSB)	MINIMUM SIGNAL-TO-(NOISE + DISTORTION) RATIO (dB)
ADS7824P	Plastic Dip	246	-40°C to $+85^{\circ}\text{C}$	± 1	70
ADS7824PB	Plastic Dip	246	-40°C to $+85^{\circ}\text{C}$	± 0.5	72
ADS7824U	SOIC	217	-40°C to $+85^{\circ}\text{C}$	± 1	70
ADS7824UB	SOIC	217	-40°C to $+85^{\circ}\text{C}$	± 0.5	72

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ABSOLUTE MAXIMUM RATINGS

Analog Inputs: $\text{AIN}_0, \text{AIN}_1, \text{AIN}_2, \text{AIN}_3$	$\pm 15\text{V}$
REF	(AGND2 -0.3V) to ($V_S + 0.3\text{V}$)
CAP	Indefinite Short to AGND2, Momentary Short to V_S
V_{S1} and V_{S2} to AGND2	$\pm 7\text{V}$
V_{S1} to V_{S2}	$\pm 0.3\text{V}$
Difference between AGND1, AGND2 and DGND	$\pm 0.3\text{V}$
Digital Inputs and Outputs	-0.3V to ($V_S + 0.3\text{V}$)
Maximum Junction Temperature	150°C
Internal Power Dissipation	825mW
Lead Temperature (soldering, 10s)	$+300^{\circ}\text{C}$
Maximum Input Current to Any Pin	100mA

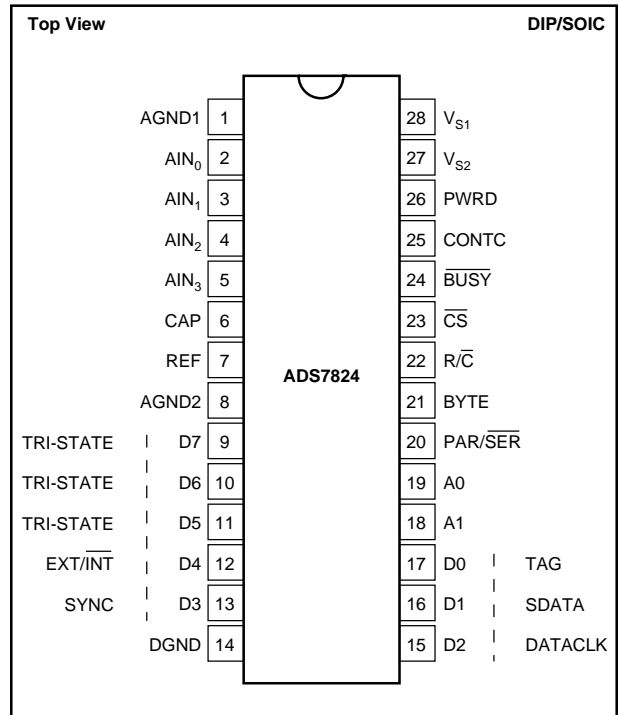


ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PIN CONFIGURATION

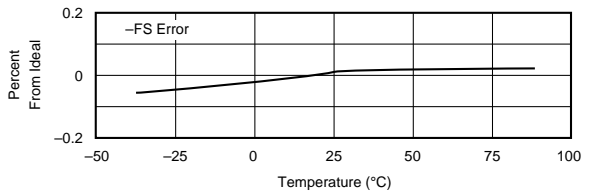
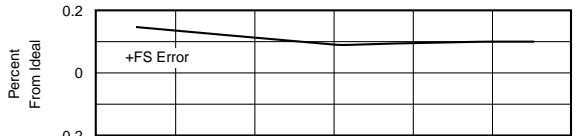
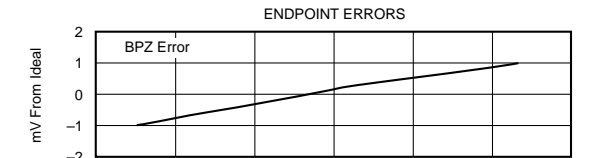
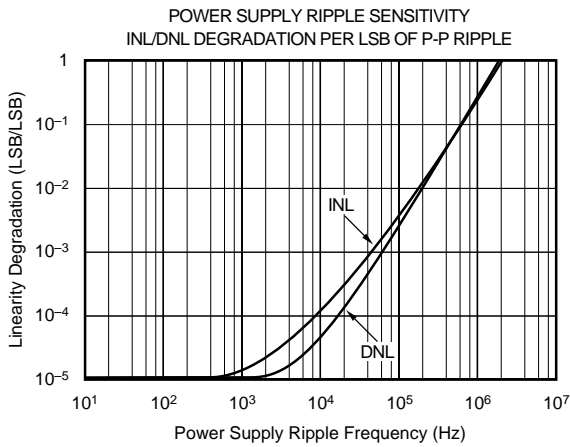
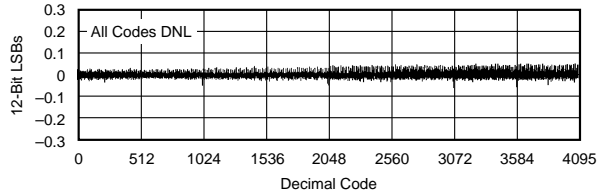
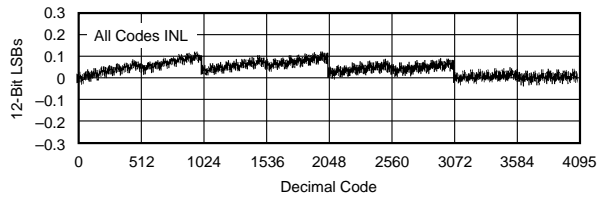
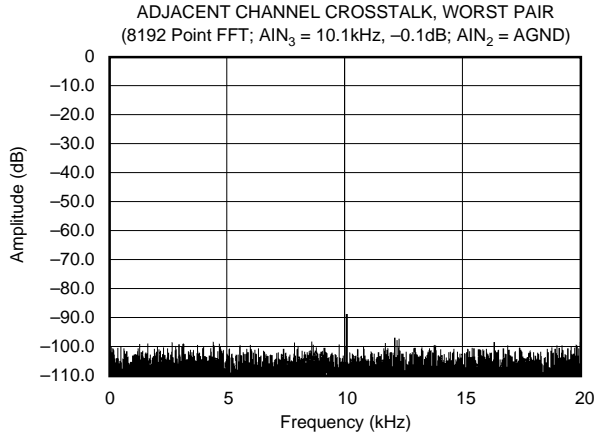
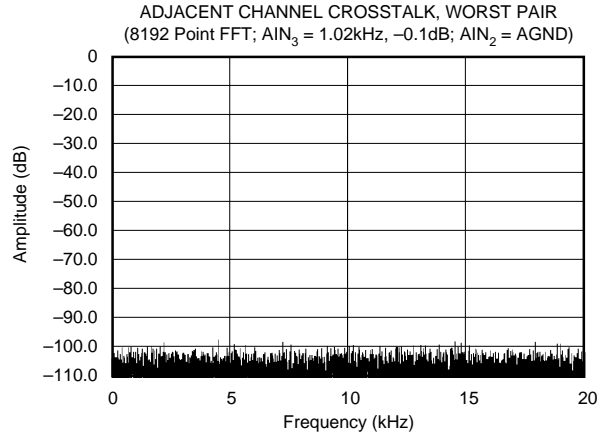
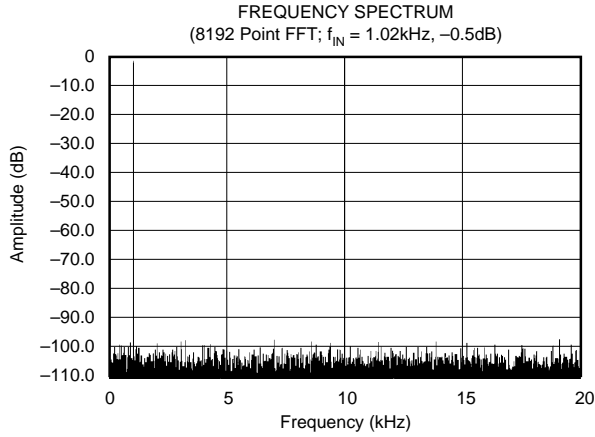


PIN ASSIGNMENTS

PIN #	NAME	I/O	DESCRIPTION
1	AGND1		Analog Ground. Used internally as ground reference point.
2	AIN ₀		Analog Input Channel 0. Full-scale input range is ±10V.
3	AIN ₁		Analog Input Channel 1. Full-scale input range is ±10V.
4	AIN ₂		Analog Input Channel 2. Full-scale input range is ±10V.
5	AIN ₃		Analog Input Channel 3. Full-scale input range is ±10V.
6	CAP		Internal Reference Output Buffer. 2.2µF Tantalum to ground.
7	REF		Reference Input/Output. Outputs +2.5V nominal. If used externally, must be buffered to maintain ADS7825 accuracy. Can also be driven by external system reference. In both cases, bypass to ground with a 2.2µF Tantalum capacitor.
8	AGND2		Analog Ground.
9	D7	O	Parallel Data Bit 7 if PAR/ $\overline{\text{SER}}$ HIGH; Tri-state if PAR/ $\overline{\text{SER}}$ LOW. See Table I.
10	D6	O	Parallel Data Bit 6 if PAR/ $\overline{\text{SER}}$ HIGH; Tri-state if PAR/ $\overline{\text{SER}}$ LOW. See Table I.
11	D5	O	Parallel Data Bit 5 if PAR/ $\overline{\text{SER}}$ HIGH; Tri-state if PAR/ $\overline{\text{SER}}$ LOW. See Table I.
12	D4	I/O	Parallel Data Bit 4 if PAR/ $\overline{\text{SER}}$ HIGH; if PAR/ $\overline{\text{SER}}$ LOW, a LOW level input here will transmit serial data on SDATA from the previous conversion using the internal serial clock; a HIGH input here will transmit serial data using an external serial clock input on DATACLK (D2). See Table I.
13	D3	O	Parallel Data Bit 3 if PAR/ $\overline{\text{SER}}$ HIGH; SYNC output if PAR/ $\overline{\text{SER}}$ LOW. See Table I.
14	DGND		Digital Ground.
15	D2	I/O	Parallel Data Bit 2 if PAR/ $\overline{\text{SER}}$ HIGH; if PAR/ $\overline{\text{SER}}$ LOW, this will output the internal serial clock if EXT/ $\overline{\text{INT}}$ (D4) is LOW; will be an input for an external serial clock if EXT/ $\overline{\text{INT}}$ (D4) is HIGH. See Table I.
16	D1	O	Parallel Data Bit 1 if PAR/ $\overline{\text{SER}}$ HIGH; SDATA serial data output if PAR/ $\overline{\text{SER}}$ LOW. See Table I.
17	D0	I/O	Parallel Data Bit 0 if PAR/ $\overline{\text{SER}}$ HIGH; TAG data input if PAR/ $\overline{\text{SER}}$ LOW. See Table I.
18	A1	I/O	Channel Address. Input if CONTC LOW, output if CONTC HIGH. See Table I.
19	A0	I/O	Channel Address. Input if CONTC LOW, output if CONTC HIGH. See Table I.
20	PAR/ $\overline{\text{SER}}$	I	Select Parallel or Serial Output. If HIGH, parallel data will be output on D0 thru D7. If LOW, serial data will be output on SDATA. See Table I and Figure 1.
21	BYTE	I	Byte Select. Only used with parallel data, when PAR/ $\overline{\text{SER}}$ HIGH. Determines which byte is available on D0 thru D7. Changing BYTE with $\overline{\text{CS}}$ LOW and R/ $\overline{\text{C}}$ HIGH will cause the data bus to change accordingly. LOW selects the 8 MSBs; HIGH selects the 4 LSBs, see Figures 2 and 3.
22	R/ $\overline{\text{C}}$	I	Read/Convert Input. With $\overline{\text{CS}}$ LOW, a falling edge on R/ $\overline{\text{C}}$ puts the internal sample/hold into the hold state and starts a conversion. With $\overline{\text{CS}}$ LOW, a rising edge on R/ $\overline{\text{C}}$ enables the output data bits if PAR/ $\overline{\text{SER}}$ HIGH, or starts transmission of serial data if PAR/ $\overline{\text{SER}}$ LOW and EXT/ $\overline{\text{INT}}$ HIGH.
23	$\overline{\text{CS}}$	I	Chip Select. Internally OR'd with R/ $\overline{\text{C}}$. With CONTC LOW and R/ $\overline{\text{C}}$ LOW, a falling edge on $\overline{\text{CS}}$ will initiate a conversion. With R/ $\overline{\text{C}}$ HIGH, a falling edge on $\overline{\text{CS}}$ will enable the output data bits if PAR/ $\overline{\text{SER}}$ HIGH, or starts transmission of serial data if PAR/ $\overline{\text{SER}}$ LOW and EXT/ $\overline{\text{INT}}$ HIGH.
24	$\overline{\text{BUSY}}$	O	Busy Output. Falls when conversion is started; remains LOW until the conversion is completed and the data is latched into the output register. In parallel output mode, output data will be valid when $\overline{\text{BUSY}}$ rises, so that the rising edge can be used to latch the data.
25	CONTC	I	Continuous Conversion Input. If LOW, conversions will occur normally when initiated using $\overline{\text{CS}}$ and R/ $\overline{\text{C}}$; if HIGH, acquisition and conversions will take place continually, cycling through all four input channels, as long as $\overline{\text{CS}}$, R/ $\overline{\text{C}}$ and PWRD are LOW. See Table I. For serial mode only.
26	PWRD	I	Power Down Input. If HIGH, conversions are inhibited and power consumption is significantly reduced. Results from the previous conversion are maintained in the output register. In the continuous conversion mode, the multiplexer address channel is reset to channel 0.
27	V _{S2}		Supply Input. Nominally +5V. Connect directly to pin 28. Decouple to ground with 0.1µF ceramic and 10µF Tantalum capacitors.
28	V _{S1}		Supply Input. Nominally +5V. Connect directly to pin 27.

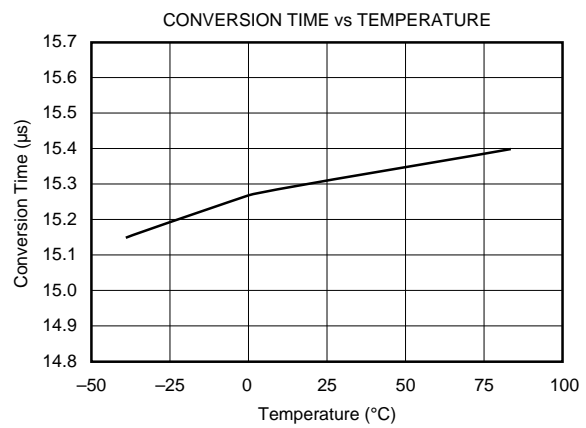
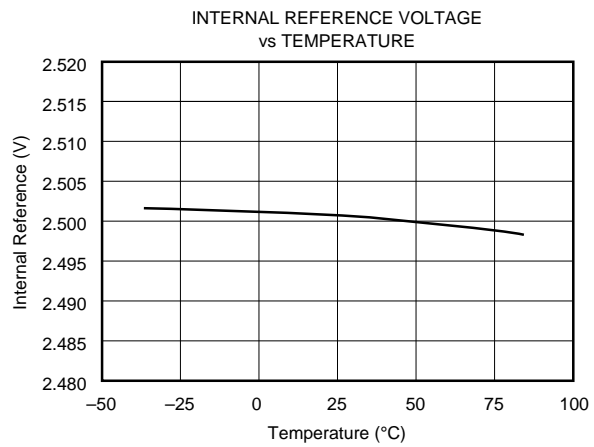
TYPICAL PERFORMANCE CURVES

At $T_A = +25^\circ\text{C}$, $f_S = 40\text{kHz}$, $V_{S1} = V_{S2} = +5\text{V}$, using internal reference, unless otherwise noted.



TYPICAL PERFORMANCE CURVES (CONT)

At $T_A = +25^\circ\text{C}$, $f_S = 40\text{kHz}$, $V_{S1} = V_{S2} = +5\text{V}$, using internal reference, unless otherwise noted.



BASIC OPERATION

PARALLEL OUTPUT

Figure 1a shows a basic circuit to operate the ADS7824 with parallel output (Channel 0 selected). Taking $\overline{R/\overline{C}}$ (pin 22) LOW for 40ns (12 μ s max) will initiate a conversion. \overline{BUSY} (pin 24) will go LOW and stay LOW until the conversion is completed and the output register is updated. If BYTE (pin 21) is LOW, the 8 most significant bits will be valid when pin 24 rises; if BYTE is HIGH, the 4 least significant bits will be valid when \overline{BUSY} rises. Data will be output in Binary Two's Complement format. \overline{BUSY} going HIGH can be used to latch the data. After the first byte has been read, BYTE can be toggled allowing the remaining byte to be read. All convert commands will be ignored while \overline{BUSY} is LOW.

The ADS7824 will begin tracking the input signal at the end of the conversion. Allowing 25 μ s between convert commands assures accurate acquisition of a new signal.

SERIAL OUTPUT

Figure 1b shows a basic circuit to operate the ADS7824 with serial output (Channel 0 selected). Taking $\overline{R/\overline{C}}$ (pin 22) LOW for 40ns (12 μ s max) will initiate a conversion and output valid data from the previous conversion on SDATA (pin 16) synchronized to 12 clock pulses output on DATACLK (pin 15). \overline{BUSY} (pin 24) will go LOW and stay LOW until the conversion is completed and the serial data has been transmitted. Data will be output in Binary Two's Complement format, MSB first, and will be valid on both the rising and falling edges of the data clock. \overline{BUSY} going HIGH can be used to latch the data. All convert commands will be ignored while \overline{BUSY} is LOW.

The ADS7824 will begin tracking the input signal at the end of the conversion. Allowing 25 μ s between convert commands assures accurate acquisition of a new signal.

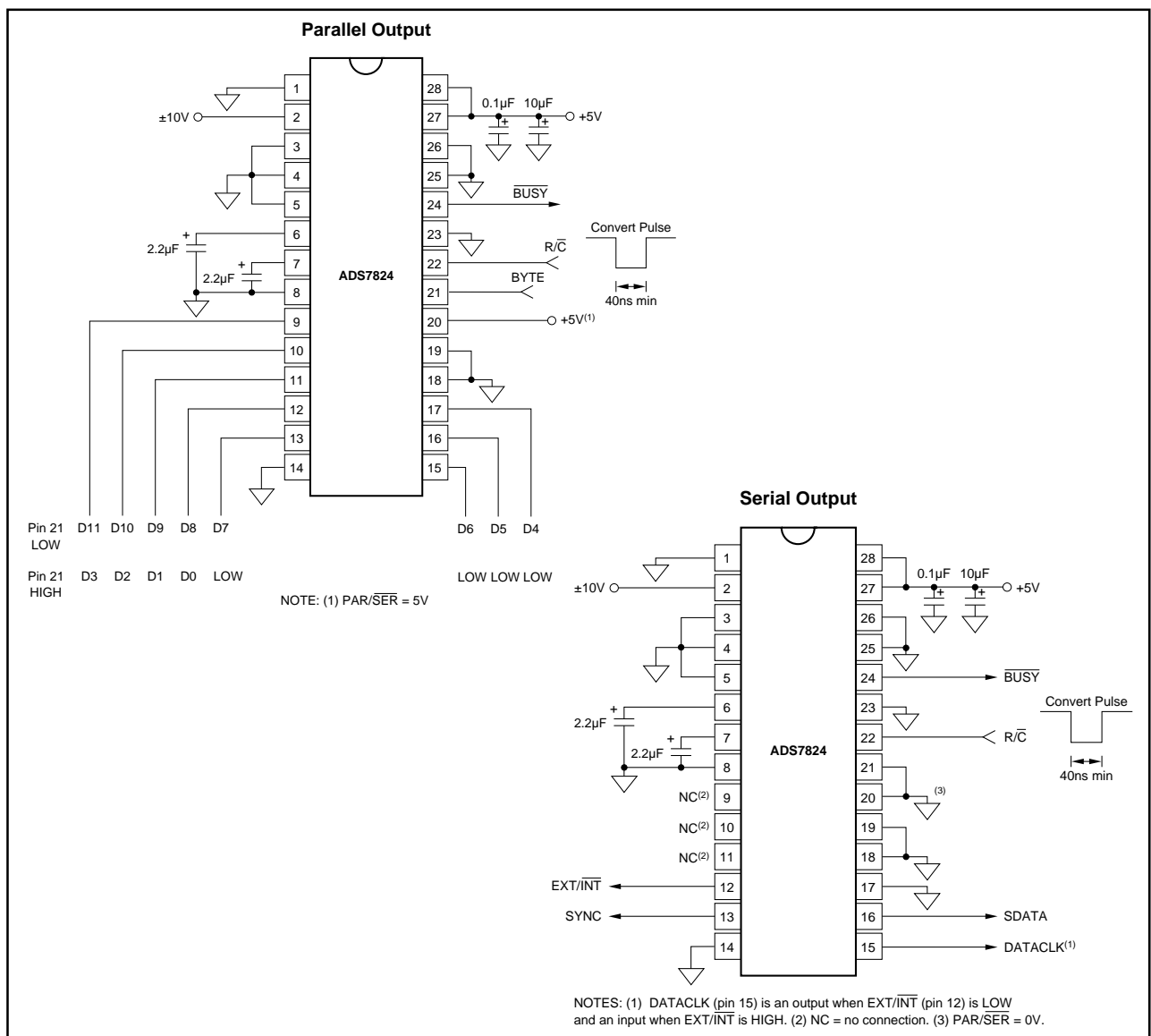


FIGURE 1. Basic Connection Diagram, (a) Parallel Output, (b) Serial Output.

STARTING A CONVERSION

The combination of \overline{CS} (pin 23) and $\overline{R/C}$ (pin 22) LOW for a minimum of 40ns places the sample/hold of the ADS7824 in the hold state and starts conversion 'n'. \overline{BUSY} (pin 24) will go LOW and stay LOW until conversion 'n' is completed and the internal output register has been updated. All new convert commands during \overline{BUSY} LOW will be ignored. \overline{CS} and/or $\overline{R/C}$ must go HIGH before \overline{BUSY} goes HIGH or a new conversion will be initiated without sufficient time to acquire a new signal.

The ADS7824 will begin tracking the input signal at the end of the conversion. Allowing 25 μ s between convert commands assures accurate acquisition of a new signal. Refer to Tables Ia and Ib for a summary of \overline{CS} , $\overline{R/C}$, and \overline{BUSY} states and Figures 2 through 6 and Table II for timing information. \overline{CS} and $\overline{R/C}$ are internally OR'd and level triggered. There is not a requirement which input goes LOW first when

initiating a conversion. If, however, it is critical that \overline{CS} or $\overline{R/C}$ initiates conversion 'n', be sure the less critical input is LOW at least 10ns prior to the initiating input. If $\overline{EXT/INT}$ (pin 12) is LOW when initiating conversion 'n', serial data from conversion 'n - 1' will be output on SDATA (pin 16) following the start of conversion 'n'. See Internal Data Clock in the Reading Data section.

To reduce the number of control pins, \overline{CS} can be tied LOW using $\overline{R/C}$ to control the read and convert modes. This will have no effect when using the internal data clock in the serial output mode. However, the parallel output and the serial output (only when using an external data clock) will be affected whenever $\overline{R/C}$ goes HIGH. Refer to the Reading Data section and Figures 2, 3, 5, and 6.

INPUTS						OUTPUTS									COMMENTS
\overline{CS}	$\overline{R/C}$	BYTE	CONTC	PWRD	\overline{BUSY}	D7	D6	D5	D4	D3	D2	D1	D0		
1	X	X	X	X	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Results from last completed conversion. Results from last completed conversion. Data will change at the end of a conversion.
X	0	X	X	X	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z		
0	1	0	X	X	X	D11 (MSB)	D10	D9	D8	D7	D6	D5	D4		
0	1	1	X	X	X	D3	D2	D1	D0 (LSB)	LOW	LOW	LOW	LOW		
0	1	X	X	X	↑	↑↓	↑↓	↑↓	↑↓	↑↓	↑↓	↑↓	↑↓		

TABLE Ia. Read Control for Parallel Data ($\overline{PAR/SER} = 5V$.)

\overline{CS}	$\overline{R/C}$	CONTC	PWRD	\overline{BUSY}	D7, D6, D5 LOW	D4 EXT/INT	D3 SYNC	D2 DATACLK	D1 SDATA	D0 TAG	COMMENTS
Input	Input	Input	Input	Output	Output	Input	Output	I/O	Output	Input	
1	X	X	X	1	Hi-Z	LOW	LOW	Output	Hi-Z	X	<p>Starts transmission of data from previous conversion on SDATA synchronized to 12 pulses output on DATACLK.</p> <p>Starts transmission of data from previous conversion on SDATA synchronized to 12 pulses output on DATACLK.</p> <p>The level output on SDATA will be the level input on TAG 12 DATACLK input cycles earlier.</p> <p>At the end of the conversion, when \overline{BUSY} rises, data from the conversion will be shifted into the output registers. If DATACLK is HIGH, valid data will be lost.</p> <p>Initiates transmission of a HIGH pulse on SYNC followed by data from last completed conversion on SDATA synchronized to the input on DATACLK.</p> <p>Initiates transmission of a HIGH pulse on SYNC followed by data from last completed conversion on SDATA synchronized to the input on DATACLK.</p> <p>Starts transmission of data from previous conversion on SDATA synchronized to 12 pulses output on DATACLK</p> <p>SDATA becomes active. Inputs on DATACLK shift out data.</p> <p>SDATA becomes active. Inputs on DATACLK shift out data.</p> <p>Restarts continuous conversion mode (n - 1 data transmitted when \overline{BUSY} is LOW).</p> <p>Restarts continuous conversion mode (n - 1 data transmitted when \overline{BUSY} is LOW).</p>
X	0	X	X	1	Hi-Z	LOW	LOW	Output	Hi-Z	X	
0	↓	0	X	1	Hi-Z	LOW	LOW	Output	Output	X	
↓	0	0	X	1	Hi-Z	LOW	LOW	Output	Output	X	
0	1	0	X	X	Hi-Z	HIGH	LOW	Input	Output	Input	
0	1	0	X	↑	Hi-Z	HIGH	LOW	Input	Output	Input	
0	↑	0	X	1	Hi-Z	HIGH	LOW	Input	Output	X	
↓	1	0	X	1	Hi-Z	HIGH	LOW	Input	Output	X	
0	0	1	0	↓	Hi-Z	LOW	LOW	Output	Output	X	
↓	1	X	X	X	Hi-Z	HIGH	Output	Input	Output	X	
0	↑	X	X	X	Hi-Z	HIGH	Output	Input	Output	X	
↓	0	1	X	X	Hi-Z	LOW	LOW	Output	Output	X	
0	↓	1	X	X	Hi-Z	LOW	LOW	Output	Output	X	

TABLE Ib. Read Control for Serial Data ($\overline{PAR/SER} = 0V$.)

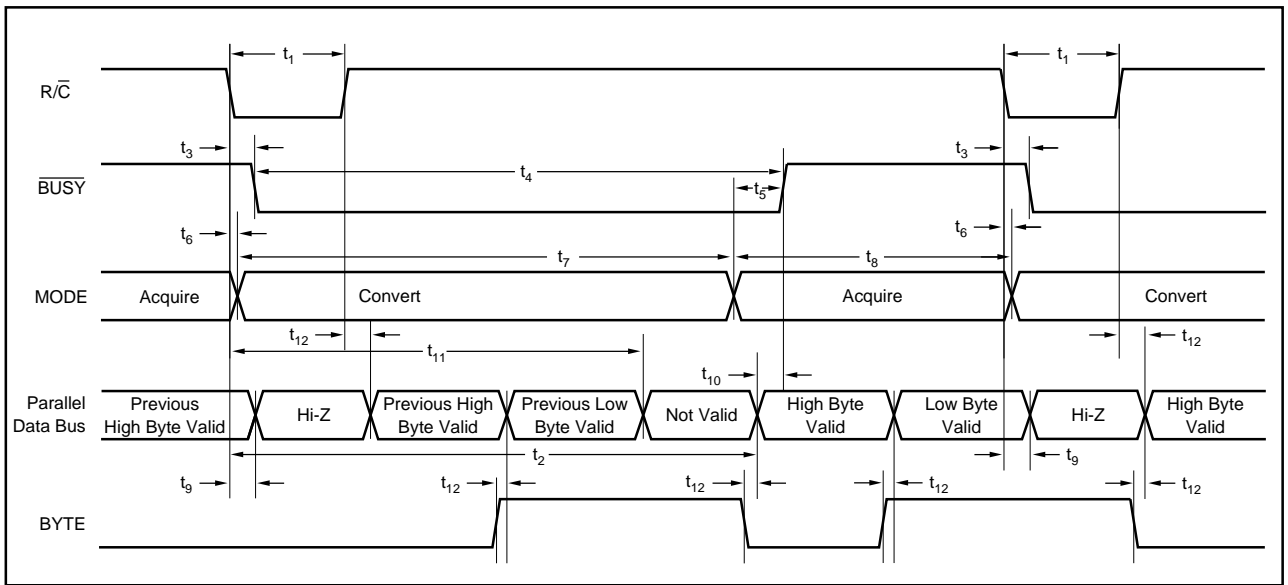


FIGURE 2. Conversion Timing with Parallel Output (\overline{CS} LOW).

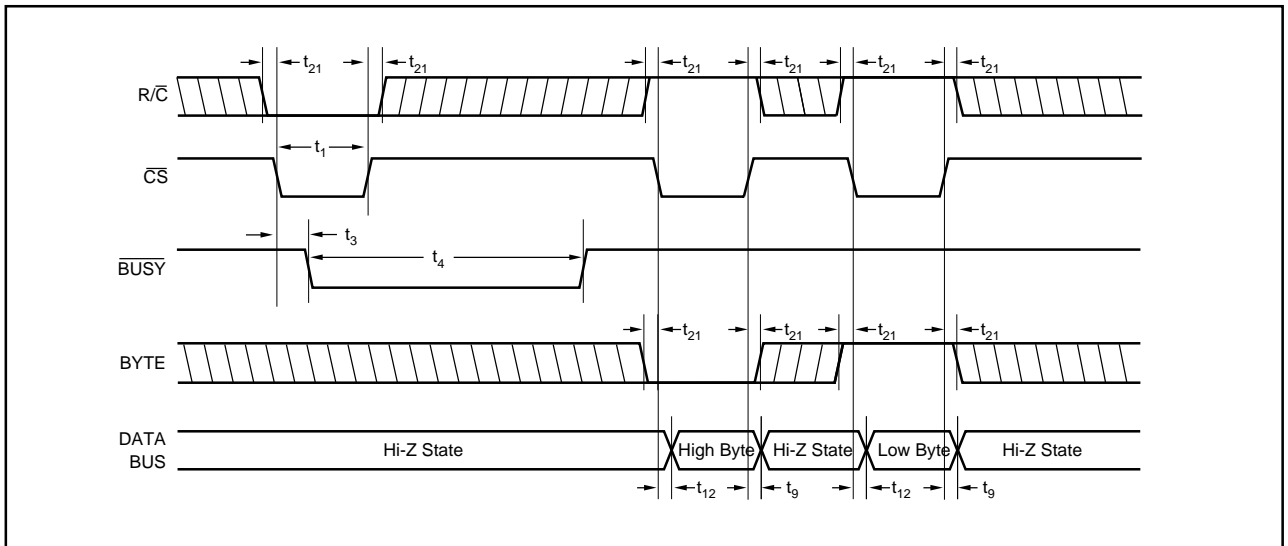


FIGURE 3. Using \overline{CS} to Control Conversion and Read Timing with Parallel Outputs.

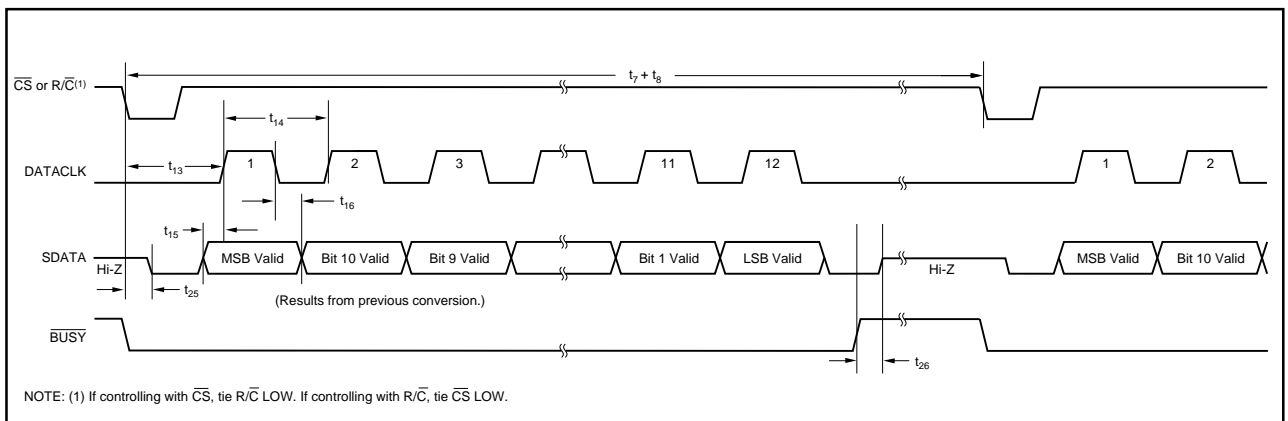


FIGURE 4. Serial Data Timing Using Internal Data Clock (TAG LOW).

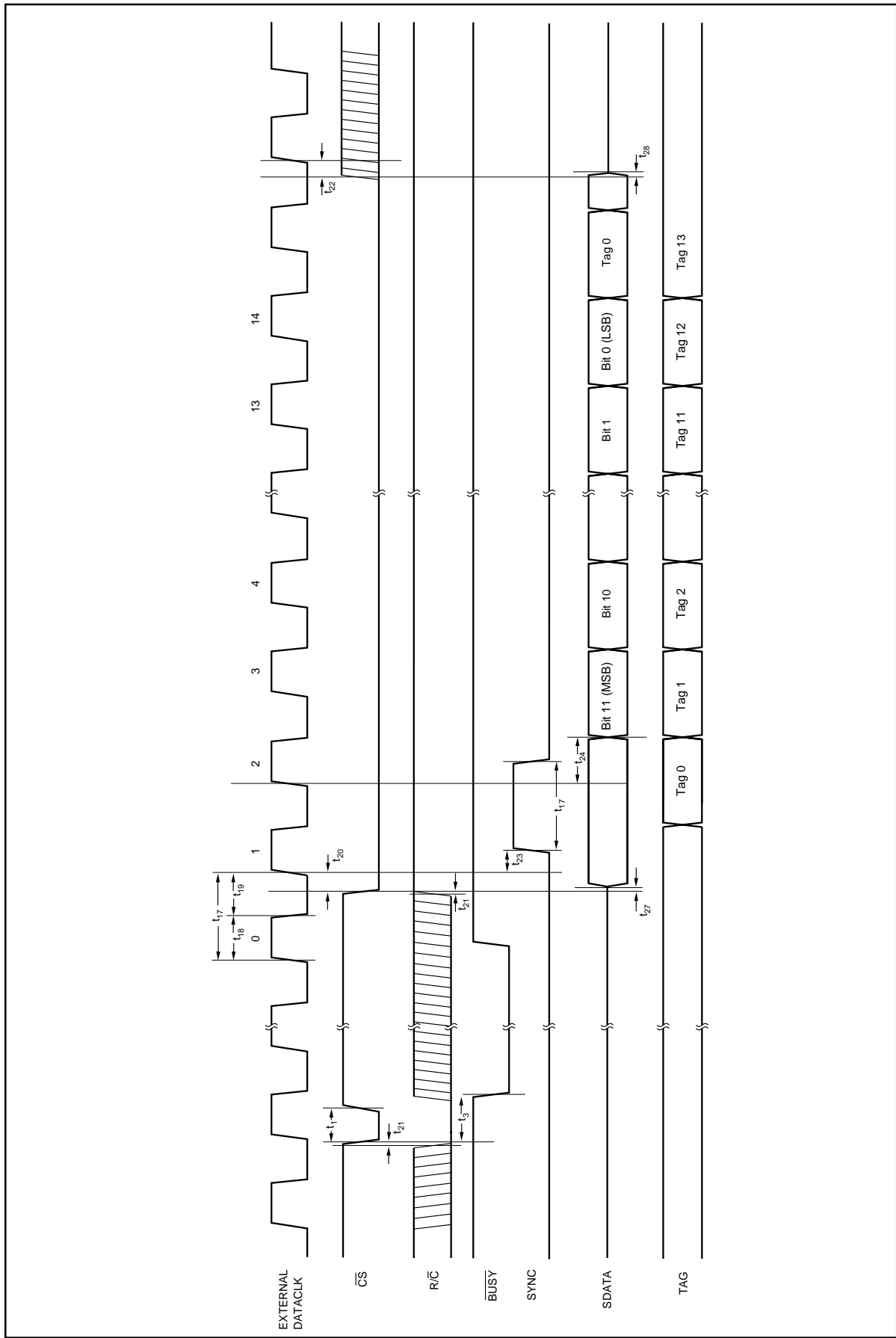


FIGURE 5. Conversion and Read Timing with External Clock (EXT/INT HIGH). Read After Conversion.

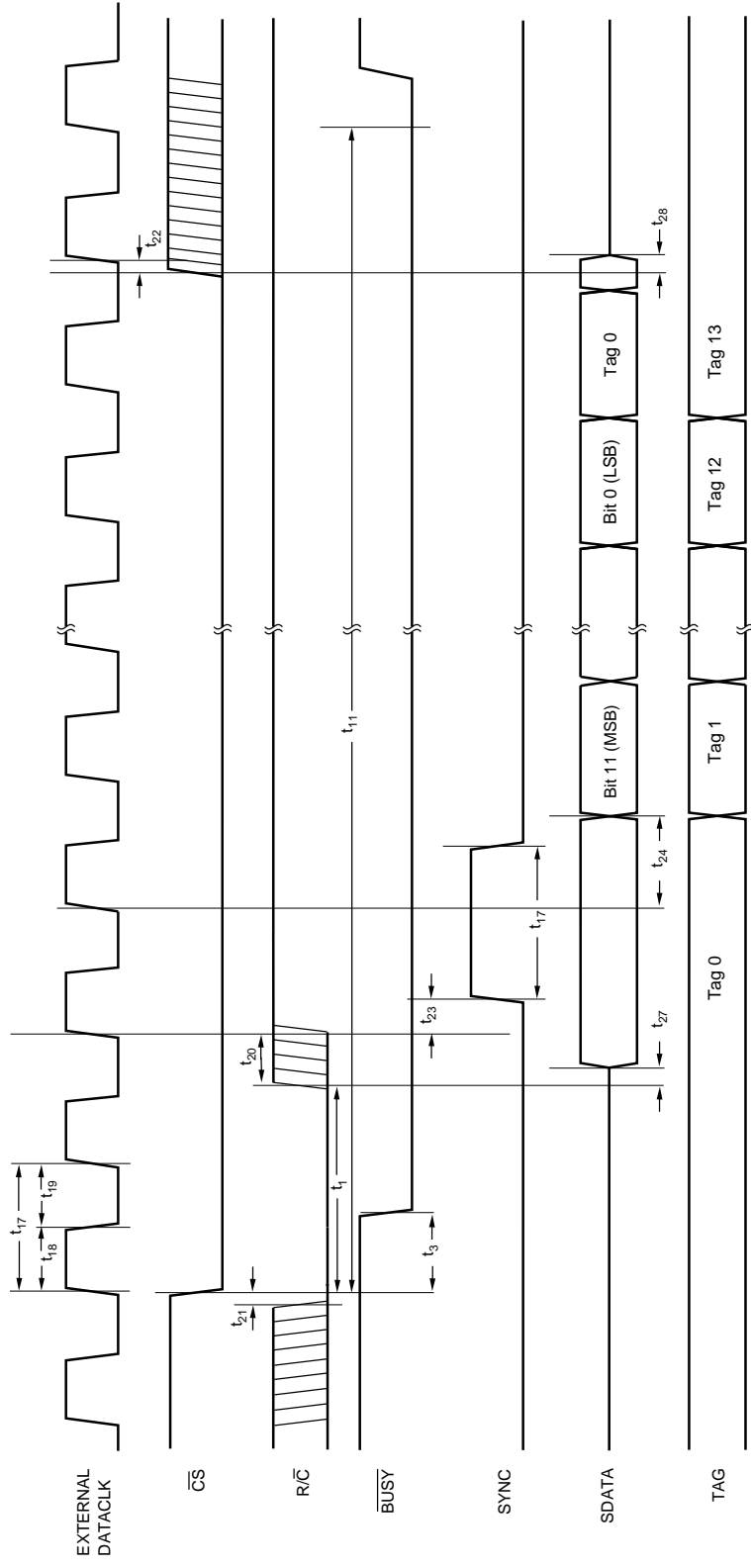


FIGURE 6. Conversion and Read Timing with External Clock (EXT/INT HIGH). Read During Conversion (Previous Conversion Results).

READING DATA

PARALLEL OUTPUT

To use the parallel output, tie $\overline{\text{PAR/SER}}$ (pin 20) HIGH. The parallel output will be active when $\overline{\text{R/C}}$ (pin 22) is HIGH and $\overline{\text{CS}}$ (pin 23) is LOW. Any other combination of $\overline{\text{CS}}$ and $\overline{\text{R/C}}$ will tri-state the parallel output. Valid conversion data can be read in two 8-bit bytes on D7-D0 (pins 9-13 and 15-17). When BYTE (pin 21) is LOW, the 8 most significant bits will be valid with the MSB on D7. When BYTE is HIGH, the 4 least significant bits will be valid with the LSB on D4. BYTE can be toggled to read both bytes within one conversion cycle.

Upon initial power up, the parallel output will contain indeterminate data.

PARALLEL OUTPUT (After a Conversion)

After conversion 'n' is completed and the output registers have been updated, $\overline{\text{BUSY}}$ (pin 24) will go HIGH. Valid data from conversion 'n' will be available on D7-D0 (pins 9-13 and 15-17). $\overline{\text{BUSY}}$ going HIGH can be used to latch the data. Refer to Table II and Figures 2 and 3 for timing constraints.

PARALLEL OUTPUT (During a Conversion)

After conversion 'n' has been initiated, valid data from conversion 'n - 1' can be read and will be valid up to 12 μ s

after the start of conversion 'n'. Do not attempt to read data beyond 12 μ s after the start of conversion 'n' until $\overline{\text{BUSY}}$ (pin 24) goes HIGH; this may result in reading invalid data. Refer to Table II and Figures 2 and 3 for timing constraints.

SERIAL OUTPUT

When $\overline{\text{PAR/SER}}$ (pin 20) is LOW, data can be clocked out serially with the internal data clock or an external data clock. When $\overline{\text{EXT/INT}}$ (pin 12) is LOW, $\overline{\text{DATACLK}}$ (pin 15) is an output and is always active regardless of the state of $\overline{\text{CS}}$ (pin 23) and $\overline{\text{R/C}}$ (pin 22). The $\overline{\text{SDATA}}$ output is active when $\overline{\text{BUSY}}$ (pin 24) is LOW. Otherwise, it is in a tri-state condition. When $\overline{\text{EXT/INT}}$ is HIGH, $\overline{\text{DATACLK}}$ is an input. The $\overline{\text{SDATA}}$ output is active when $\overline{\text{CS}}$ is LOW and $\overline{\text{R/C}}$ is HIGH. Otherwise, it is in a tri-state condition. Regardless of the state of $\overline{\text{EXT/INT}}$, SYNC (pin 13) is an output and always active, while TAG (pin 17) is always an input.

INTERNAL DATA CLOCK (During A Conversion)

To use the internal data clock, tie $\overline{\text{EXT/INT}}$ (pin 12) LOW. The combination of $\overline{\text{R/C}}$ (pin 22) and $\overline{\text{CS}}$ (pin 23) LOW will initiate conversion 'n' and activate the internal data clock (typically 900kHz clock rate). The ADS7824 will output 12 bits of valid data, MSB first, from conversion 'n - 1' on $\overline{\text{SDATA}}$ (pin 16), synchronized to 12 clock pulses output on $\overline{\text{DATACLK}}$ (pin 15). The data will be valid on both the

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_1	Convert Pulse Width	0.04		12	μ s
t_2	Start of Conversion to New Data Valid		15	21	μ s
t_3	Start of Conversion to $\overline{\text{BUSY}}$ LOW			85	ns
t_4	$\overline{\text{BUSY}}$ LOW		15	21	μ s
t_5	End of Conversion to $\overline{\text{BUSY}}$ HIGH		90		ns
t_6	Aperture Delay		40		ns
t_7	Conversion Time		15	21	μ s
t_8	Acquisition Time		3	5	μ s
$t_7 + t_8$	Throughput Time			25	μ s
t_9	Bus Relinquish Time	10		83	ns
t_{10}	Data Valid to $\overline{\text{BUSY}}$ HIGH	20	60		ns
t_{11}	Start of Conversion to Previous Data Not Valid	12	15		μ s
t_{12}	Bus Access Time and BYTE Delay			83	ns
t_{13}	Start of Conversion to $\overline{\text{DATACLK}}$ Delay		1.4		μ s
t_{14}	$\overline{\text{DATACLK}}$ Period		1.1		μ s
t_{15}	Data Valid to $\overline{\text{DATACLK}}$ HIGH	20	75		ns
t_{16}	$\overline{\text{DATACLK}}$ LOW to Data Not Valid	400	600		ns
t_{17}	External $\overline{\text{DATACLK}}$ Period	100			ns
t_{18}	External $\overline{\text{DATACLK}}$ HIGH	50			ns
t_{19}	External $\overline{\text{DATACLK}}$ LOW	40			ns
t_{20}	$\overline{\text{CS}}$ LOW and $\overline{\text{R/C}}$ HIGH to External $\overline{\text{DATACLK}}$ HIGH (Enable Clock)	25			ns
t_{21}	$\overline{\text{R/C}}$ to $\overline{\text{CS}}$ Setup Time	10			ns
t_{22}	$\overline{\text{CS}}$ HIGH or $\overline{\text{R/C}}$ LOW to External $\overline{\text{DATACLK}}$ HIGH (Disable Clock)	25			ns
t_{23}	$\overline{\text{DATACLK}}$ HIGH to SYNC HIGH	15		35	ns
t_{24}	$\overline{\text{DATACLK}}$ HIGH to Valid Data	25		55	ns
t_{25}	Start of Conversion to $\overline{\text{SDATA}}$ Active			83	ns
t_{26}	End of Conversion to $\overline{\text{SDATA}}$ Tri-State			83	ns
t_{27}	$\overline{\text{CS}}$ LOW and $\overline{\text{R/C}}$ HIGH to $\overline{\text{SDATA}}$ Active			83	ns
t_{28}	$\overline{\text{CS}}$ HIGH or $\overline{\text{R/C}}$ LOW to $\overline{\text{SDATA}}$ Tri-State			83	ns
t_{29}	$\overline{\text{BUSY}}$ HIGH to Address Valid			20	ns
t_{30}	Address Valid to $\overline{\text{BUSY}}$ LOW	500			ns

TABLE II. Conversion, Data, and Address Timing. $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$.

rising and falling edges of the internal data clock. The rising edge of $\overline{\text{BUSY}}$ (pin 24) can be used to latch the data. After the 12th clock pulse, DATACLK will remain LOW until the next conversion is initiated, while SDATA will go to whatever logic level was input on TAG (pin 17) during the first clock pulse. The SDATA output will tri-state when $\overline{\text{BUSY}}$ returns HIGH. Refer to Table II and Figure 4 for timing information.

EXTERNAL DATA CLOCK

To use an external clock, tie $\overline{\text{EXT/INT}}$ (pin 12) HIGH. The external clock is not a conversion clock; it can only be used as a data clock. To enable the output mode of the ADS7824, $\overline{\text{CS}}$ (pin 23) must be LOW and $\text{R}/\overline{\text{C}}$ (pin 22) must be HIGH. DATACLK must be HIGH for 20% to 70% of the total data clock period; the clock rate can be between DC and 10MHz. Serial data from conversion 'n' can be output on SDATA (pin 16) after conversion 'n' is completed or during conversion 'n + 1'.

An obvious way to simplify control of the converter is to tie $\overline{\text{CS}}$ LOW while using $\text{R}/\overline{\text{C}}$ to initiate conversions. While this is perfectly acceptable, there is a possible problem when using an external data clock. At an indeterminate point from 12 μs after the start of conversion 'n' until $\overline{\text{BUSY}}$ rises, the internal logic will shift the results of conversion 'n' into the output register. If $\overline{\text{CS}}$ is LOW, $\text{R}/\overline{\text{C}}$ is HIGH and the external clock is HIGH at this point, data will be lost. So, with $\overline{\text{CS}}$ LOW, either $\text{R}/\overline{\text{C}}$ and/or DATACLK must be LOW during this period to avoid losing valid data.

EXTERNAL DATA CLOCK (After a Conversion)

After conversion 'n' is completed and the output registers have been updated, $\overline{\text{BUSY}}$ (pin 24) will go HIGH. With $\overline{\text{CS}}$ LOW (pin 23) and $\text{R}/\overline{\text{C}}$ HIGH (pin 22), valid data from conversion 'n' will be output on SDATA (pin 16) synchronized to the external data clock input on DATACLK (pin 15). Between 15 and 35ns following the rising edge of the first external data clock, the SYNC output pin will go HIGH for one full data clock period (100ns minimum). The MSB will be valid between 25 and 55ns after the rising edge of the second data clock. The LSB will be valid on the 13th falling edge and the 14th rising edge of the data clock. TAG (pin 17) will input a bit of data for every external clock pulse. The first bit input on TAG will be valid on SDATA on the

14th falling edge and the 15th rising edge of DATACLK ; the second input bit will be valid on the 15th falling edge and the 16th rising edge, etc. With a continuous data clock, TAG data will be output on DATA until the internal output registers are updated with the results from the next conversion. Refer to Table II and Figure 5 for timing information.

EXTERNAL DATA CLOCK (During a Conversion)

After conversion 'n' has been initiated, valid data from conversion 'n - 1' can be read and will be valid up to 12 μs after the start of conversion 'n'. Do not attempt to clock out data from 12 μs after the start of conversion 'n' until $\overline{\text{BUSY}}$ (pin 24) rises; this will result in data loss.

NOTE: For the best possible performance when using an external data clock, data should not be clocked out during a conversion. The switching noise of the asynchronous data clock can cause digital feedthrough degrading the converter's performance. Refer to Table II and Figure 6 for timing information.

TAG FEATURE

TAG (pin 17) inputs serial data synchronized to the external or internal data clock.

When using an external data clock, the serial bit stream input on TAG will follow the LSB output on SDATA (pin 16) until the internal output register is updated with new conversion results. See Table II and Figures 5 and 6.

The logic level input on TAG for the first rising edge of the internal data clock will be valid on SDATA after all 12 bits of valid data have been output.

MULTIPLEXER TIMING

The four channel input multiplexer may be addressed manually or placed in a continuous conversion mode where all four channels are sequentially addressed.

CONTINUOUS CONVERSION MODE (CONTC= 5V)

To place the ADS7824 in the continuous conversion mode, CONTC (pin 25) must be tied HIGH. In this mode, acquisition and conversions will take place continually, cycling through all four channels as long as $\overline{\text{CS}}$, $\text{R}/\overline{\text{C}}$ and PWRD are LOW (See Table III). Whichever address was last loaded

CONTC	$\overline{\text{CS}}$	$\text{R}/\overline{\text{C}}$	$\overline{\text{BUSY}}$	PWRD	A0 and A1	OPERATION
0	X	X	X	X	Inputs	Initiating conversion n latches in the levels input on A0 and A1 to select the channel for conversion 'n + 1'.
0	X	X	0	0	Inputs	Conversion in process. New convert commands ignored.
0	0	↓	1	0	Inputs	Initiates conversion on channel selected at start of previous conversion.
0	↓	0	1	0	Inputs	Initiates conversion on channel selected at start of previous conversion.
0	X	X	X	1	Inputs	All analog functions powered down. Conversions in process or initiated will yield meaningless data.
1	X	X	X	X	Outputs	The end of conversion n (when $\overline{\text{BUSY}}$ rises) increments the internal channel latches and outputs the channel address for conversion 'n + 1' on A0 and A1.
1	X	X	0	0	Outputs	Conversion in process.
1	0	↓	1	0	Outputs	Restarts continuous conversion process on next input channel.
1	↓	0	1	0	Outputs	Restarts continuous conversion process on next input channel.
1	X	X	X	1	Outputs	All analog functions powered down. Conversions in process or initiated will yield meaningless data. Resets selected input channel for next conversion to AIN_0 .

TABLE III. Conversion Control.

into the A0 and A1 registers (pins 19 and 18, respectively) prior to $\overline{\text{CONTC}}$ being raised HIGH, becomes the first address in the sequential continuous conversion mode (e.g., if Channel 1 was the last address selected then Channel 2 will follow, then Channel 3, and so on). The A0 and A1 address inputs become outputs when the device is in this mode. When $\overline{\text{BUSY}}$ rises at the end of a conversion, A0 and A1 will output the address of the channel that will be converted when $\overline{\text{BUSY}}$ goes LOW at the beginning of the next conversion. Data will be valid for the previous channel after $\overline{\text{BUSY}}$ rises. The address lines are updated when $\overline{\text{BUSY}}$ rises. See Table IVa and Figure 7 for channel selection timing in continuous conversion mode.

PWRD (pin 26) can be used to reset the multiplexer address to zero. With the ADS7824 configured for no conversion, PWRD can be taken HIGH for a minimum of 200ns. When PWRD returns LOW, the multiplexer address will be reset to zero. When the continuous conversion mode is enabled, the first conversion will be done on Channel 0. Subsequent

conversions will proceed through each higher channel, cycling back to zero after Channel 3.

If PWRD is held HIGH for a significant period of time, the REF (pin 7) bypass capacitor may discharge (if the internal reference is being utilized) and the CAP (pin 6) bypass capacitor will discharge (for both internal and external references). The continuous conversion mode should not be enabled until the bypass capacitor(s) have recharged and stabilized (1ms for 2.2 μ F capacitors recommended). In addition, the continuous conversion mode should not be enabled even with a short pulse on PWRD until the minimum acquisition time has been met.

MANUAL CHANNEL SELECTION ($\overline{\text{CONTC}} = 0\text{V}$)

The channels of the ADS7824 can be selected manually by using the A0 and A1 address pins (pins 19 and 18, respectively). See Table IVb for the multiplexer truth table and Figure 8 for channel selection timing.

ADS7824 TIMING AND CONTROL

A1	A0	DATA AVAILABLE FROM CHANNEL	CHANNEL TO BE OR BEING CONVERTED	DESCRIPTION OF OPERATION
0	0	AIN ₃	AIN ₀	Channel being acquired or converted is output on these address lines. Data is valid for the previous channel. These lines are updated when $\overline{\text{BUSY}}$ rises.
0	1	AIN ₀	AIN ₁	
1	0	AIN ₁	AIN ₂	
1	1	AIN ₂	AIN ₃	

TABLE IVa. A0 and A1 Outputs ($\overline{\text{CONTC}}$ HIGH).

A1	A0	CHANNEL SELECTED WHEN $\overline{\text{BUSY}}$ GOES HIGH	DESCRIPTION OF OPERATION
0	0	AIN ₀	Channel to be converted during conversion 'n + 1' is latched when conversion 'n' is initiated ($\overline{\text{BUSY}}$ goes LOW). The selected input starts being acquired as soon as conversion 'n' is done ($\overline{\text{BUSY}}$ goes HIGH).
0	1	AIN ₁	
1	0	AIN ₂	
1	1	AIN ₃	

TABLE IVb. A0 and A1 Inputs ($\overline{\text{CONTC}}$ LOW).

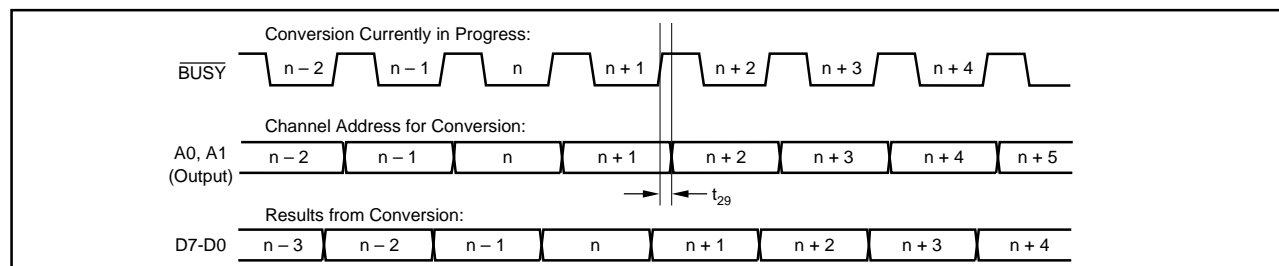


FIGURE 7. Channel Addressing in Continuous Conversion Mode ($\overline{\text{CONTC}}$ HIGH, $\overline{\text{CS}}$ and $\overline{\text{R/C}}$ LOW).

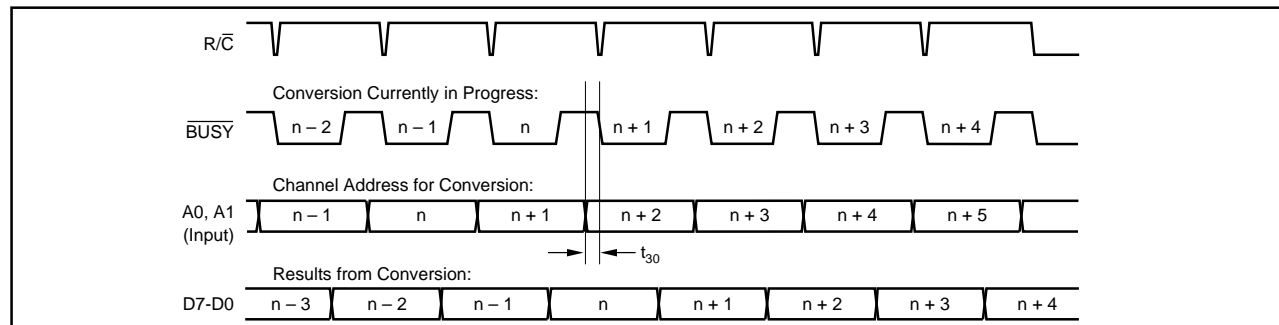


FIGURE 8. Channel Addressing in Normal Conversion Mode ($\overline{\text{CONTC}}$ and $\overline{\text{CS}}$ LOW).

CALIBRATION

The ADS7824 has no internal provision for correcting the individual bipolar zero error or full-scale error for each individual channel. Instead, the bipolar zero error of each channel is guaranteed to be below a level which is quite small for a converter with a $\pm 10\text{V}$ input range (slightly more than ± 2 LSBs). In addition, the channel errors should match each other to within 1 LSB.

For the full-scale error, the circuit of Figure 9 can be used. This will allow the reference to be adjusted such that the full-scale error for any single channel can be set to zero. Again, the close matching of the channels will ensure that the full-scale errors on the other channels will be small.

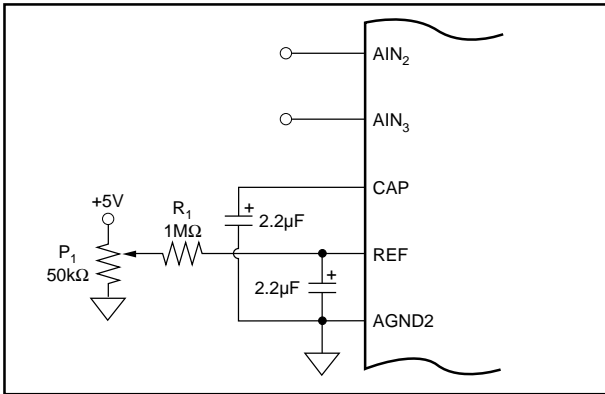


FIGURE 9. Full Scale Trim.

REFERENCE

The ADS7824 can operate with its internal 2.5V reference or an external reference. By applying an external reference to pin 7, the internal reference can be bypassed.

REF

REF (pin 7) is an input for an external reference or the output for the internal 2.5V reference. A 2.2 μF capacitor should be connected as close to the REF pin as possible. This capacitor and the output resistance of REF create a low pass filter to bandlimit noise on the reference. Using a smaller value capacitor will introduce more noise to the reference degrading the SNR and SINAD. The REF pin should not be used to drive external AC or DC loads.

The range for the external reference is 2.3V to 2.7V and determines the actual LSB size. Increasing the reference voltage will increase the full scale range and the LSB size of the converter which can improve the SNR.

CAP

CAP (pin 6) is the output of the internal reference buffer. A 2.2 μF capacitor should be placed as close to the CAP pin as possible to provide optimum switching currents for the CDAC throughout the conversion cycle. This capacitor also provides compensation for the output of the buffer. Using a capacitor any smaller than 1 μF can cause the output buffer to oscillate and may not have sufficient charge for the

CDAC. Capacitor values larger than 2.2 μF will have little affect on improving performance.

The output of the buffer is capable of driving up to 1mA of current to a DC load. Using an external buffer will allow the internal reference to be used for larger DC loads and AC loads. Do not attempt to directly drive an AC load with the output voltage on CAP. This will cause performance degradation of the converter.

PWRD

PWRD (pin 26) HIGH will power down all of the analog circuitry including the reference. Data from the previous conversion will be maintained in the internal registers and can still be read. With PWRD HIGH, a convert command yields meaningless data. When PWRD is returned LOW, adequate time must be provided in order for the capacitors on REF (pin 7) and CAP (pin 6) to recharge. For 2.2 μF capacitors, a minimum recharge/settling time of 1ms is recommended before the conversion results should be considered valid.

LAYOUT

POWER

The ADS7824 uses 90% of its power for the analog circuitry, and the converter should be considered an analog component. For optimum performance, tie both power pins to the same +5V power supply and tie the analog and digital grounds together.

The +5V power for the converter should be separate from the +5V used for the system's digital logic. Connecting V_{S1} and V_{S2} (pins 28 and 27) directly to a digital supply can reduce converter performance due to switching noise from the digital logic. For best performance, the +5V supply can be produced from whatever analog supply is used for the rest of the analog signal conditioning. If +12V or +15V supplies are present, a simple +5V regulator can be used. Although it is not suggested, if the digital supply must be used to power the converter, be sure to properly filter the supply. Either using a filtered digital supply or a regulated analog supply, both V_{S1} and V_{S2} should be tied to the same +5V source.

GROUNDING

Three ground pins are present on the ADS7824. DGND is the digital supply ground. AGND2 is the analog supply ground. AGND1 is the ground which all analog signals internal to the A/D are referenced. AGND1 is more susceptible to current induced voltage drops and must have the path of least resistance back to the power supply.

All the ground pins of the A/D should be tied to an analog ground plane, separated from the system's digital logic ground, to achieve optimum performance. Both analog and digital ground planes should be tied to the 'system' ground as near to the power supplies as possible. This helps to prevent dynamic digital ground currents from modulating the analog ground through a common impedance to power ground.

CROSSTALK

With a full-scale 1kHz input signal, worst case crosstalk on the ADS7824 is better than -95dB. This should be adequate for even the most demanding applications. However, if crosstalk is a concern, the following items should be kept in mind:

The worst case crosstalk is generally from Channel 3 to 2. In addition, crosstalk from Channel 3 to any other channel is worse than from those channels to Channel 3. The reason for this is that channel three is nearer to the reference on the ADS7824. This allows two coupling modes: channel-to-channel and Channel 3 to the reference. In general, when crosstalk is a concern, avoid placing signals with higher frequency components on Channel 3.

If a particular channel should be as immune as possible from crosstalk, Channel 0 would be the best channel for the signal and Channel 1 should have the signal with the lowest frequency content. If two signals are to have as little crosstalk as possible, they should be placed on Channel 0 and Channel 2 with lower frequency, less-sensitive inputs on the other channels.

SIGNAL CONDITIONING

The FET switches used for the sample hold on many CMOS A/D converters release a significant amount of charge injection which can cause the driving op amp to oscillate. The amount of charge injection due to the sampling FET switch on the ADS7824 is approximately 5-10% of the amount on similar ADCs with the charge redistribution DAC (CDAC) architecture. There is also a resistive front end which attenuates any charge which is released. The end result is a

minimal requirement for the drive capability on the signal conditioning preceding the A/D. Any op amp sufficient for the signal in an application will be sufficient to drive the ADS7824.

The resistive front end of the ADS7824 also provides a guaranteed $\pm 15V$ overvoltage protection. In most cases, this eliminates the need for external over voltage protection circuitry.

INTERMEDIATE LATCHES

The ADS7824 does have tri-state outputs for the parallel port, but intermediate latches should be used if the bus will be active during conversions. If the bus is not active during conversions, the tri-state outputs can be used to isolate the A/D from other peripherals on the same bus.

Intermediate latches are beneficial on any monolithic A/D converter. The ADS7824 has an internal LSB size of $610\mu V$. Transients from fast switching signals on the parallel port, even when the A/D is tri-stated, can be coupled through the substrate to the analog circuitry causing degradation of converter performance. The effect of this phenomenon will be more obvious when using the pin-compatible ADS7825 or any of the other 16-bit converters in the ADS Family. This is due to the smaller LSB size of $38\mu V$.

For an ADS7824 with proper layout, grounding, and bypassing; the effect should only be a few tenths of an LSB at the most. In those cases where this is not true, it is possible for the conversion results to exhibit random errors of many LSBs. Poor grounding, poor bypassing, and high-speed digital signals will increase the magnitude of the errors.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS7824P	ACTIVE	PDIP	NT	28	13	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		ADS7824P	Samples
ADS7824PB	ACTIVE	PDIP	NT	28	13	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		ADS7824P B	Samples
ADS7824PBG4	ACTIVE	PDIP	NT	28	13	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		ADS7824P B	Samples
ADS7824PG4	ACTIVE	PDIP	NT	28	13	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		ADS7824P	Samples
ADS7824U	ACTIVE	SOIC	DW	28	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	ADS7824U	Samples
ADS7824U/1K	ACTIVE	SOIC	DW	28	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	ADS7824U	Samples
ADS7824U/1KE4	ACTIVE	SOIC	DW	28	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	ADS7824U	Samples
ADS7824UB	ACTIVE	SOIC	DW	28	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	ADS7824U B	Samples
ADS7824UBE4	ACTIVE	SOIC	DW	28	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	ADS7824U B	Samples
ADS7824UE4	ACTIVE	SOIC	DW	28	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	ADS7824U	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

- (3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS7824U/1K	SOIC	DW	28	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS7824U/1K	SOIC	DW	28	1000	367.0	367.0	55.0

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