LatticeECP3 Family

Build Leading Edge Systems with Proven 3rd Generation FPGAs

LatticeECP3™ is the best-in-class mid-range FPGA with high-performance SERDES, full-featured DSP blocks, and support for state-of-the-art memory interfaces including DDR3. It offers 35% to 100% more silicon resources in smaller packages compared to competitors. Low-power LatticeECP3 FPGAs are used in a wide range of applications, such as wireless and wireline communication, video processing, security and surveillance, industrial networking, industrial automation, computing, storage, medical equipment, and consumer.

LatticeECP3 FPGAs offer up to 150K LUTs of logic capacity and 7 Mbits of memory for system integration, cascadable high-performance DSP blocks for signal processing, high-speed memory interfaces including DDR3 at 800 Mbps, and up to 1 Gbps LVDS performance for ADC/DAC and SPI4.2 interfaces. LatticeECP3 further enables you to build high-speed systems with proven 3.2 Gbps low-power SERDES qualified for a number of protocols – PCI Express 1.1, Ethernet (GbE, SGMII & XAUI), SMPTE SDI (3G/HD/SD), Serial RapidIO 2.1, low-latency CPRI, and JESD204A.

To accelerate design of LatticeECP3 powered systems, Lattice also offers a number of generic and application-specific development kits, an expanding portfolio of free readymade reference designs, and a set of economical IP suites.

FPGA Fabric Features and Capabilities

- **Low-Power, High-Value FPGA Fabric**
  - Low-power 65nm process with 4-input look-up table (LUT) fabric
  - Logic densities from 17K to 149K LUTs
  - Up to 7Mbits of Embedded Block RAM (EBR) and 303Kbits of distributed RAM
- **High-Speed Embedded SERDES**
  - Up to 16 channels with data rates from 150Mbps to 3.2Gbps
  - Less than 110mW power per channel at 3.2Gbps
  - Supports PCI Express, Ethernet (GbE, XAUI, SGMII), SMPTE, Serial RapidIO 2.1, CPRI
- **Flexible sysIO™ Buffers**
  - LVCMOS 33/25/18/15/12, PCI
  - SSTL 33/25/18/15 & HSTL15 & HSTL18
  - LVDS, Bus-LVDS, RSDS, MLVDS & LVPECL
  - 800Mbps DDR3
  - Up to 1Gbps LVDS
- **Wide Range of Package & User I/O Options**
  - Up to 586 user I/O pins
  - Proven low-cost wirebond fpBGA packages
  - Density migration across all densities
  - Pb-free / RoHS-compliant
- **sysCLOCK™ PLL and DLL**
  - 2 DLLs per device, 2 to 10 PLLs per device

LatticeECP3 Features and Benefits

Embedded SERDES

- 3.2Gbps operation with less than 110mW power per channel
- Built-in pre-emphasis and equalization
- Supports PCIe, Ethernet (GbE, XAUI, & SGMII), SMPTE, Serial RapidIO, CPRI and JESD204A
- Quad-based architecture with mix and match of different protocols within a quad
- Single-channel granularity for 3G/HD/SD SDI
- Support low latency variation CPRI links for multi-hop RRH applications

Cascadable DSP with ALU

- Fully cascadable slice for high performance filter and wide arithmetic functions
- Implement rounding and truncation functions with 54-bit cascadable arithmetic logic unit
- Multiply, accumulate, addition and subtraction
- Up to 320 18x18 multipliers

High-Speed I/O

- Pre-engineered DDR3 memory (800Mbps)
- Up to 1Gbps LVDS
- ADC/DAC, 7:1 LVDS, XGMII

Advanced Configuration Options

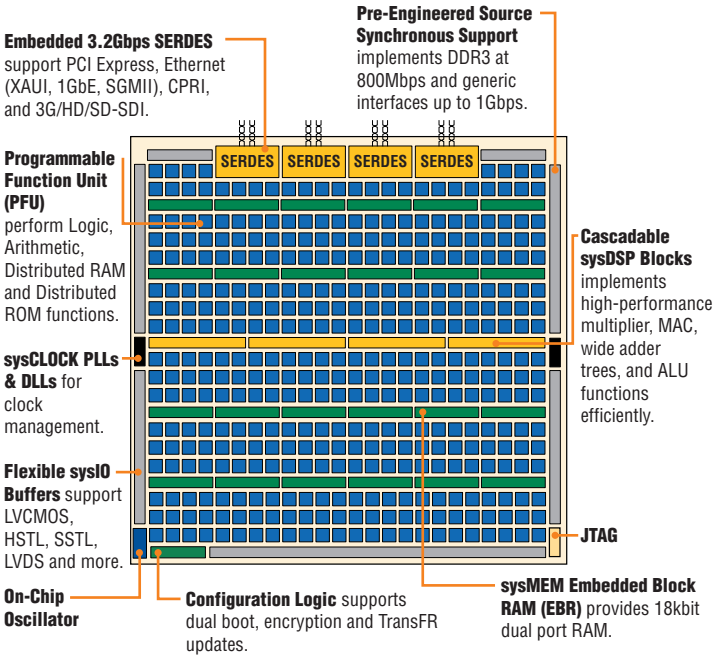
- Configure with SPI boot flash or parallel burst mode flash
- Protect your designs with 128-bit AES
- Dual-boot provides backup configuration copy
- TransFR™ I/O support updates while system operates

LatticeECP3 Architecture

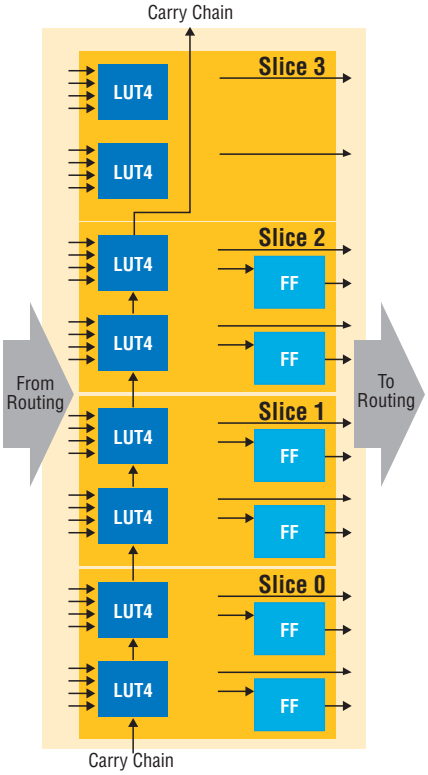
Architecture Overview

LatticeECP3 FPGAs utilize Lattice's third generation of cost optimized transceivers and a low-power 65-nm process FPGA architecture. Building on the successful LatticeECP2M™ FPGA family, LatticeECP3 devices deliver high-performance SERDES blocks, cascadable high-performance sysDSP™, ultra-high logic and sysMEM™ embedded RAM, distributed memory, sysCLOCK PLLs, DDR3 memory interface, and sysIO buffers. LatticeECP3 provides a low-cost, low-power programmable solution for a wide variety of wireless and wireline applications.

LatticeECP3 Block Diagram



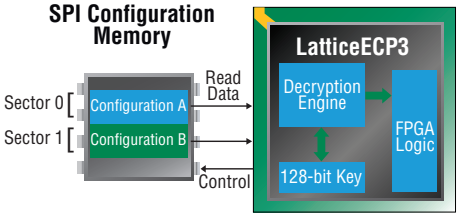
Programmable Function Unit (PFU) Block Diagram



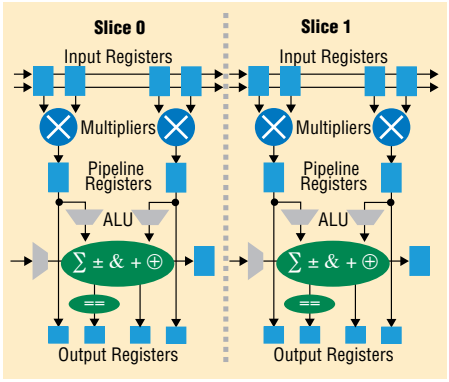
sysMEM Config Options

Single Port	Dual Port	Pseudo-Dual Port
16384 x 1	16384 x 1	16384 x 1
8192 x 2	8192 x 2	8192 x 2
4096 x 4	4096 x 4	4096 x 4
2048 x 9	2048 x 9	2048 x 9
1024 x 18	1024 x 18	1024 x 18
512 x 36	—	512 x 36

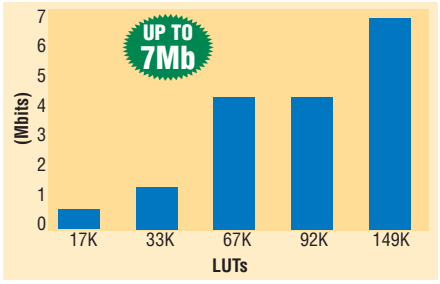
Dual-boot and 128-bit AES Encryption



sysDSP Block Diagram

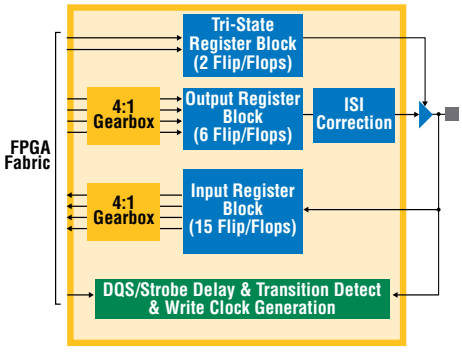


LatticeECP3 EBR SRAM (Mbits)

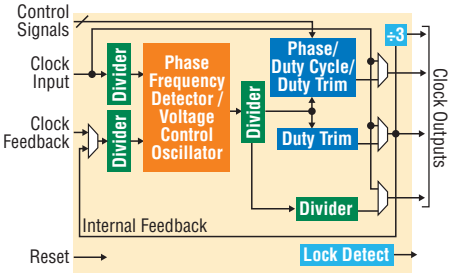


Pre-Engineered Source Synchronous Interfaces

- DDR3 (800 Mbps)
- 7:1 LVDS, ADC/DAC



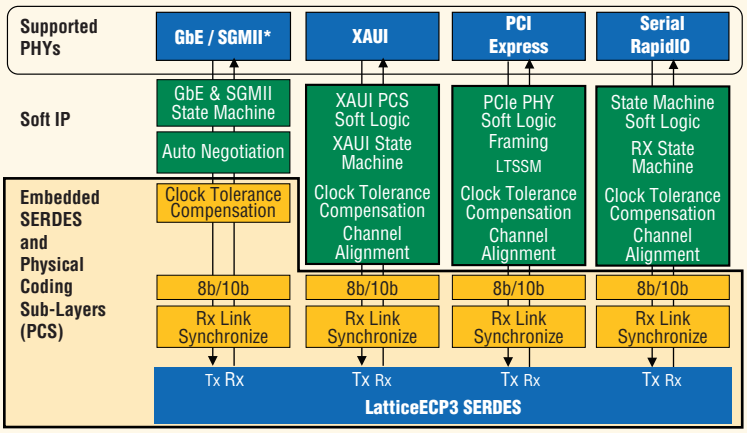
sysCLOCK PLL Block Diagram



High-Value, Low-Power Serial Protocol Solutions

LatticeECP3 Multi-Protocol Stack

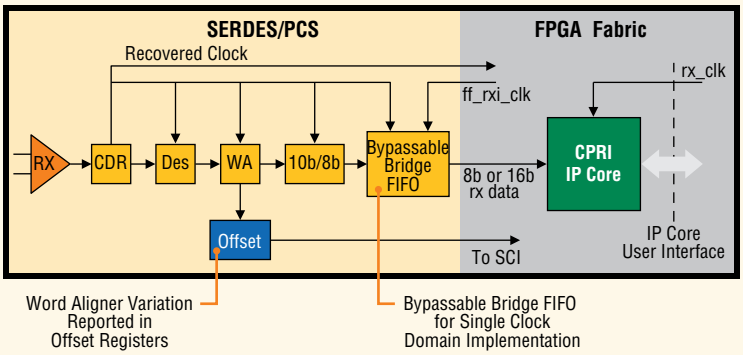
- Supports commonly used Ethernet protocols (1GbE, SGMII, and XAUI), Wireless protocols, such as CPRI, are supported by extension
- Supports PCI Express and Serial RapidIO



* CPRI Supported By Extension

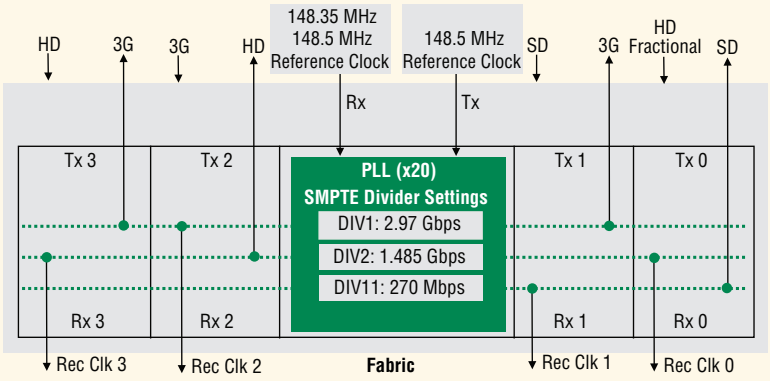
CPRI Low Latency Option

- Supports data rates for up to 3.072Gbps CPRI links
- Supports multi-hop RRH applications through innovative low-latency variation SERDES implemementation
- Library of CPRI, JESD204A, SRIO, Ethernet and DSP cores and reference designs for single-chip RF and baseband implementations



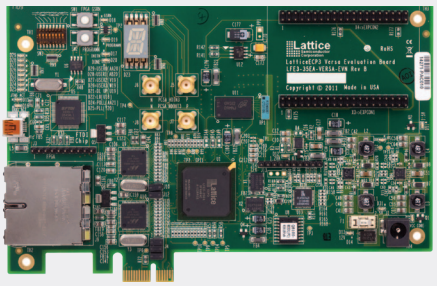
Enhanced SMPTE Support

- Any rate, any channel, any direction for SD/HD and 3G
  - New x11 divider setting
  - Added independent Rx clocking per channel
- Truly independent Rx/Tx multi-rate support for SD/HD/3G!



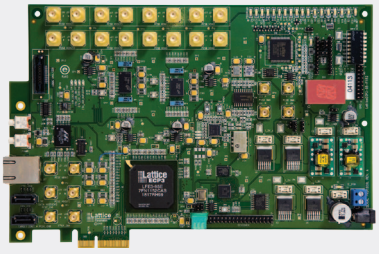
Evaluation & Development Boards

To accelerate your design development, Lattice offers several development boards to support LatticeECP3 designs. These boards enable you to evaluate the benefits and capabilities of LatticeECP3 devices in a lab setting.

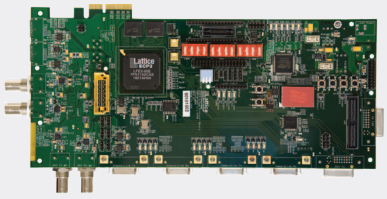


The LatticeECP3 Versa Evaluation Board is the industry's lowest cost FPGA board with PCI Express and two Gigabit Ethernet ports. It is useful for appreciating the quality of LatticeECP3 SERDES and developing a wide-range of networking and system design applications.

The Lattice HDR-60 Video Camera Development Kit is an FPGA-based HDR camera capable of supporting 1080p60 over HDMI/DVI output. The design needs no external frame buffer, enabling the lowest cost FPGA HDR camera BOM. Features include Auto White Balance, industry's fastest auto-exposure, extremely low-latency and 120dB High Dynamic Range.



The LatticeECP3 Serial Protocol Board provides a platform to evaluate the LatticeECP3 device's multi-protocol serial protocol functionality as well as DDR2 and DDR3 memory interfaces.



The LatticeECP3 Video Protocol Board provides a platform to evaluate the LatticeECP3 device's multi-rate 3G/HD/SDI and 7:1 LVDS capabilities. Breakout options for other display interfaces are also available.

Design Made Simple with Advanced Design Software and IP

Lattice Diamond Design Software

Lattice Diamond® design software offers leading-edge design and implementation tools optimized for cost sensitive, low-power Lattice FPGA architectures. Diamond is the next generation replacement for ispLEVER® featuring design exploration, ease of use, improved design flow, and numerous other enhancements. The combination of new and enhanced features allows users to complete designs faster, easier, and with better results than ever before.

Intellectual Property

Lattice offers an expanding portfolio of IP cores (LatticeCORE™) to support the easy integration of commonly used functions. Lattice also offers IP Suites that are a collection of related IP cores for select applications/markets at very attractive prices. The following table provides a partial listing of IP Suites available for the LatticeECP3 family. In addition to these, LatticeCORE Connections Partners also offer a wide range of IP. For a complete list of IP options, please visit www.latticesemi.com/ip.

LatticeCORE IP Suites for LatticeECP3 FPGAs

IP Suite	Included IP Cores	
Value	• DDR3/DDR2/DDR Memory Controller • FFT Compiler	• FIR Filter Generator • Triple Speed 10/100/1G Ethernet MAC
PCI Express	• PCI Express Endpoint x1 / x4 • PCI Express Root Complex Lite x1 / x4 • PCI Target 32-bit / 64-bit	• PCI Master/Target 32-bit / 64-bit • Scatter Gather DMA
Gigbit Ethernet	• 10Gb+ Ethernet MAC • Scatter Gather DMA • SGMII & Gigabit Ethernet MAC	• Triple Speed 10/100/1G Ethernet MAC • XAUI
Signal Processing	• Advanced FIR Filter • Block Convolutional Encoder • Block Viterbi Decoder • Cascaded Integrated Comb Filter - CIC • CORDIC • Correlator • Distributed Arithmetic FIR Filter	• Dynamic Block Reed Solomon Decoder / Encoder • FFT Compiler • FIR Filter Generator • Interleaver / De-interleaver • Numerically Controlled Oscillator • Turbo Decoder / Encoder
Video & Display	• 2D FIR Filter • Color Space Converter • Edge Detector • Gamma Corrector	• Median Filter • Tri-rate SDI PHY • Scaler

LatticeECP3 (Economy Plus FPGAs with SERDES, sysDSP Blocks, & Source Synchronous I/O)

Parameter	ECP3-17	ECP3-35	ECP3-70	ECP3-95	ECP3-150
LUTs (K)	17	33	67	92	149
Number of EBR SRAM Blocks	38	72	240	240	372
EBR Block SRAM (K bits)	700	1327	4420	4420	6850
Distributed RAM (K bits)	36	68	145	188	303
18x18 Embedded Multipliers	24	64	128	128	320
3.2Gbps SERDES Channels	4	4	12	12	16
Maximum Available I/O	222	310	490	490	586
Number of PLLs/DLLs	2+2	4+2	10+2	10+2	10+2
Power Grades[1]	-S, -L	-S, -L	-S, -L	-S, -L	-S, -L
Speed Grades[2]	-6, -7, -8	-6, -7, -8, -9	-6, -7, -8, -9	-6, -7, -8, -9	-6, -7, -8, -9
Packages & SERDES / I/O Combinations					
328-ball csBGA (10 x 10 mm)	2/116				
256-ball ftBGA (17 x 17 mm)	4/133	4/133			
484-ball fpBGA (23 x 23 mm)	4/222	4/295	4/295	4/295	
672-ball fpBGA (27 x 27 mm)		4/310	8/380	8/380	8/380
1156-ball fpBGA (35 x 35 mm)			12/490	12/490	16/586

1. -S = Standard Power; -L = Low Power
2. -9 = High-Speed Device

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