

Fully integrated stepper motor driver mounting the L6470

Data brief – production data

Features

- Voltage range from 8 V to 45 V
- Phase current up to 3 A_{rms}
- SPI with daisy-chain feature
- Socket for external resonator or crystal
- SW input
- FLAG and BUSY LED indicators
- Adjustable supply voltage compensation
- Suitable to be used in combination with STEVAL-PCC009V2

Description

The EVAL6470H demonstration board is a fully integrated microstepping motor driver. In combination with the STEVAL-PCC009V2 communication board and the dSPIN evaluation software, the board allows the user to investigate all the features of the L6470 device. In particular, the board can be used to check the voltage mode driving and to regulate the L6470 parameters in order to fit the application requirements.

The EVAL6470H supports the daisy-chain configuration making it suitable for the evaluation of the L6470 in multi-motor applications.



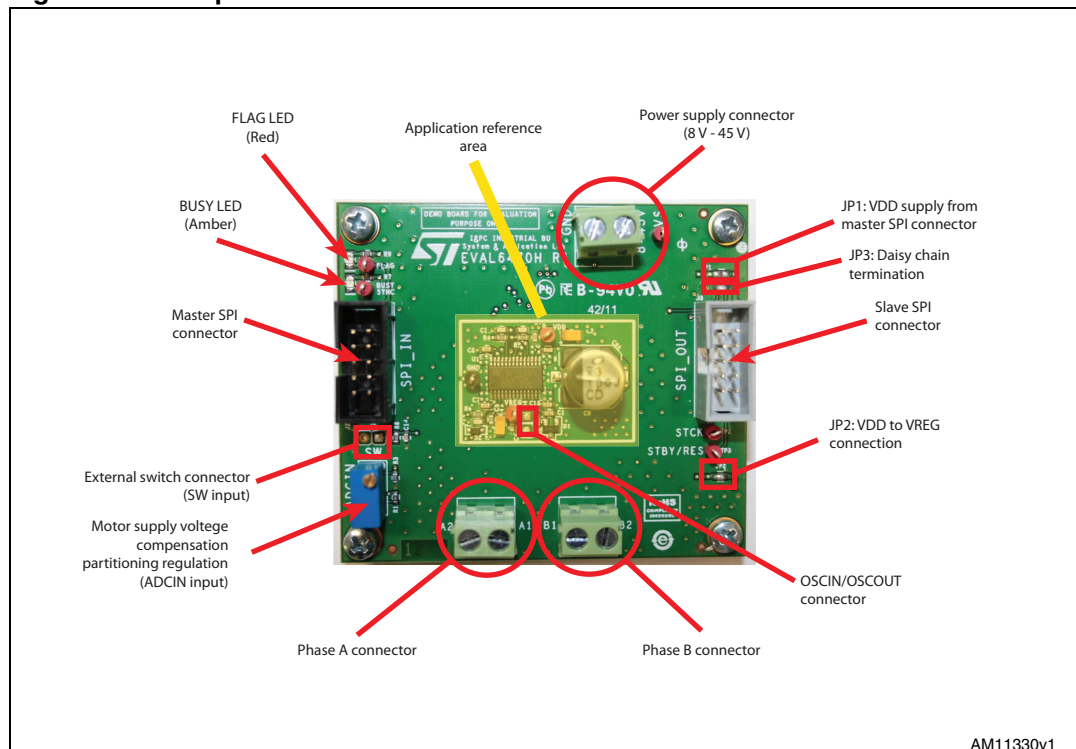
1 Board description

Table 1. EVAL6470H specifications

| Parameter | Value |
|---|--|
| Supply voltage (VS) | 8 to 45 V |
| Maximum output current (each phase) | 3 A _{r.m.s.} |
| Logic supply voltage (VREG) | Externally supplied: 3.3 V, internally supplied: 3 V (typ.) |
| Logic interface voltage (VDD) | Externally supplied: 3.3 V or 5 V, internally supplied: VREG |
| Low level logic inputs voltage | 0 V |
| High level logic input voltage | VDD ⁽¹⁾ |
| Operating temperature | -25 to +125 °C |
| L6470H thermal resistance junction-to-ambient | 21 °C/W (typ.) |

1. All logic inputs are 5 V tolerant.

Figure 1. Jumpers and connectors location



AM11330v1

Table 2. Jumpers and connectors description

| Name | Type | Function |
|-----------------|---------------|--|
| J1 | Power supply | Motor supply voltage |
| J5 | Power output | Bridge A outputs |
| J6 | Power output | Bridge B outputs |
| J2 | SPI connector | Master SPI |
| J3 | SPI connector | Slave SPI |
| J4 | NM connector | OSCIN and OSCOUT pins |
| J7 | NM connector | External switch input |
| TP1 (VS) | Test point | Motor supply voltage test point |
| TP4 (VDD) | Test point | Logic interface supply voltage test point |
| TP5 (VREG) | Test point | Logic supply voltage/L6470 internal regulator test point |
| TP6 (GND) | Test point | Ground test point |
| TP2 (STCK) | Test point | Step clock input test point |
| TP3 (STBY/RES) | Test point | Standby/reset input test point |
| TP7 (FLAG) | Test point | FLAG output test point |
| TP8 (BUSY/SYNC) | Test point | BUSY/SYNC output test point |

Table 3. Master SPI connector pinout (J10)

| Pin number | Type | Description |
|------------|-------------------|---|
| 1 | Open drain output | L6470 BUSY/SYNC output |
| 2 | Open drain output | L6470 FLAG output |
| 3 | Ground | Ground |
| 4 | Supply | EXT_VDD (can be used as external logic power supply) |
| 5 | Digital output | SPI Master-In Slave-Out signal (connected to L6470 SDO output through daisy-chain termination jumper JP2) |
| 6 | Digital input | SPI serial clock signal (connected to L6470 CK input) |
| 7 | Digital input | SPI Master-Out Slave-In signal (connected to L6470 SDI input) |
| 8 | Digital input | SPI slave select signal (connected to L6470 CS input) |
| 9 | Digital input | L6470 step-clock input |
| 10 | Digital input | L6470 STBY/RST input |

Table 4. Slave SPI connector pinout (J11)

| Pin number | Type | Description |
|------------|-------------------|------------------------|
| 1 | Open drain output | L6470 BUSY/SYNC output |
| 2 | Open drain output | L6470 FLAG output |

Table 4. Slave SPI connector pinout (J11) (continued)

| Pin number | Type | Description |
|------------|----------------|--|
| 3 | Ground | Ground |
| 4 | Supply | EXT_VDD (can be used as external logic power supply) |
| 5 | Digital output | SPI Master-In Slave-Out signal (connected to pin 5 of J10) |
| 6 | Digital input | SPI serial clock signal (connected to L6470 CK input) |
| 7 | Digital input | SPI Master-Out Slave-In signal (connected to L6470 SDO output) |
| 8 | Digital input | SPI slave select signal (connected to L6470 CS input) |
| 9 | Digital input | L6470 step-clock input |
| 10 | Digital input | L6470 STBY/RST input |

Figure 2. EVAL6470H - schematic

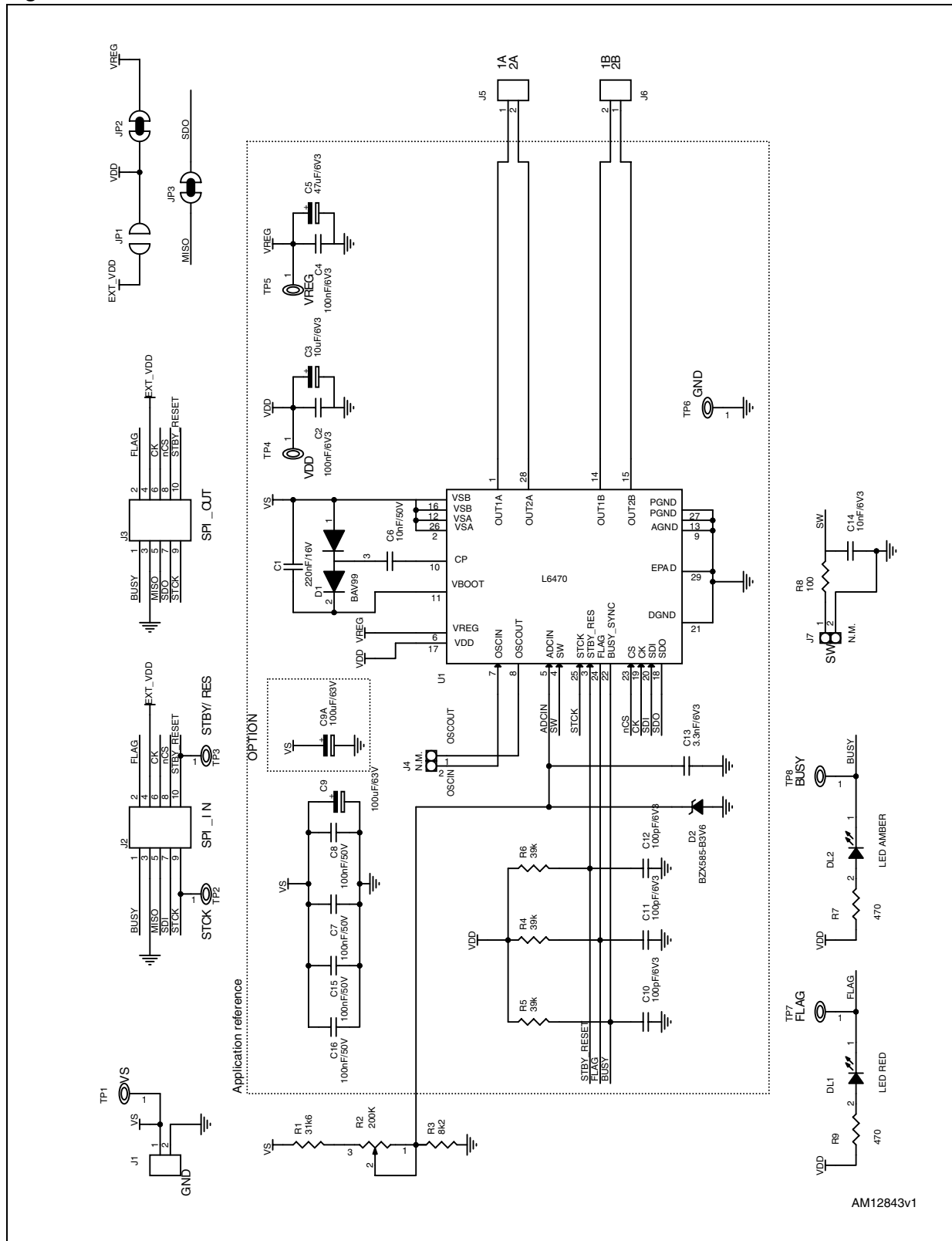


Table 5. EVAL6470H - bill of material

| Item | Quantity | Reference | Value | Package |
|------|----------|--|--|----------------------|
| 1 | 1 | C1 | 220 nF/16 V | CAPC-0603 |
| 2 | 2 | C2,C4 | 100 nF/6.3 V | CAPC-0603 |
| 3 | 1 | C3 | 10 μ F/6.3 V | CAPC-3216 |
| 4 | 1 | C5 | 47 μ F/6.3 V | CAPC-3216 |
| 5 | 1 | C6 | 10 nF/50 V | CAPC-0603 |
| 6 | 4 | C7,C8,C15,C16 | 100 nF/50 V | CAPC-0603 |
| 7 | 1 | C9A | 100 μ F/63 V | CAPE-R8H12-P35 |
| 8 | 1 | C9 | 100 μ F/63 V | CAPE-R10HXX |
| 9 | 3 | C10,C11,C12 | 100 pF/6.3 V | CAPC-0603 |
| 10 | 1 | C13 | 3.3 nF/6.3 V | CAPC-0603 |
| 11 | 1 | C14 | 10 nF/6.3 V | CAPC-0603 |
| 12 | 1 | DL1 | LED diode (red) | LEDC-0805 |
| 13 | 1 | DL2 | LED diode (amber) | LEDC-0805 |
| 14 | 1 | D1 | BAV99 | SOT23 |
| 15 | 1 | D2 | BZX585-B3V6(1) | SOD523 |
| 16 | 1 | JP1 | Jumper - OPEN | JP2SO |
| 17 | 2 | JP2,JP3 | Jumper - CLOSED | JP2SO |
| 18 | 3 | J1,J5,J6 | Screw connector 2 poles | MORSV-508-2P |
| 19 | 2 | J2,J3 | Pol. IDC male header vertical 10 poles | CON-FLAT-5X2-180M |
| 20 | 2 | J4,J7 | N.M. | STRIP254P-M-2 |
| 21 | 1 | R1 | 31.6 k Ω | RESC-0603 |
| 22 | 1 | R2 | 200 k Ω | TRIMM-100X50X110-64W |
| 23 | 1 | R3 | 8.2 k Ω | RESC-0603 |
| 24 | 3 | R4,R5,R6 | 39 k Ω | RESC-0603 |
| 25 | 2 | R7,R9 | 470 Ω | RESC-0603 |
| 26 | 1 | R8 | 100 Ω | RESC-0603 |
| 27 | 8 | TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8 | Test point | TH |
| 28 | 1 | U1 | L6470H | HTSSOP28 |

Figure 3. EVAL6470H - layout (silk screen)

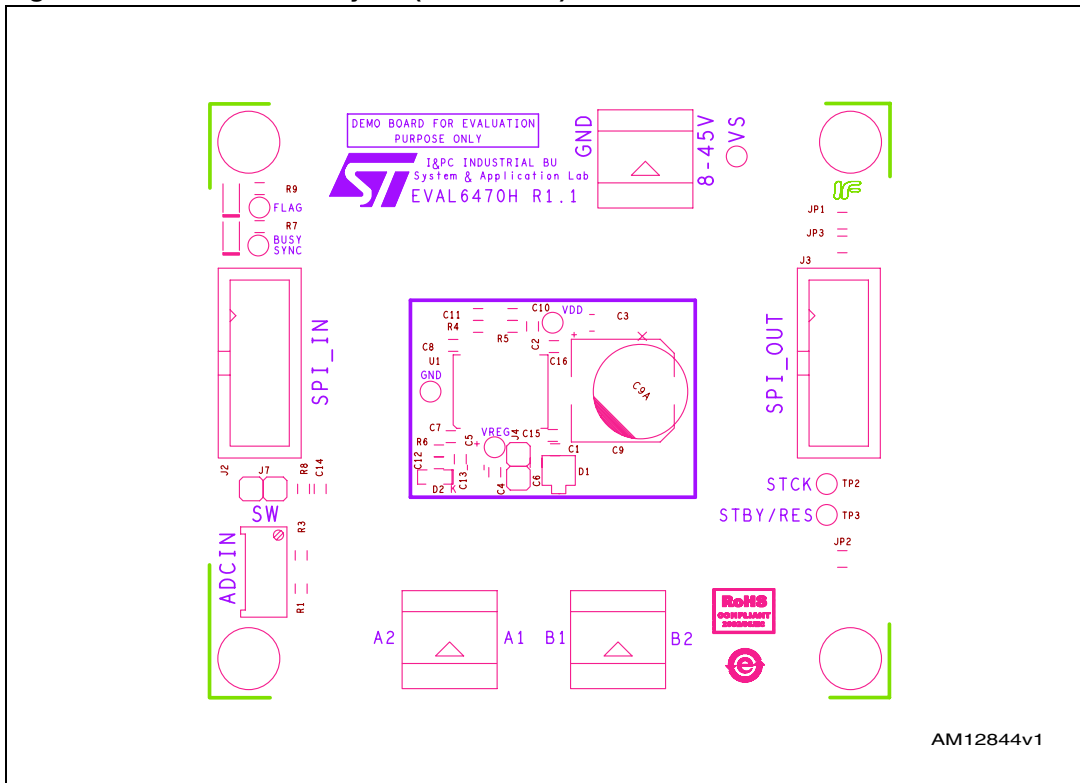


Figure 4. EVAL6470H - layout (top layer)

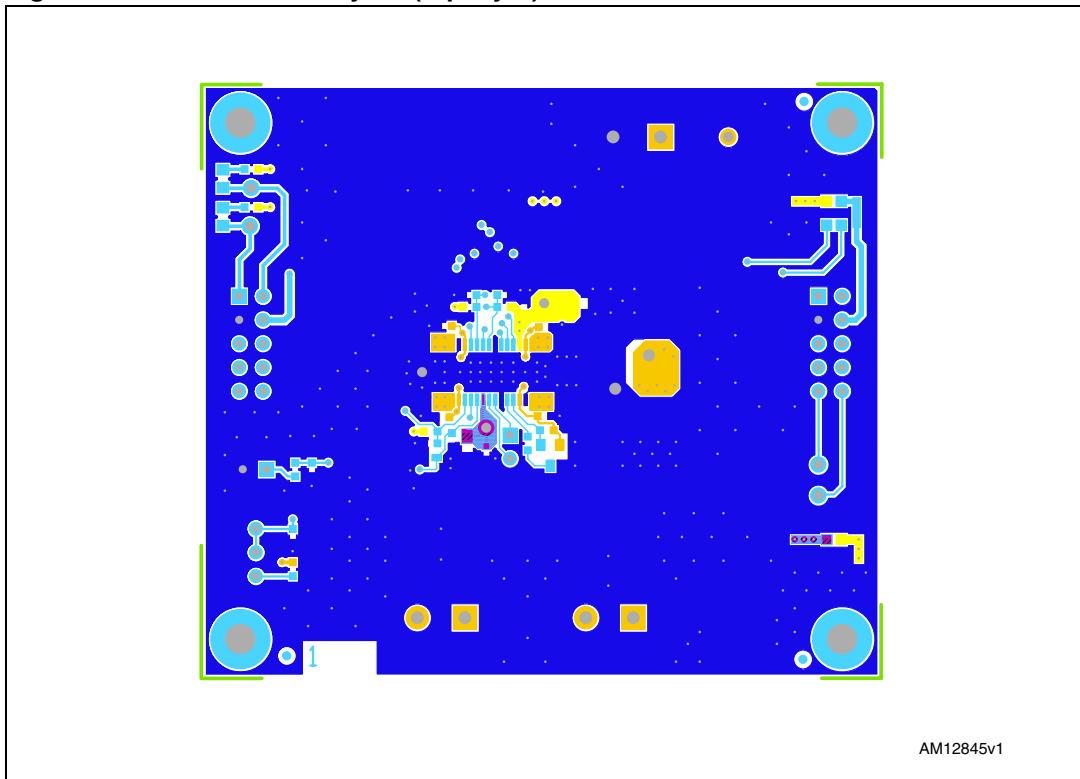


Figure 5. EVAL6470H - layout (inner layer 2)

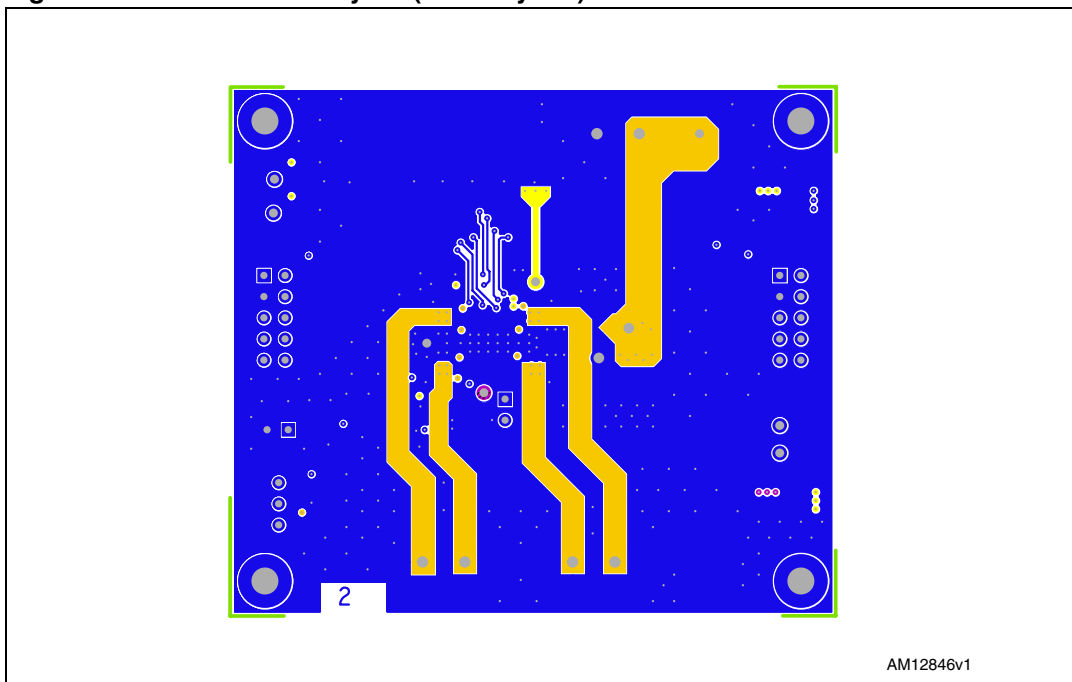


Figure 6. EVAL6470H - layout (inner layer 3)

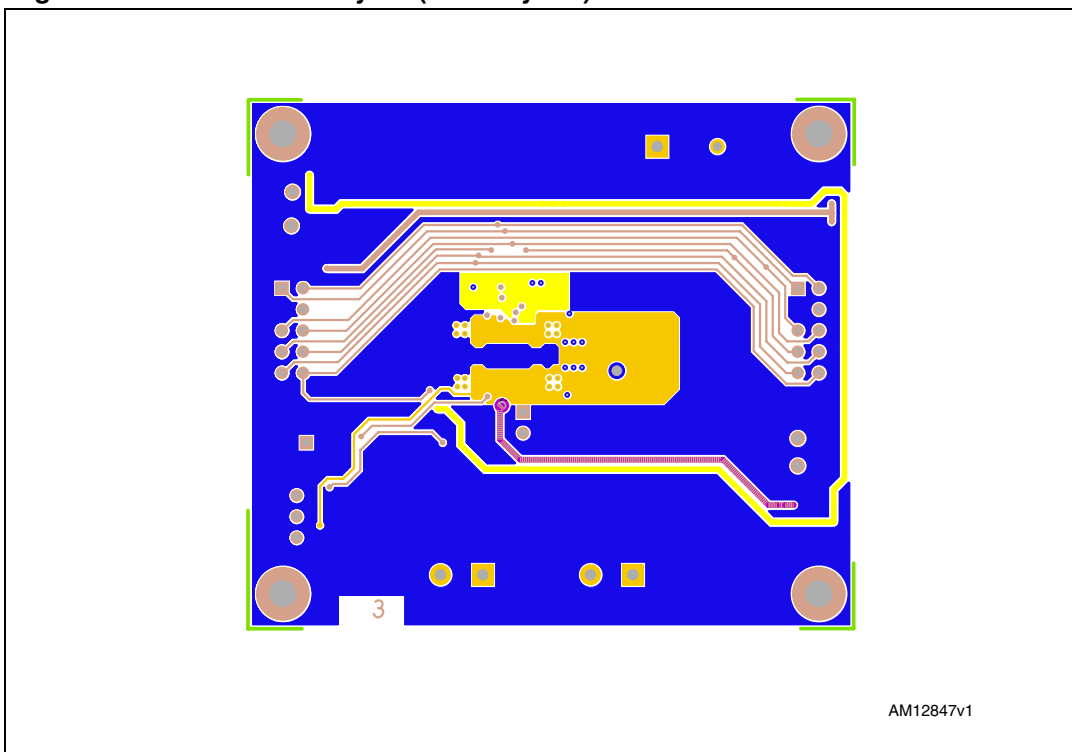
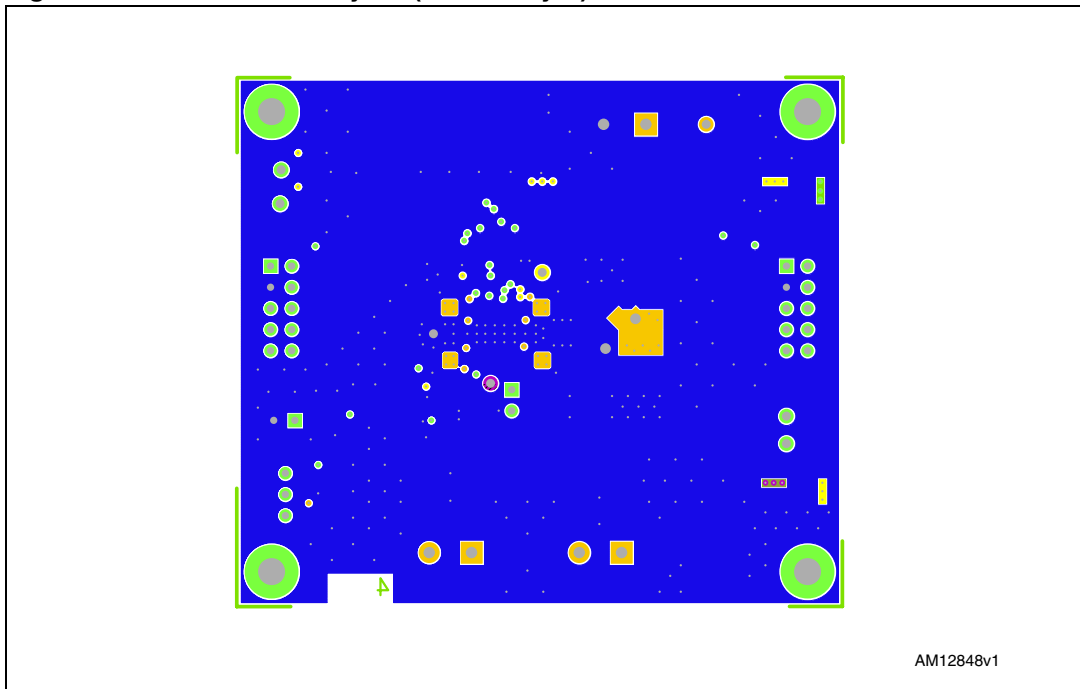
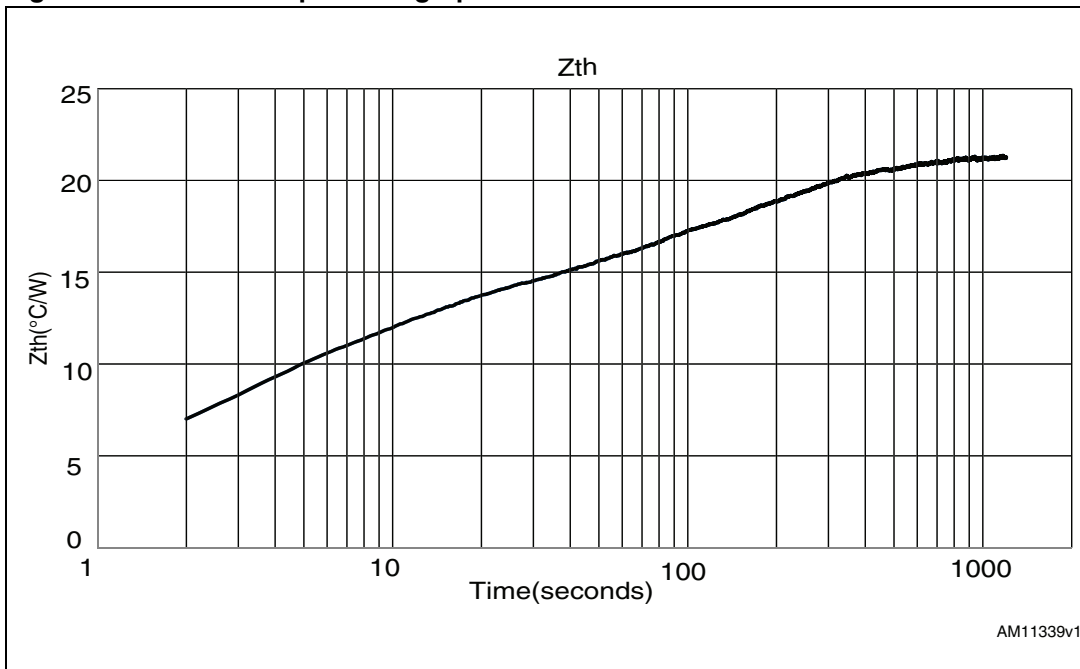


Figure 7. EVAL6470H - layout (bottom layer)



1.1 Thermal data

Figure 8. Thermal impedance graph



2 Revision history

Table 6. Document revision history

| Date | Revision | Changes |
|-------------|----------|--|
| 25-Jan-2012 | 1 | Initial release. |
| 23-Apr-2012 | 2 | Updated information: Table 2 for connector TP3 (STBY/RES). Table 3 , and Table 4 description changed for pin 1 and pin 10 Table 5 for item 15. Updated: Figure 2 , Figure 3 , Figure 4 , Figure 5 , Figure 6 , and Figure 7 . |

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