FAIRCHILD SEMICONDUCTOR®

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# BSS123

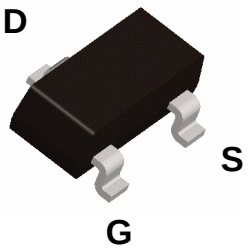
## N-Channel Logic Level Enhancement Mode Field Effect Transistor

### General Description

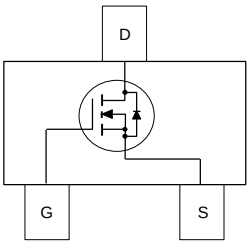
These N-Channel enhancement mode field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. These products have been designed to minimize on-state resistance while provide rugged, reliable, and fast switching performance.These products are particularly suited for low voltage, low current applications such as small servo motor control, power MOSFET gate drivers, and other switching applications.

### Features

- 0.17 A, 100 V. $R_{DS(ON)}$ = 6Ω @ $V_{GS}$ = 10 V
  $R_{DS(ON)}$ = 10Ω @ $V_{GS}$ = 4.5 V
- High density cell design for extremely low $R_{DS(ON)}$
- Rugged and Reliable
- Compact industry standard SOT-23 surface mount package




SOT-23




## Absolute Maximum Ratings

$T_A$=25°C unless otherwise noted

| Symbol | Parameter | | Ratings | Units |
|---|---|---|---|---|
| $V_{DSS}$ | Drain-Source Voltage | | 100 | V |
| $V_{GSS}$ | Gate-Source Voltage | | ±20 | V |
| $I_D$ | Drain Current – Continuous | (Note 1) | 0.17 | A |
| | – Pulsed | | 0.68 | |
| $P_D$ | Maximum Power Dissipation | (Note 1) | 0.36 | W |
| | Derate Above 25°C | | 2.8 | mW/°C |
| $T_J$, $T_{STG}$ | Operating and Storage Junction Temperature Range | | –55 to +150 | °C |
| $T_L$ | Maximum Lead Temperature for Soldering Purposes, 1/16" from Case for 10 Seconds | | 300 | |

## Thermal Characteristics

| | | | | |
|---|---|---|---|---|
| $R_{\theta JA}$ | Thermal Resistance, Junction-to-Ambient | (Note 1) | 350 | °C/W |

## Package Marking and Ordering Information

| Device Marking | Device | Reel Size | Tape width | Quantity |
|---|---|---|---|---|
| SA | BSS123 | 7'' | 8mm | 3000 units |

## Electrical Characteristics

$T_A$ = 25°C unless otherwise noted

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Off Characteristics** | | | | | | |
| $BV_{DSS}$ | Drain–Source Breakdown Voltage | $V_{GS}$ = 0 V, $I_D$ = 250 µA | 100 | | | V |
| $\frac{\Delta BV_{DSS}}{\Delta T_J}$ | Breakdown Voltage Temperature Coefficient | $I_D$ = 250 µA,Referenced to 25°C | | 97 | | mV/°C |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$ = 100 V, $V_{GS}$ = 0 V | | | 1 | µA |
| | | $V_{DS}$ = 100 V,$V_{GS}$ = 0 V $T_J$ = 125°C | | | 60 | µA |
| | | $V_{DS}$ = 20 V, $V_{GS}$ = 0 V | | | 10 | nA |
| $I_{GSS}$ | Gate–Body Leakage. | $V_{GS}$ = ±20 V, $V_{DS}$ = 0 V | | | ±50 | nA |
| **On Characteristics** (Note 2) | | | | | | |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = 1 mA | 0.8 | 1.7 | 2 | V |
| $\frac{\Delta V_{GS(th)}}{\Delta T_J}$ | Gate Threshold Voltage Temperature Coefficient | $I_D$ = 1 mA,Referenced to 25°C | | –2.7 | | mV/°C |
| $R_{DS(on)}$ | Static Drain–Source On–Resistance | $V_{GS}$ = 10 V, $I_D$ = 0.17 A<br>$V_{GS}$ = 4.5 V, $I_D$ = 0.17 A<br>$V_{GS}$ = 10 V, $I_D$ = 0.17 A, $T_J$ = 125°C | | 1.2<br>1.3<br>2.2 | 6<br>10<br>12 | Ω |
| $I_{D(on)}$ | On–State Drain Current | $V_{GS}$ = 10 V, $V_{DS}$ = 5 V | 0.68 | | | A |
| $g_{FS}$ | Forward Transconductance | $V_{DS}$ = 10V, $I_D$ = 0.17 A | 0.08 | 0.8 | | S |
| **Dynamic Characteristics** | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{DS}$ = 25 V, $V_{GS}$ = 0 V, f = 1.0 MHz | | 73 | | pF |
| $C_{oss}$ | Output Capacitance | | | 7 | | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | | 3.4 | | pF |
| $R_G$ | Gate Resistance | $V_{GS}$ = 15 mV, f = 1.0 MHz | | 2.2 | | Ω |
| **Switching Characteristics** (Note 2) | | | | | | |
| $t_{d(on)}$ | Turn–On Delay Time | $V_{DD}$ = 30 V, $I_D$ = 0.28 A, $V_{GS}$ = 10 V, $R_{GEN}$ = 6 Ω | | 1.7 | 3.4 | ns |
| $t_r$ | Turn–On Rise Time | | | 9 | 18 | ns |
| $t_{d(off)}$ | Turn–Off Delay Time | | | 17 | 31 | ns |
| $t_f$ | Turn–Off Fall Time | | | 2.4 | 5 | ns |
| $Q_g$ | Total Gate Charge | $V_{DS}$ = 30 V, $I_D$ = 0.22 A, $V_{GS}$ = 10 V | | 1.8 | 2.5 | nC |
| $Q_{gs}$ | Gate–Source Charge | | | 0.2 | | nC |
| $Q_{gd}$ | Gate–Drain Charge | | | 0.3 | | nC |
| **Drain–Source Diode Characteristics and Maximum Ratings** | | | | | | |
| $I_S$ | Maximum Continuous Drain–Source Diode Forward Current | | | | 0.17 | A |
| $V_{SD}$ | Drain–Source Diode Forward Voltage | $V_{GS}$ = 0 V, $I_S$ = 0.34 A(Note 2) | | 0.8 | 1.3 | V |
| $t_{rr}$ | Diode Reverse Recovery Time | $I_F$ = 0.17 A, $d_{iF}/d_t$ = 100 A/µs | | 11 | | nS |
| $Q_{rr}$ | Diode Reverse Recovery Charge | | | 3 | | nC |

**NOTE:**

**1.** $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

a) 350°C/W when mounted on a minimum pad..

Scale 1 : 1 on letter size paper

**2.** Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2.0%

## Typical Characteristics

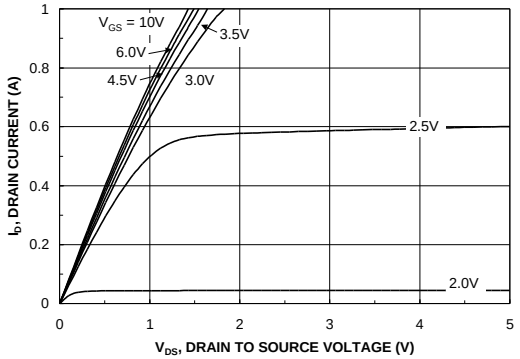



**Figure 1. On-Region Characteristics.**

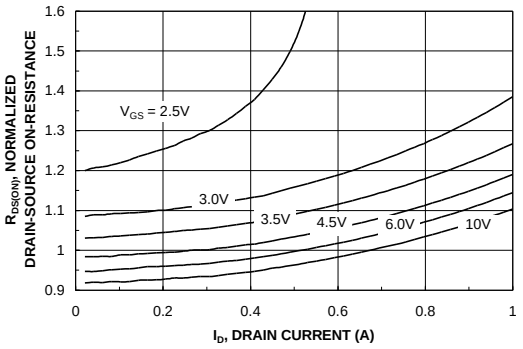



**Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.**

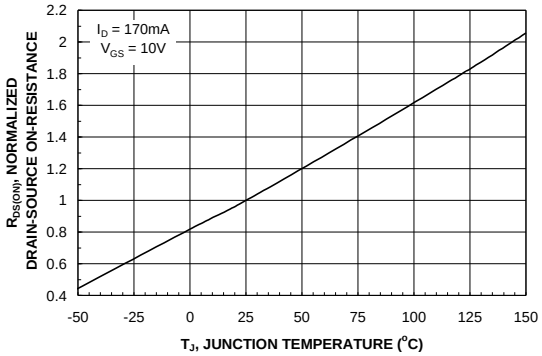



**Figure 3. On-Resistance Variation with Temperature.**

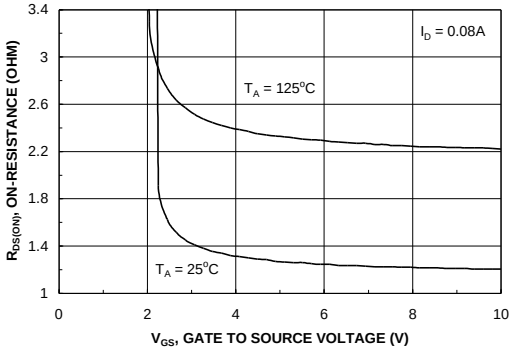



**Figure 4. On-Resistance Variation with Gate-to-Source Voltage.**

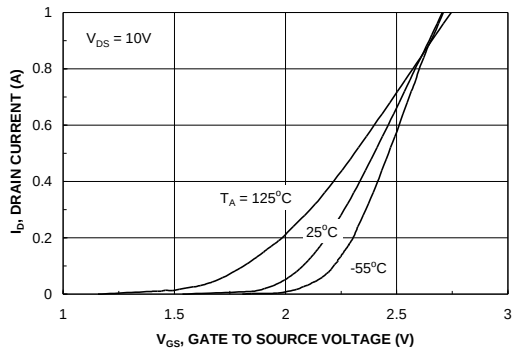



**Figure 5. Transfer Characteristics.**

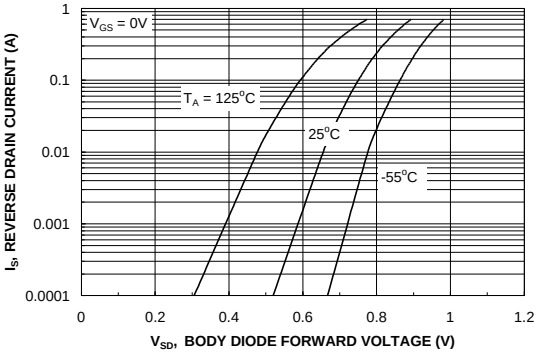



**Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.**

## Typical Characteristics

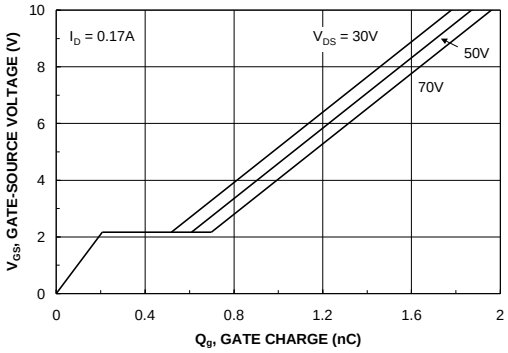



**Figure 7. Gate Charge Characteristics.**

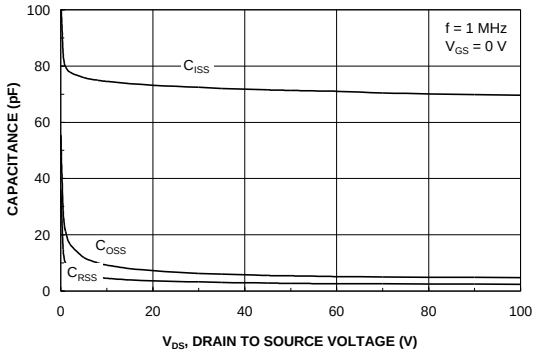



**Figure 8. Capacitance Characteristics.**

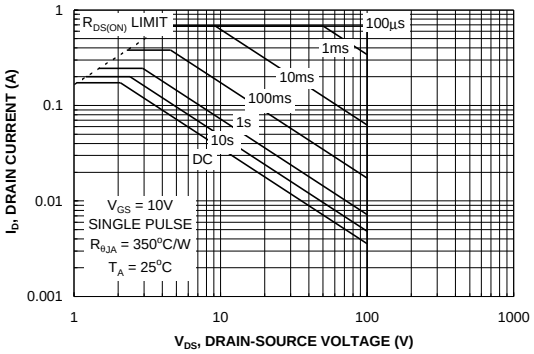



**Figure 9. Maximum Safe Operating Area.**

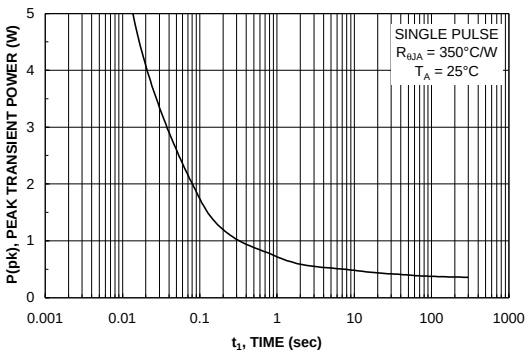



**Figure 10. Single Pulse Maximum Power Dissipation.**

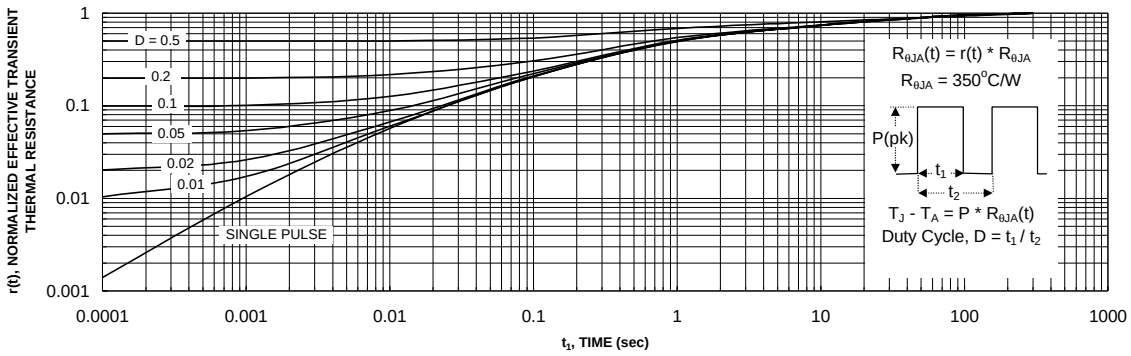



**Figure 11. Transient Thermal Response Curve.**

**Thermal characterization performed using the conditions described in Note 1a.**
**Transient thermal response will change depending on the circuit board design.**

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